

## AUTO-ZEROED OPERATIONAL AMPLIFIERS

### FEATURES

- First Monolithic Chopper-Stabilized Amplifier With On-Chip Nulling Capacitors
- Offset Voltage ..... 5 $\mu$ V
- Offset Voltage Drift ..... 0.05 $\mu$ V/ $^{\circ}$ C
- Low Supply Current ..... 350 $\mu$ A
- High Common-Mode Rejection ..... 116dB
- Single Supply Operation ..... 4.5V to 16V
- High Slew Rate ..... 2.5V/ $\mu$ s
- Wide Bandwidth ..... 1.5MHz
- High Open-Loop Voltage Gain (R<sub>L</sub> = 10 k $\Omega$ ) ..... 120dB
- Low Input Voltage Noise (0.1 Hz to 1 Hz) ..... 0.65 $\mu$ V<sub>P-P</sub>
- Pin Compatible With ICL7650
- Lower System Parts Count

### ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum Offset Voltage
TC911ACOA	8-Pin SOIC	0 $^{\circ}$ C to +70 $^{\circ}$ C	15 $\mu$ V
TC911ACPA	8-Pin Plastic DIP	0 $^{\circ}$ C to +70 $^{\circ}$ C	15 $\mu$ V
TC911BCOA	8-Pin SOIC	0 $^{\circ}$ C to +70 $^{\circ}$ C	30 $\mu$ V
TC911BCPA	8-Pin Plastic DIP	0 $^{\circ}$ C to +70 $^{\circ}$ C	30 $\mu$ V

### GENERAL DESCRIPTION

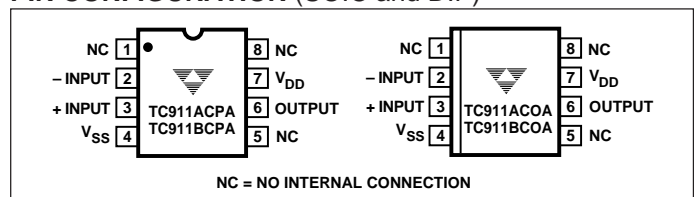
The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user-supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional OP07 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count, reduced assembly time and cost, greater system reliability, reduced PC board layout effort and greater board area utilization. Space savings can be significant in multiple-amplifier designs.

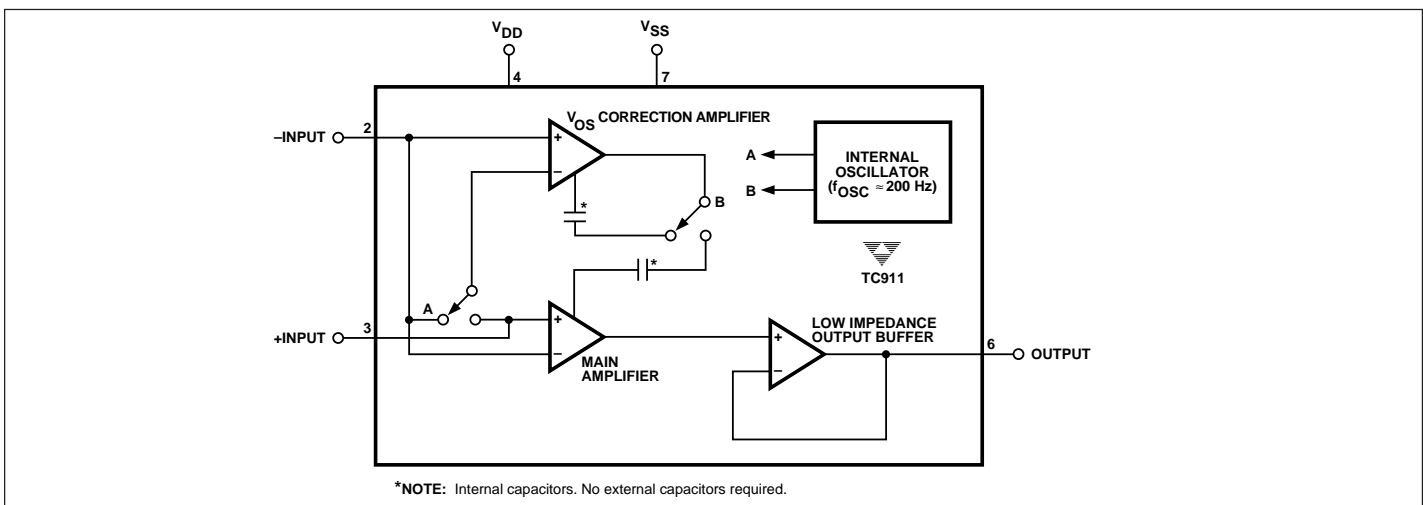
Electrical specifications include 15 $\mu$ V maximum offset voltage, 0.15 $\mu$ V/ $^{\circ}$ C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

The TC911 operates from dual or single power supplies. Supply current is typically 350 $\mu$ A. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC911 is available in 2 package types: 8-pin plastic DIP and SOIC.

### PIN CONFIGURATION (SOIC and DIP)



### FUNCTIONAL BLOCK DIAGRAM



# AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIERS

## TC911A TC911B

### ABSOLUTE MAXIMUM RATINGS\*

Total Supply Voltage ( $V_{DD}$ to $V_{SS}$ )	+18V
Input Voltage	( $V_{DD} + 0.3V$ ) to ( $V_{SS} - 0.3V$ )
Current into Any Pin	10mA
While Operating	100 $\mu$ A
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Operating Temperature Range	
C Device	0°C to +70°C

Package Power Dissipation ( $T_A = \leq 70^\circ\text{C}$ )

Plastic DIP	730mW
Plastic SOIC	470mW

\*Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

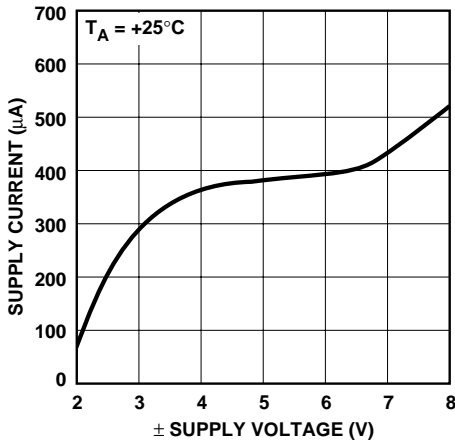
### ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ , $T_A = +25^\circ\text{C}$ , unless otherwise indicated.

Symbol	Parameter	Test Conditions	TC911A			TC911B			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{OS}$	Input Offset Voltage	$T_A = +25^\circ\text{C}$	—	5	15	—	15	30	$\mu\text{V}$
$TCV_{OS}$	Average Temperature Coefficient of Input Offset Voltage	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	—	0.05	0.15	—	0.1	0.25	$\mu\text{V}/^\circ\text{C}$
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ (Note 1)	—	0.05	0.15	—	0.1	0.25	$\mu\text{V}/^\circ\text{C}$
$I_B$	Average Input Bias Current	$T_A = +25^\circ\text{C}$	—	—	70	—	—	120	pA
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	—	—	3	—	—	4	nA
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	—	4	—	—	6	nA
$I_{OS}$	Average Input Offset Current	$T_A = +25^\circ\text{C}$	—	5	20	—	10	40	pA
		$T_A = +85^\circ\text{C}$	—	—	1	—	—	1	nA
$e_N$	Input Voltage Noise	0.1 to 1 Hz, $R_S \leq 100\Omega$	—	0.65	—	—	0.65	—	$\mu\text{V}_{P-P}$
		0.1 to 10 Hz, $R_S \leq 100\Omega$	—	11	—	—	11	—	$\mu\text{V}_{P-P}$
CMRR	Common-Mode Rejection Ratio	$V_{SS} \leq V_{CM} \leq V_{DD} - 2.2$	110	116	—	105	110	—	dB
CMVR	Common-Mode Voltage Range		$V_{SS}$	—	$V_{DD} - 2$	$V_{SS}$	—	$V_{DD} - 2$	V
$A_{OL}$	Open-Loop Voltage Gain	$R_L = 10\text{ k}\Omega$ , $V_{OUT} = \pm 4V$	115	120	—	110	120	—	dB
$V_{OUT}$	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	$V_{SS} + 0.3$	—	$V_{DD} - 0.9$	$V_{SS} + 0.3$	—	$V_{DD} - 0.9$	V
BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$	—	2.5	—	—	2.5	—	V/ $\mu\text{s}$
PSRR	Power Supply Rejection Ratio	$\pm 3.3V$ to $\pm 5.5V$	112	—	—	105	—	—	dB
$V_S$	Operating Supply Voltage Range	Split Supply	$\pm 3.3$	—	$\pm 8$	$\pm 3.3$	—	$\pm 8$	V
		Single Supply	6.5	—	16	6.5	—	16	V
$I_S$	Quiescent Supply Current	$V_S = \pm 5V$	—	350	600	—	—	800	$\mu\text{A}$

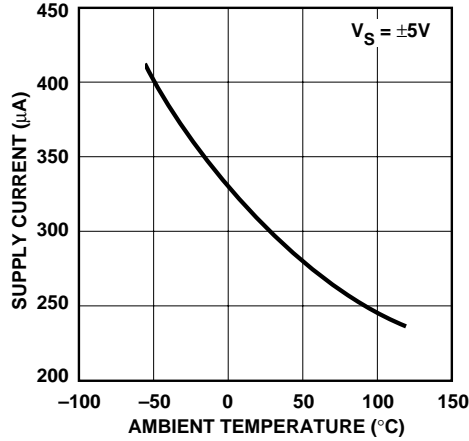
NOTES: 1. Characterized; not 100% tested.

## TYPICAL CHARACTERISTICS

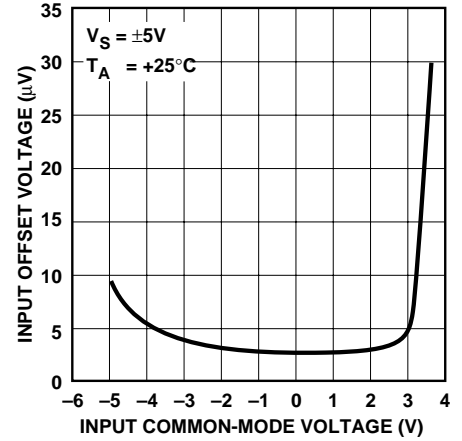
Supply Current vs.  $\pm$  Supply Voltage



Supply Current vs. Temperature

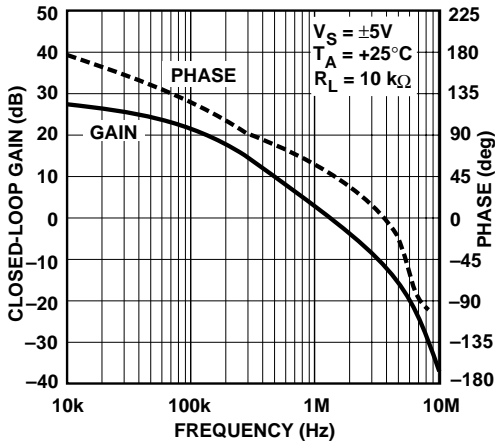


Input Offset Voltage vs. Common-Mode Voltage

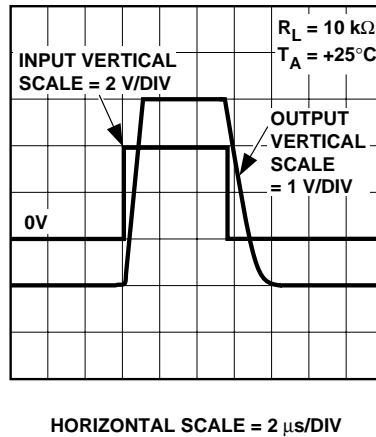


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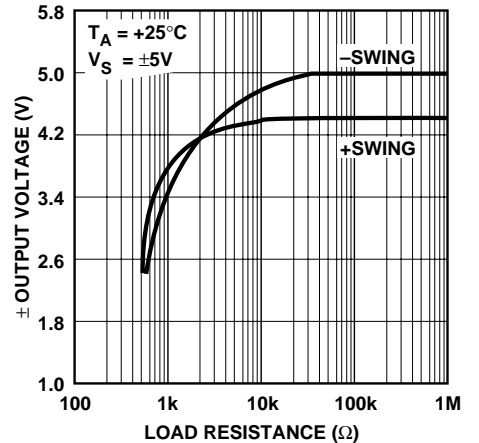
Gain and Phase vs. Frequency



Large Signal Output Switching Waveform



Output Voltage Swing vs. Load Resistance



## TC911A TC911B

### Pin Compatibility

The CMOS TC911 is pin compatible with the industry standard ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1μF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TC911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time, and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op amps: 741, LM101, LM108, OP05–OP08, OP-20, OP-21, ICL7650 and ICL7652. In many applications operating from +5V supplies the TC911 offers superior electrical performance and can be a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs.

### Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage

(Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1μV/°C to 10μV/°C. Thermal-induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and thermocouple-induced errors.

### Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible input current should be limited to 0.1mA to avoid triggering the p-n-p-n structure.

### Overload Recovery

The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20msec. Negative output saturation recovery time is typically 5msec.

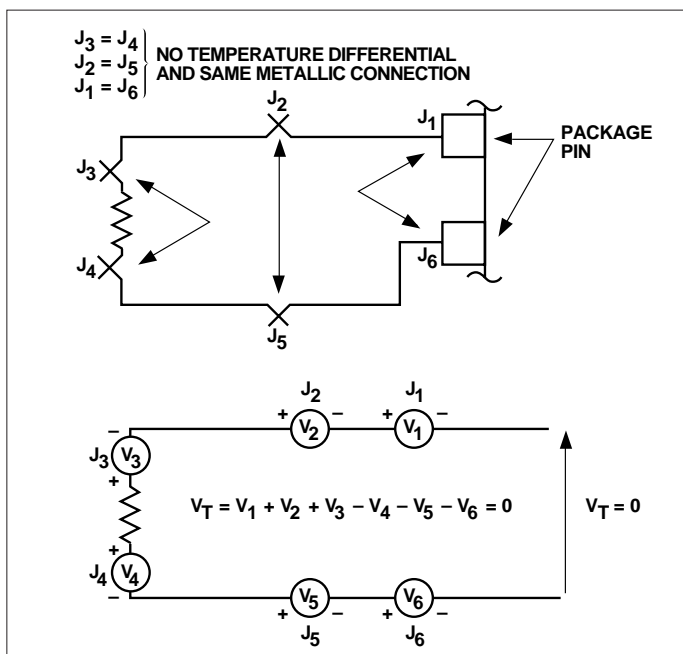


Figure 1. Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

### TYPICAL APPLICATIONS

