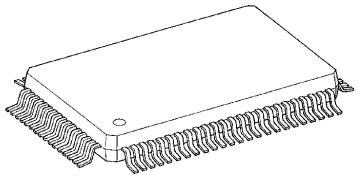
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9240F

AUDIO LCD DRIVER IC

The TC9240F is a driver IC designed for exclusive use for output expansion LCD which is controlled by serial data.



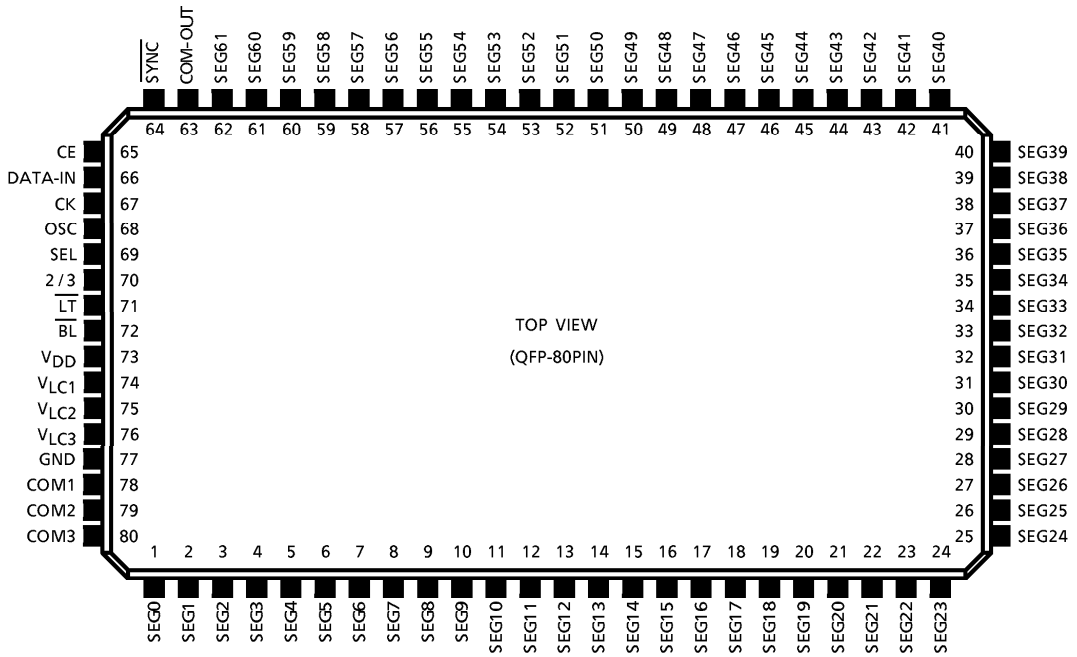
QFP80-P-1420-0.80A

Weight : 1.57g (Typ.)

FEATURES

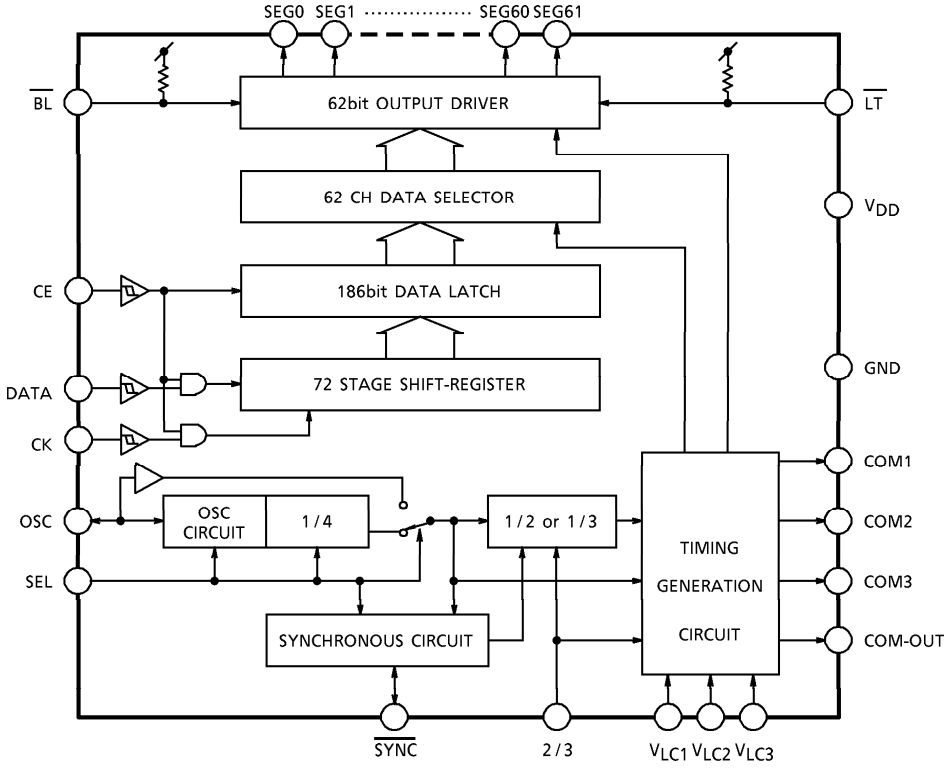
- 1/2 or 1/3 duty and 1/2 or 1/3 bias can be switched.
- Max. 124 segments can be displayed in the 1/2 duty mode and 186 segments in the 1/3 duty mode.
- Built-in display synchronizing circuit enables display in multi-chip configuration.
- Built-in oscillation circuit with externally connected capacitor and resistor.
- Connected to the controller using the tree-wire system.
- Display data split in 3 segment blocks enables efficient data transfer.

PIN CONNECTION

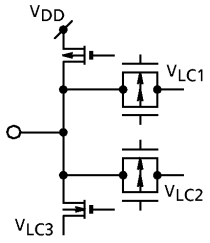
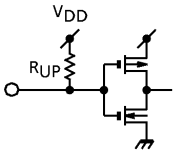


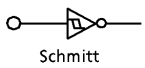
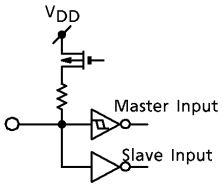
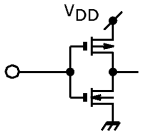
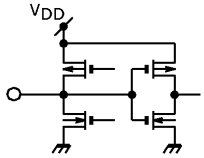
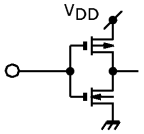
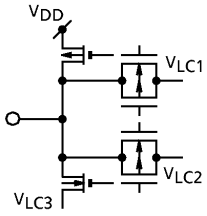
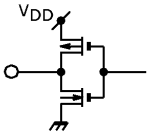
980508EBA2

BLOCK DIAGRAM



PIN DESCRIPTION

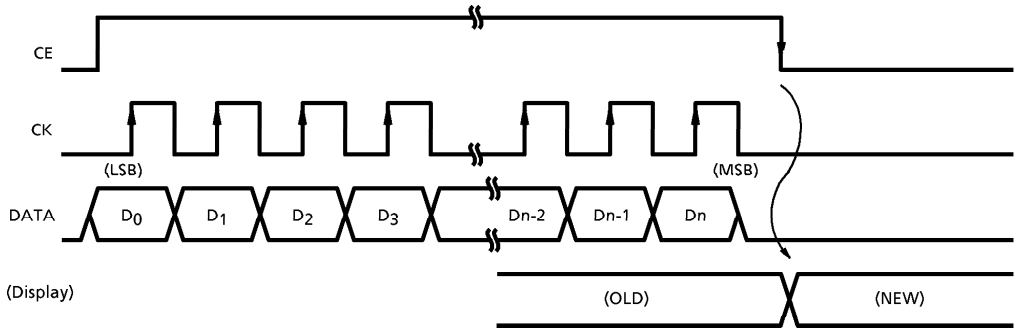
PIN No.	SYMBOL	PIN NAME	DESCRIPTION	REMARKS
73	V_{DD}	Power Supply Pin	Power Supply Pin (5V±0.5V)	—
77	GND	GND Pin		
1 ≀ 62	SEG0 ≀ SEG61	Segment Output Pin	LCD segment drive output pins 1/2 or 1/3 duty 1/2 or 1/3 bias } can be switched.	
72	$\overline{BL}$	Blanking Input Pin	All segments are put in the blanking state when "L" level signal is input.	
71	$\overline{LT}$	Lamp Test Input Pin	All segments light when "L" level signal is input.	

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	REMARKS
65	CE	Chip Select Input Pin	Display data input pins Input data becomes valid only when CE = "H". Display data is input synchronizing with rise of CK clock. When CE = "H" changes to CE = "L", data is latched and display is updated.	
66	DATA	Data Input Pin		
67	CK	Clock Input Pin		
68	OSC	Oscillation Pin	This pin serves as an oscillator when a capacitor and a resistor are connected externally. In the slave mode, COM-OUT output from the master IC is input to this pin.	
69	SEL	Master / Slave Switching Pin	Master / slave switching input when more than 2 pieces of this IC are used simultaneously. "H" = Master Mode "L" = Slave Mode	
64	$\overline{SYNC}$	Synchronous Pin	Synchronizing input / output pin when more than 2 pieces of this IC are used simultaneously. Master Mode : Synchronous output Slave Mode : Synchronous input	
70	2 / 3	Duty Switching Pin	1 / 2 or 1 / 3 duty switching input "H" = 1 / 2 duty mode "L" = 1 / 3 duty mode	
74	V_{LC1}	Bias Input Pin	LCD drive voltage input pins Set input voltage to $V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq GND$	—
75	V_{LC2}			
76	V_{LC3}			
78	COM1	Common Output Pin	Common pin drive output In the 1 / 2 duty mode, COM3 pin is used in the open state.	
79	COM2			
80	COM3			
63	COM-OUT	Common Clock Output Pin	Synchronizing clock output pin Supplies clock to the OSC pin of the slave IC. $f_{COM} = f_{OSC} / 4$[Hz]	

DESCRIPTION OF OPERATION

1. Data Input Format

- Display data are input at the following timings:



(Display)

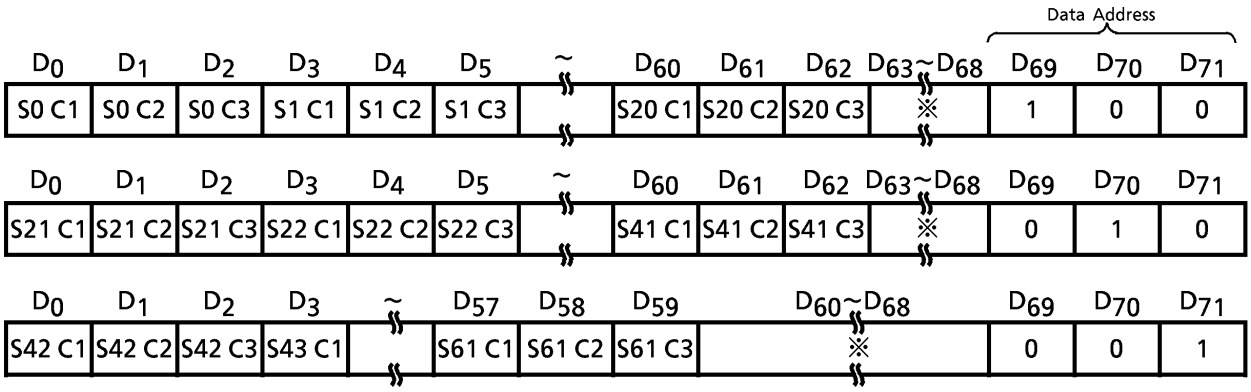
- For data length, 48 bits (D0~D47) are transferred 3 times in the 1/2 duty mode and 72 bits (D0~D71) 3 times in the 1/3 duty mode
- 3 bits (last 3 bits) from MSB side of data are address data.
  (D45~D47 in the 1/2 duty mode, while D69~D71 in the 1/3 duty mode.)
- Data in the 1/2 duty mode (2/3 = "H")

  COM1 system data : $D_0, D_2, D_4 \cdots (D_0 + 2n)$
  COM2 system data : $D_1, D_3, D_5 \cdots (D_1 + 2n)$
  } n = 0~61
  Address data : "100" = SEG0~SEG20
  "010" = SEG21~SEG41
  "001" = SEG42~SEG61

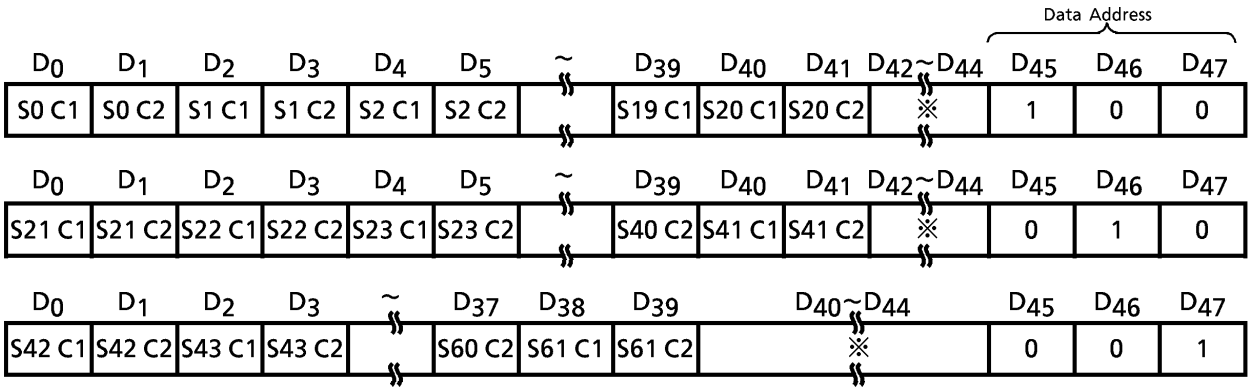
- Data in the 1/3 duty mode (2/3 = "L")

  COM1 system data : $D_0, D_3, D_6 \cdots (D_0 + 3n)$
  COM2 system data : $D_1, D_4, D_7 \cdots (D_1 + 3n)$
  COM3 system data : $D_2, D_5, D_8 \cdots (D_2 + 3n)$
  } n = 0~61
  Address data : "100" = SEG0~SEG20
  "010" = SEG21~SEG41
  "001" = SEG42~SEG61

1) Data Format at 1/3 Duty (186 Segment)



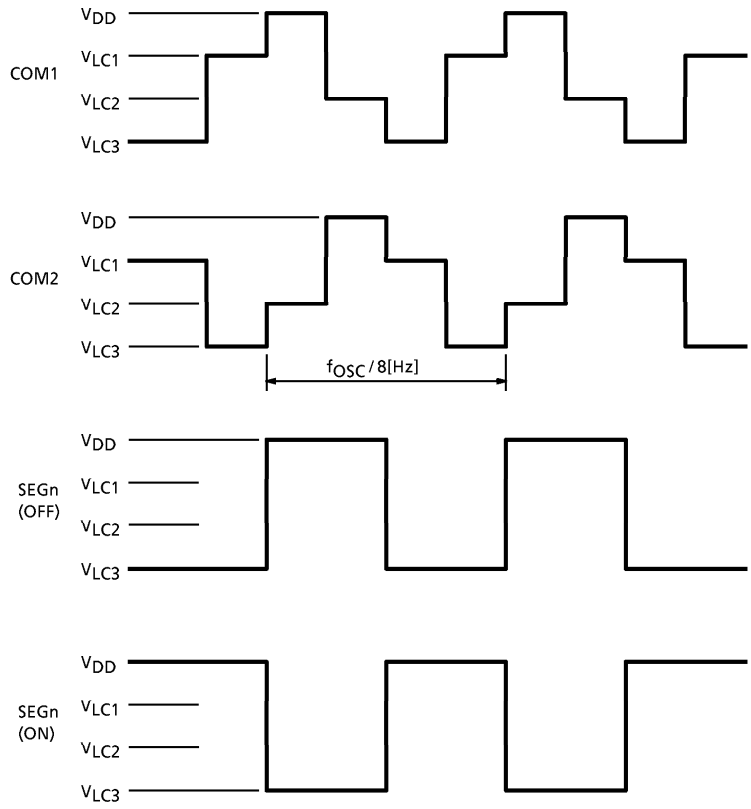
2) Data Format at 1/2 Duty (124 Segment)



Note) ※ : 1 or 0

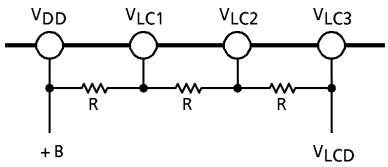
2. LCD Display Timings

1) 1 / 2 Duty Mode (2 / 3 = "H")

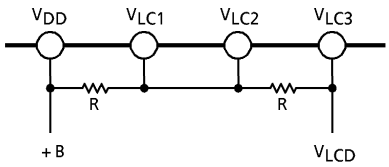


(Note) When used in the 1 / 2 bias, supply bias by connecting V_{LC2} pin and V_{LC3} pin. (This also applies to the 1 / 3 duty mode.)

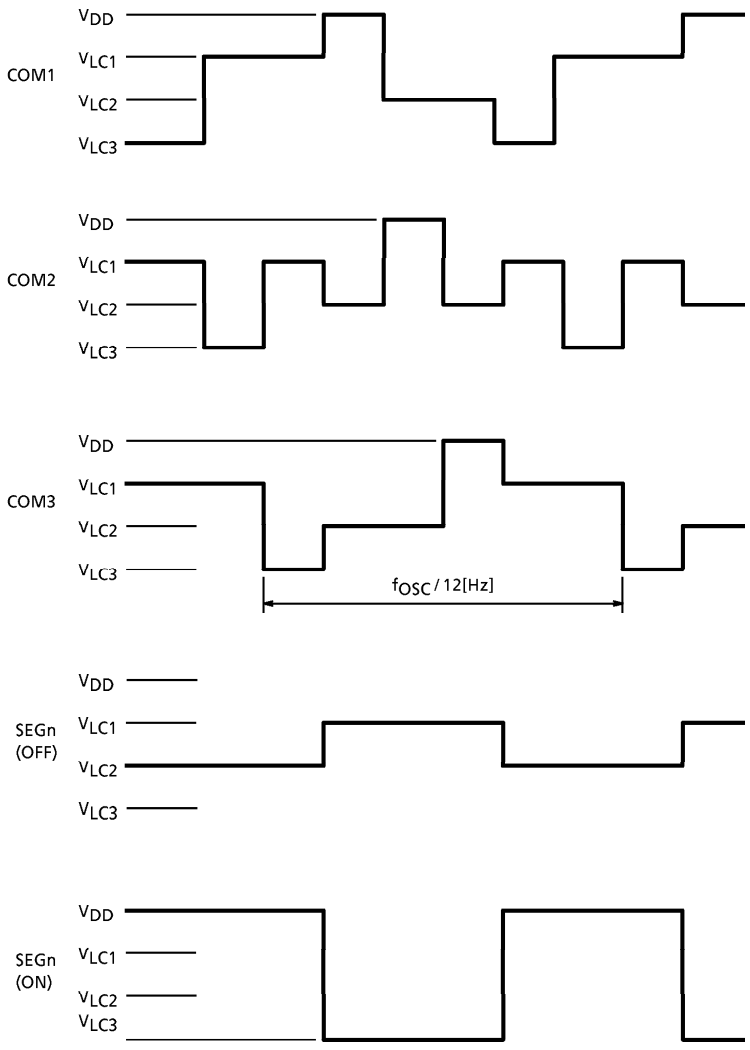
- 1 / 3 Bias Operation



- 1 / 2 Bias Operation



2) 1 / 3 Duty Mode (2 / 3 = "L")



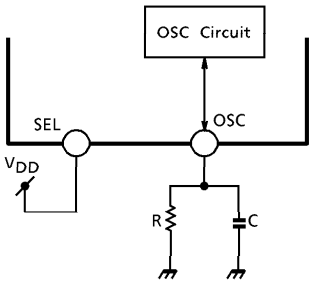
3. Oscillation Circuit

When a resistor and a capacitor are connected to the OSC pin and oscillation circuit is composed and common signal is generated. 1 / 4 division of oscillation frequency becomes common frequency. Capacitor (C) and resistor (R) are connected as shown in the right-side figure and the oscillation frequency is expressed by the following expression :

$f_{OSC} \approx 1.44 / C \cdot R$ (Ta = 25°C, V_{DD} = 5V)

For instance, when C = 0.012μF, and R = 150kΩ, f_{OSC} will be about 800Hz and common frequency will be 200Hz. Use the external resistor at 12~220kΩ.

However, there is no restriction for the external capacitor C.



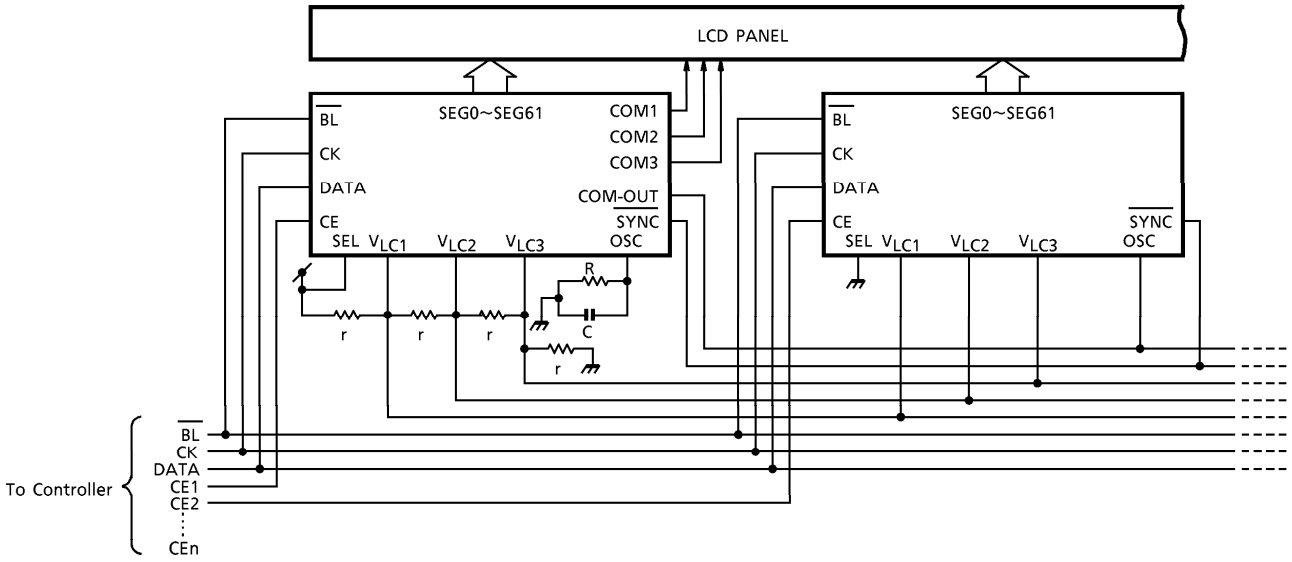
4. In Case of Using More Than 2

When more than 2 TC9240F are used simultaneously, common frequency is generated using one IC in the master mode. As a result, the slave mode IC performs the simultaneous operation.

1) Processing of Pins at Simultaneous Operation

PIN NAME	PIN No.	MASTER MODE IN	SLAVE MODE IC
SEL	68	"H" (V_{DD}) Level	"L" (GND) Level
OSC	75	Connect External C&R	Connect to Master IC : COM-OUT
$\overline{SYNC}$	64	Generate SYNC Output	Connect to Master IC : $\overline{SYNC}$
COM-OUT	63	Connect to Slave IC : OSC	Open (unused)
COM1	78	Connect to COM Pin of LCD	Open (unused)
COM2	79		
COM3	80		

2) Example of Application Circuit Synchronizing Operation



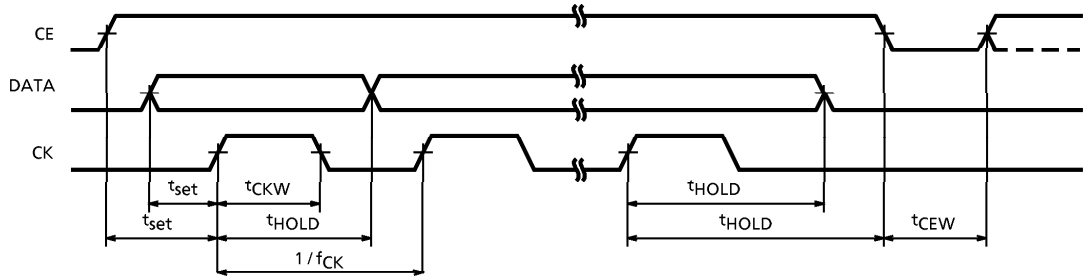
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 4.5~5.5V, Ta = −40~85°C)

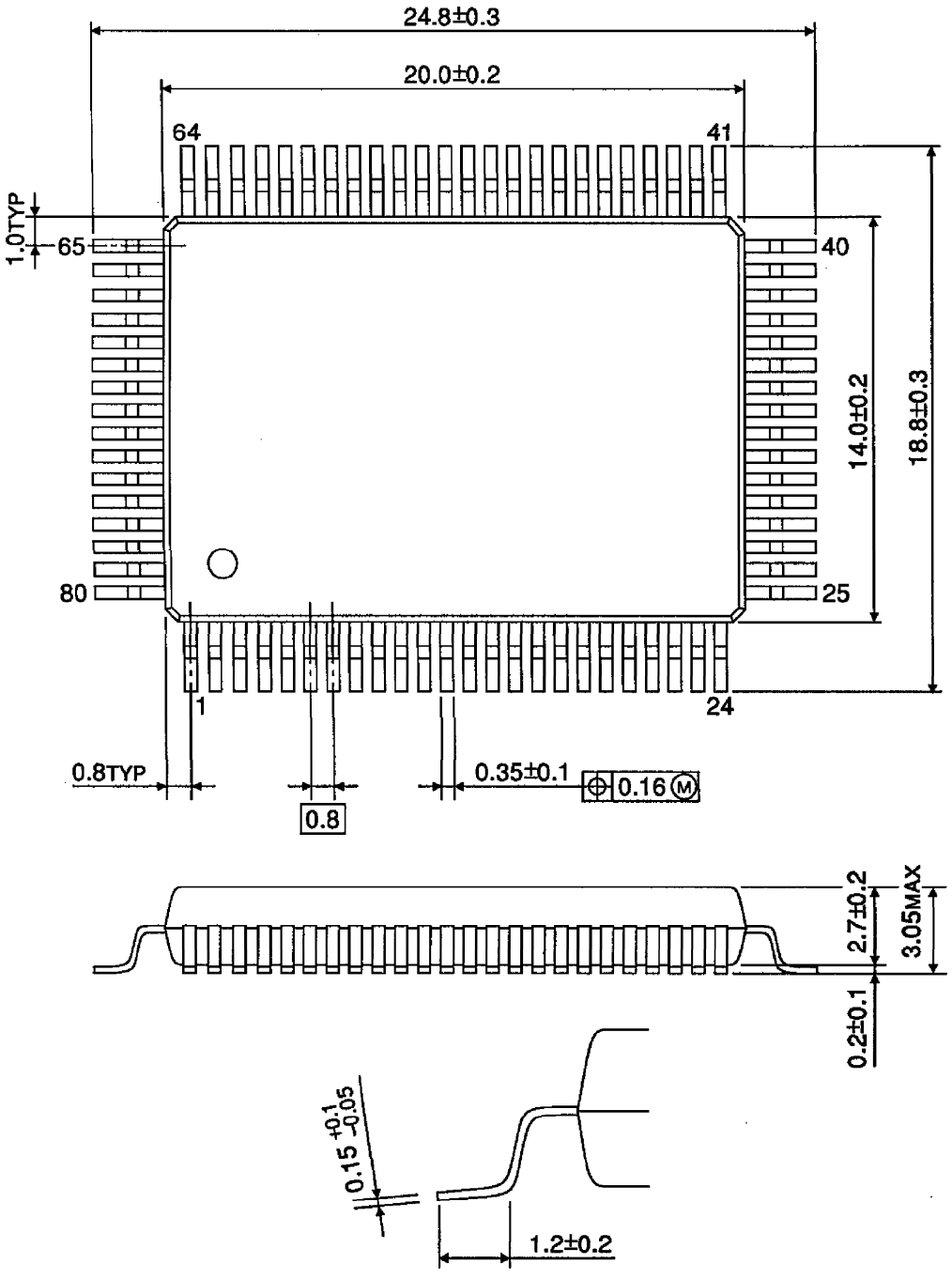
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	—		4.5	5.0	5.5	V
Operating Supply Current		I_{DD}	—	f_{OSC} = 1.2kHz, No load, V_{DD} = 5V		—	0.3	1.0	mA
Input Voltage	"H" Level	V_{IH}	—	All input pins		V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL}				GND	~	V_{DD} × 0.3	
Input Current	"H" Level	I_{IH}	—	CMOS input pins, V_{DD} = 5V	$V_{IH} = V_{DD}$	−2	—	2	μA
	"L" Level	I_{IL}			V_{IL} = GND	−2	—	2	
Pull-up Resistance		R_{UP}	—	$\overline{BL}$, $\overline{LT}$ pins, V_{DD} = 5V, Ta = 25°C		50	100	200	kΩ
Output Resistance	Segment	R_{seg}	—	SEG0~SEG61 Output pins	$V_{LC1} = V_{LC2}$ = 1/2V_{DD}	—	0.6	3.0	kΩ
	Common	R_{COM}		COM1~COM3 Output pins	V_{LC3} = GND, V_{DD} = 5V	—	0.5	3.0	
Output Current	"H" Level	I_{OH}	—	$\overline{SYNC}$, COM-OUT Output pins, V_{DD} = 5V	V_{OH} = 4.5V	−0.2	−0.8	—	mA
	"L" Level	I_{OL}			V_{OL} = 0.5V	0.2	1.0	—	
Oscillation Frequency		f_{OSC}	—	OSC Pin Operation Frequency		—	1.2	50	kHz
Max. Clock Frequency		f_{CK}	—	Refer to the timing chart as below.		0	~	2.0	MHz
Clock Pulse Width		t_{CKW}				250	—	—	ns
Data Set Time		t_{set}				250	—	—	
Data Hold Time		t_{HOLD}				250	—	—	
CE Pulse Width		t_{CEW}				250	—	—	

CE, CK, DATA TIMING



OUTLINE DRAWING

QFP80-P-1420-0.80A Unit : mm



Weight : 1.57g (Typ.)