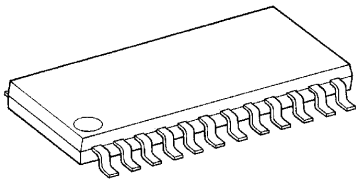
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9293F, TC9293FN, TC9293N

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH ANALOG FILTER

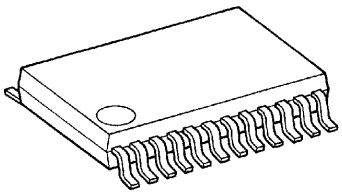
TC9293F, TC9293FN, TC9293N are a 2'nd order Σ-Δ modulation system 1bit DA converter with a built-in 8 times over sampling digital filter and analog filter developing for digital audio equipment. As this IC is small package, SSOP24 (1.00mm, 0.65mm) and SDIP24, and the analog filter has been incorporated, it is able to output a direct analog wave form and construct small the digital filter~the analog output unit at a low price.

TC9293F



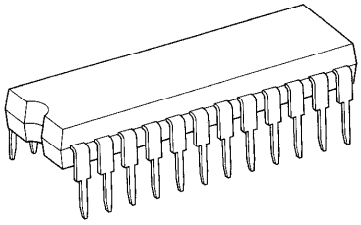
SSOP24-P-300-1.00

TC9293FN



SSOP24-P-300-0.65A

TC9293N



SDIP24-P-300-1.78

Weight
SSOP24-P-300-1.00 : 0.31g (Typ.)
SSOP24-P-300-0.65A : 0.14g (Typ.)
SDIP24-P-300-1.78 : 1.2g (Typ.)

FEATURES

- Built in 8 times over sampling digital filter
- Low voltage operate (3.0~5.5V)
- Built-in digital de-emphasis filter
- In serial control mode, output amplitude can be set in 128steps of resolution using microcontroller command
- In parallel control mode, soft mute can be set for the output signal in 64steps in 20ms
- Over sampling ratio (OSR) of Σ-Δ modulation circuit is 192fs
- Support double speed operation
- Sampling frequency : 32kHz, 44.1kHz, 48kHz
- Built-in 2'nd order analog filter
- Characteristics of the digital filter and DA converter are as follows :

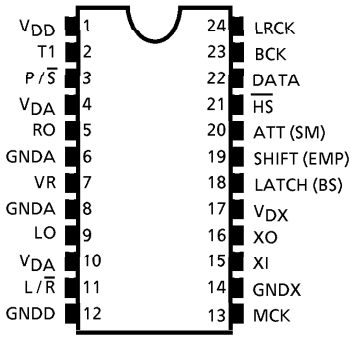
DIGITAL FILTER (fs = 44.1kHz)

	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP BAND SUPPRESSION
Standard Operation	8fs	±0.11dB	20k~24.1kHz	– 26dB
Double Speed Operation	8fs	±0.11dB	20k~24.1kHz	– 26dB

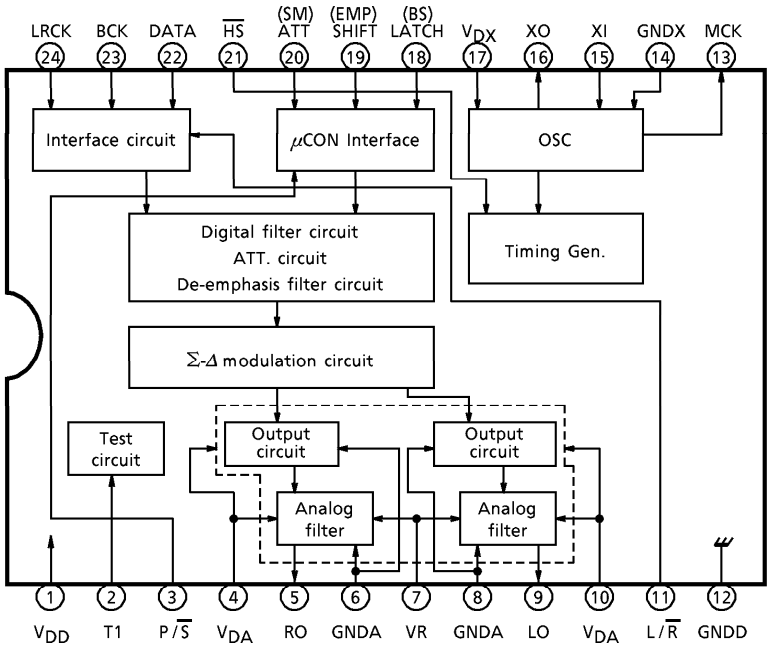
DA CONVERTER (V_{DD} = 5V)

	OSR	NOISE DISTORTION	S / N
Standard Operation	192fs	– 85dB (Typ.)	96dB (Typ.)
Double Speed Operation	96fs	– 85dB (Typ.)	86dB (Typ.)

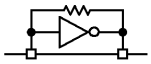
PIN CONNECTION



BLOCK DIAGRAM



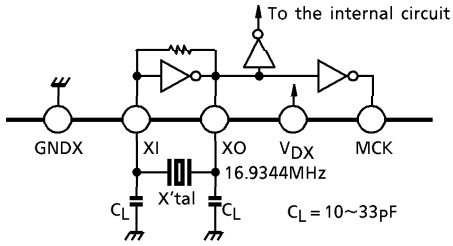
PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
1	V_{DD}	—	Digital block power supply pin.	
2	T1	I	Test pin. Normally, use at "L".	
3	P / $\overline{S}$	I	Parallel / serial mode select pin.	
4	V_{DA}	—	Analog power supply pin.	
5	RO	O	R-ch analog output pin.	
6	GNDA	—	Analog ground pin.	
7	VR	—	Reference voltage pin.	
8	GNDA	—	Analog ground pin.	
9	LO	O	L-ch analog output pin.	
10	V_{DA}	—	Analog power supply pin.	
11	L / $\overline{R}$	I	LRCK polarity switching pin.	
12	GNDD	—	Digital ground pin.	
13	MCK	O	System clock output pin.	
14	GNDX	—	Crystal oscillator ground pin.	
15	XI	I	Crystal oscillator connection pin.	
16	XO	O	Generate the clock required by the system.	
17	V_{DX}	—	Crystal oscillator power supply pin.	
18	LATCH (BS)	I	Serial mode : Data latch signal input pin. Parallel mode : De-emphasis filter mode select pin.	SHUMITT INPUT
19	SHIFT (EMP)	I	Serial mode : Shift clock input pin. Parallel mode : De-emphasis filter control pin.	SHUMITT INPUT
20	ATT (SM)	I	Serial mode : Data input pin. Parallel mode : Soft mute control pin.	SHUMITT INPUT
21	$\overline{HS}$	I	Standard / double speed operation control pin. Standard operation at "H", double speed operation at "L".	
22	DATA	I	Audio data input pin.	
23	BCK	I	Bit clock input pin.	
24	LRCK	I	LR clock input pin.	

DESCRIPTION OF BLOCK OPERATION

1. Crystal oscillation circuit and timing generator

   Clock required for internal operation can be generated when crystal and capacitors are connected as shown in the following figure.
   Further, this converter is also operable when system clock is input from the outside through XI pin (pin⑮).
   However, a through consideration is required in this case because noise distortion and S/N ratio of the DA converter are largely affected by qualities of wave form such as jitter, rising and falling characteristics, etc. of system clock.



Use a crystal having a low CI value and good statability.

Fig.1 Configuration of crystal oscillation circuit.

   The timing generator generates clock required for the digital filter, de-emphasis filter, interpolation filter and process timing signal.

2. Data input circuit

   DATA and LRCK are taken in the shift register in the LSI at the rising edge of BCK.
   As shown in the following timing example, it is therefore necessary to input DATA and LRCK in synchronism with the falling edge of BCK.
   Further, because DATA has been to designed that 16 bits before the change point of LRCK are made effective data.

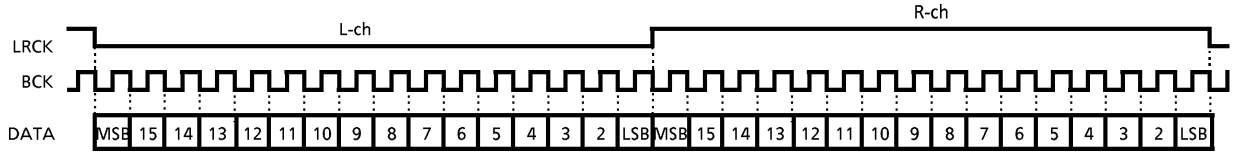


Fig.2a Example of input timing diagram ($L/\overline{R}$ = "L")

If BCK is 48fs or 64fs, please input data as follows.

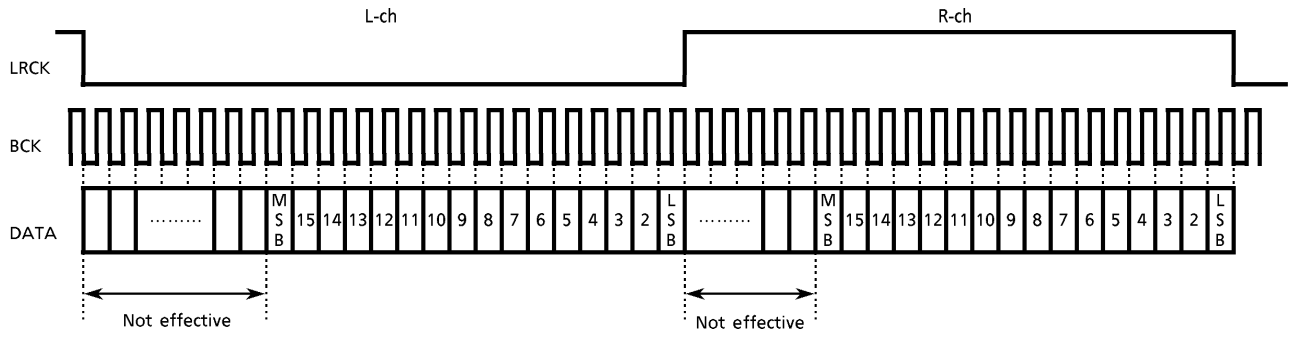


Fig.2b Example of input timing diagram (L/$\overline{R}$ = "L")

L/R channel data selection pin is pin⑪.

Table-1 Channel data

L/$\overline{R}$ INPUT	LRCK	
	L	H
H	R-ch data	L-ch data
L	L-ch data	R-ch data

3. Digital filter

Foldover noise component of the outside band is removed by the 8 times oversampling digital filter.

Table-2 Characteristics of the digital filter

	Pass-band Ripple	Transient Bandwidth	Stop-Band Suppression
Standard Operation	±0.11dB	20.0k~24.1kHz	−26dB
Double Speed Operation	±0.11dB	20.0k~24.1kHz	−26dB

Frequency characteristics of the digital filter are as follows : (Double speed operation is same)

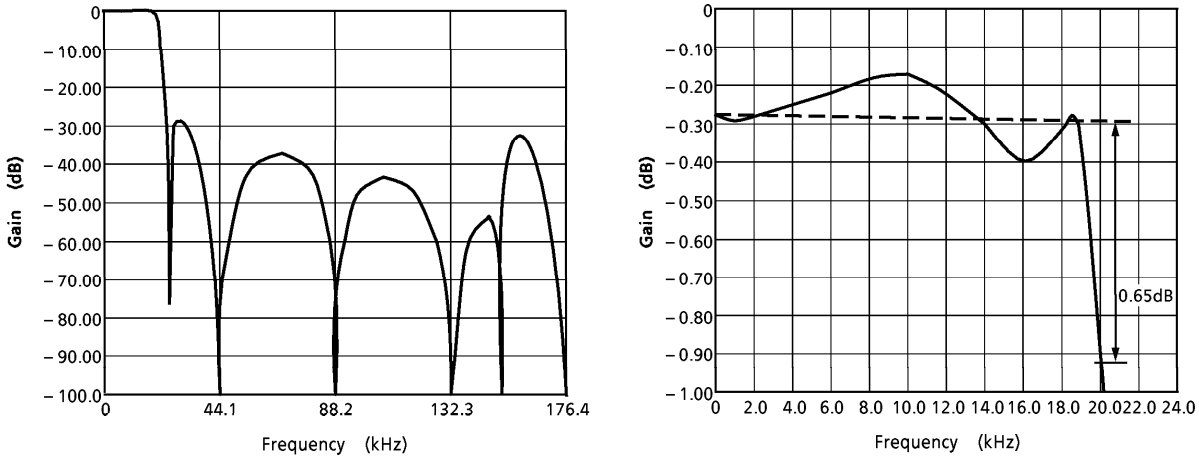


Fig.3 Digital filter frequency characteristics (fs = 44.1kHz)

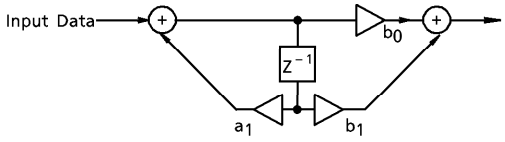
4. De-emphasis filter

The built-in digital de-emphasis circuit is available for three kinds of sampling frequency, fs of 32kHz, 44.1kHz, and 48kHz. The selection is done as shown in the following table.

Table-3 Truth table for de-emphasis filter selection at parallel mode

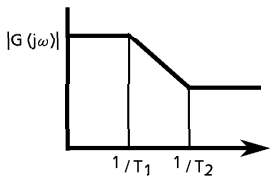
LATCH (BS)	H	H	L	L	
SHIFT (EMP)	H	L	H	L	
MODE (fs SELECT)	32	48	44.1	OFF	(kHz)

Digitization of the de-emphasis filter has eliminated the necessity for external parts such as resistor, capacitor, analog switch, etc.
Further, to reduce the characteristic error of the de-emphasis filter, coefficients have been adjusted. The construction and characteristics of the de-emphasis filter are shown below.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 Construction of IIR type digital de-emphasis filter

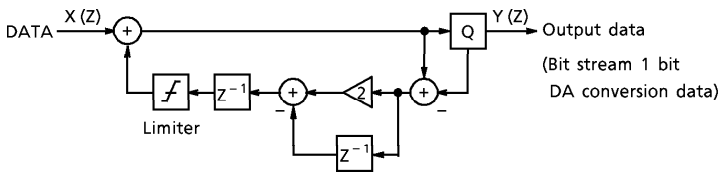


$T_1 = 50\mu s$, $T_2 = 15\mu s$

Fig.5 Filter characteristic

5. DA conversion circuit

The 2'nd order Σ-Δ modulation system DA converter for 2 channels (simultaneous output type) has been incorporated.



2'nd order Σ-Δ modulator : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.6 Construction of Σ-Δ modulation DA converter

It has been designed that clock for the Σ-Δ modulator is a half of master clock (MCK : Crystal oscillation clock) and the converter operates at 192fs at the standard operation.
The noise shaping characteristic is shown below.

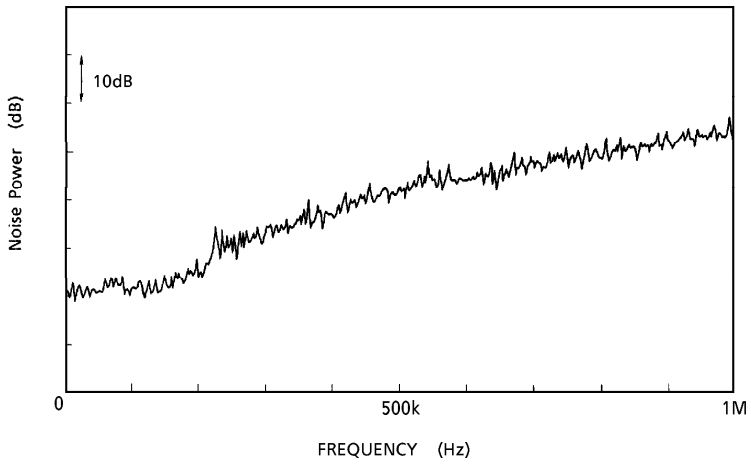


Fig.7 Noise shaping characteristic

6. Output circuit

These ICs is built-in 2'nd order analog low pass filter.
These output is analog signal directly, RQ (pin⑤) and LO (pin⑨) pins.

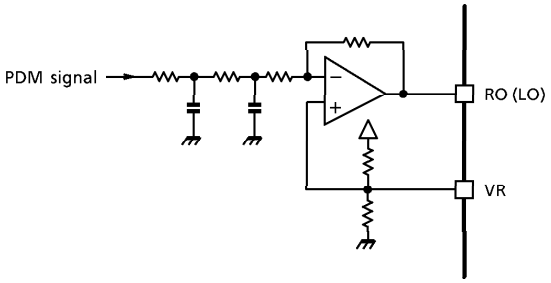


Fig.8 Analog filter circuit

7. Soft mute circuit

This IC is a built-in soft mute circuit, it is possible to do soft mute, when SM pin is changed "L" level to "H" level during parallel mode.
Characteristic of soft mute ON / OFF and DA converter output level is as follows.
While output level is changing, it is not possible to accept soft mute ON / OFF control.

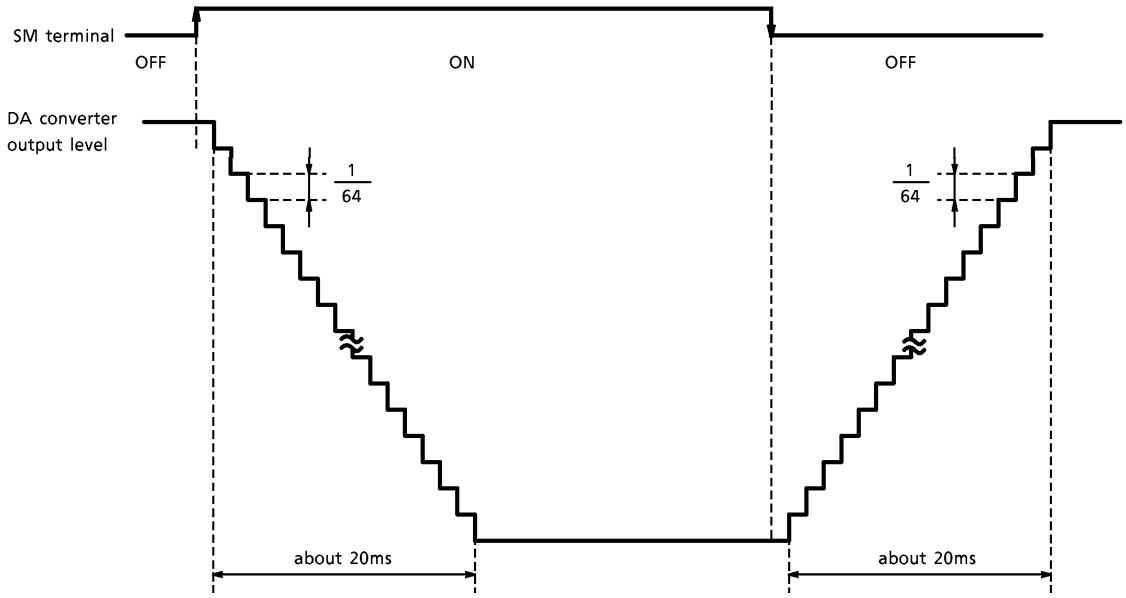


Fig.9 Soft mute DA converter output level

8. Description of internal control signal

Parallel and serial modes can be selected by the P/$\overline{S}$ pin. The controll functions are described as follow.

8-1 Parallel mode (P/$\overline{S}$ pin = "H")

In parallel mode, pin⑱, ⑲, ⑳ are set as follows.

Table-4 Pin names at parallel mode

PIN No.	PIN NAME	FUNCTION
18	BS	De-emphasis filter mode select pin.
19	EMP	De-emphasis filter control pin.
20	SM	Soft mute control pin.

8-2 Serial mode (P/$\overline{S}$ pin = "L" : For micro processor control use)

In serial mode, these ICs can be controlled by micro processor. The control function of pin⑱, ⑲, ⑳ are as follows.

Table-5 Pin names at serial mode

PIN No.	PIN NAME	FUNCTION
18	LATCH	Data latch signal input pin
19	SHIFT	Shift clock signal input pin
20	ATT	Data input pin

LATCH and ATT signals are entered to the shift register of the LSI at the rising edge of SHIFT signal.
Also, LATCH signal should rise after a minimum of 1.5μs of the last data is shifted to the register. If the shift pulse is changed while LATCH is Low, Mis-operation may occur. LATCH should be set at Low level until after D7 is shifted into the register.

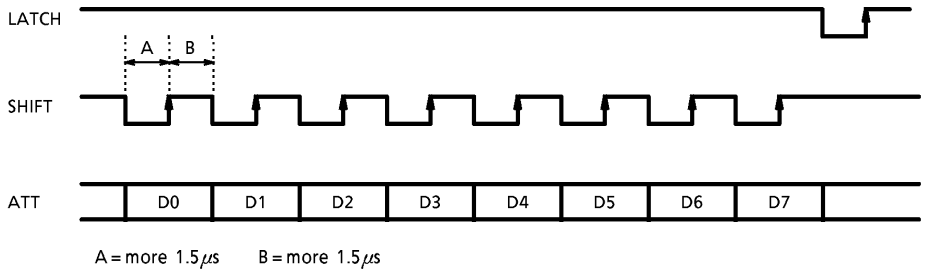


Fig.10 Example for serial control mode data

In serial control mode, the control features are as follows.
When this IC's power is ON, all these data must be setting.

Table-6 Serial mode control

SERIAL INPUT DATA	CONTROL SIGNAL	
D7	0	1
D6	AT6	μBS
D5	AT5	μEMP
D4	AT4	—
D3	AT3	—
D2	AT2	—
D1	AT1	—
D0	AT0	—

AT0~6 : Attenuation level setting
μBS : De-emphasis mode select
EMP : De-emphasis ON / OF select

① Digital attenuator

D7 = "L" is the command for digital attenuator. It can be set to 128 levels as show below.

Table-7 Audio output of attenuation data

ATTENUATION CONTROL DATA D6~D0	AUDIO OUTPUT
7F (HEX)	0dB
7E (HEX)	– 0.069dB
⋮	⋮
01 (HEX)	– 42.076dB
00 (HEX)	– ∞

The attenuation value can be calculated from input data as follow :

ATT = 20ℓog (input data / 127)dB

Example : In case of attenuator = 7A

ATT = 20ℓog (122 / 127)dB = – 0.349dB

② Digital De-emphasis filter

D7 = "H" is the command for Digital De-emphasis filter.

Table-8 De-emphasis filter setting

μBS	H	H	L	L
μEMP	H	L	H	L
MODE	32	48	44.1	OFF

(kHz)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~6.0	V
		V_{DA}	−0.3~6.0	
		V_{DX}	−0.3~6.0	
Input Voltage		V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9293F	P_D	200	mW
	TC9293FN		200	
	TC9293N		300	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DA} = 5V$)

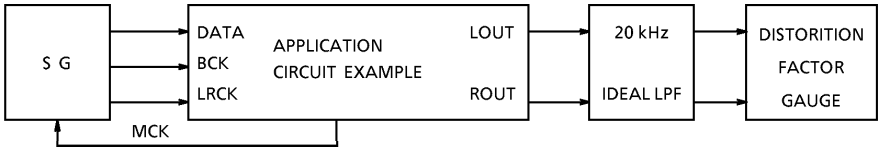
DC item

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Operating Supply Voltage (2)		V_{DD}	—	Ta = −15~55°C (Operation frequency 12MHz ≦ f_{opr} ≦ 18.5MHz)	3.0	3.2	5.5	V
		V_{DX}			3.0	3.2	5.5	
		V_{DA}			3.0	3.2	5.5	
Power Dissipation		I_{DD}	—	XI = 16.9MHz	—	12	20	mA
Input Voltage	"H" Level	V_{IH}	—		$V_{DD} \times 0.7$	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	$V_{DD} \times 0.3$	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC item (Over-sampling ratio = 192fs)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Table Harmonic Distortion + Noise 1	THD + N1	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	−85	−80	dB
Table Harmonic Distortion + Noise 2	THD + N2	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	−85	−78	dB
S / N Ratio	S / N	1		88	96	—	dB
Dynamic Range	DR	1	1kHz Sine wave, −60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1kHz Sine wave, full-scale input	—	−95	−90	dB
Analog Output Level	Aout 1	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	1250	—	mVrms
	Aout 2		1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	750	—	
Operating Frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5V$	10	16.9344	19.2	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	2.1168	4.3	MHz
Rise Time	t_r	—	LRCK, BCK (10%~90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCK ↓ Edge → LRCK, DATA	—	—	40	ns

- **TEST CIRCUIT 1** : Application circuit example is used.

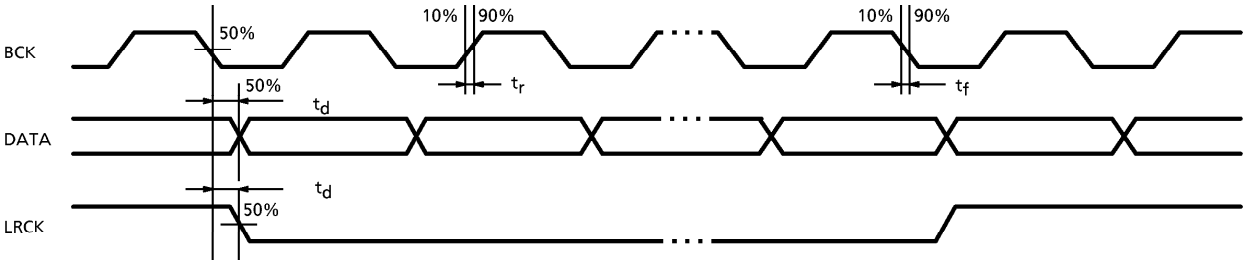


SG : ANRITSU MG-22A or equivalent
LPF : SHIBASOKU 725C built-in Filter
Distortion Factor Gauge : SHIBASOKU 725C or equivalent

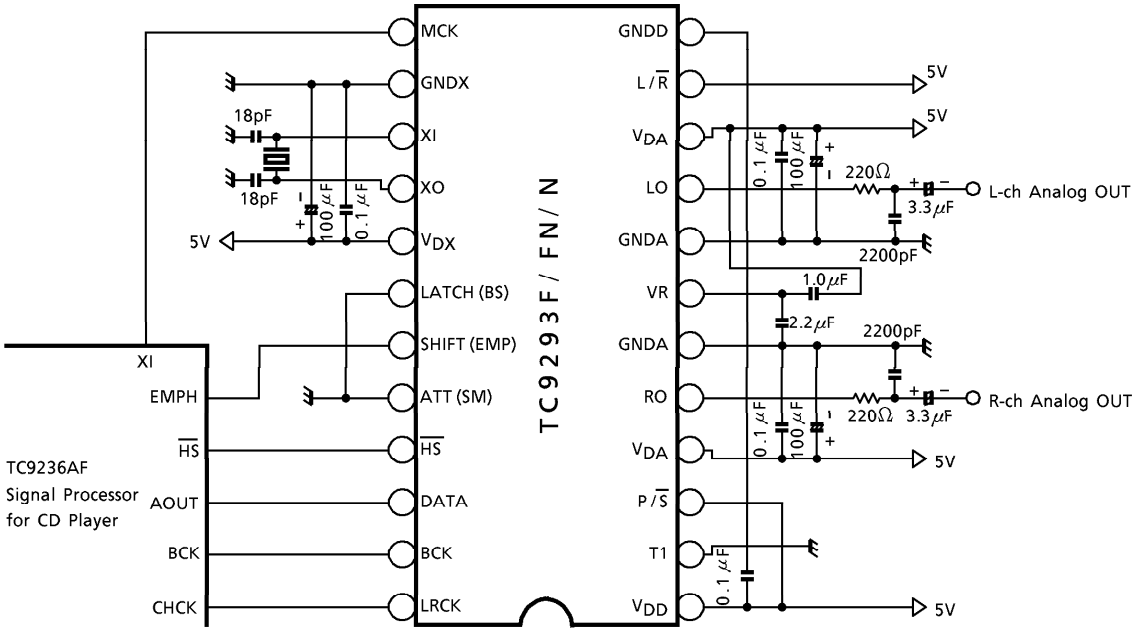
Measuring Item	Distortion factor gauge filter setting A weight
THD + N, CT	OFF
S / N, DR	ON

A weight : IEC-A or equivalent

- **AC CHARACTERISTIC POINT** (Input signal : LRCK, BCK, DATA)

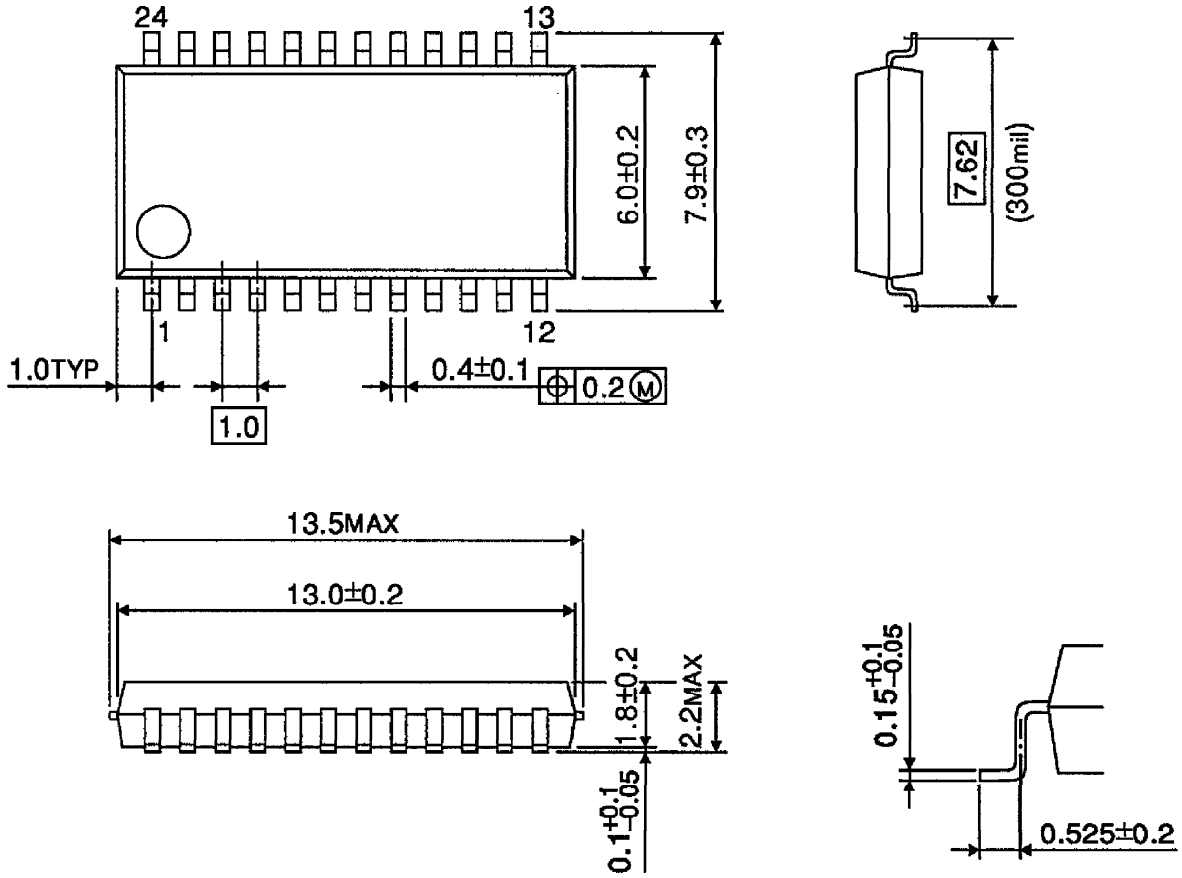


APPLICATION CIRCUIT



PACKAGE DIMENSIONS

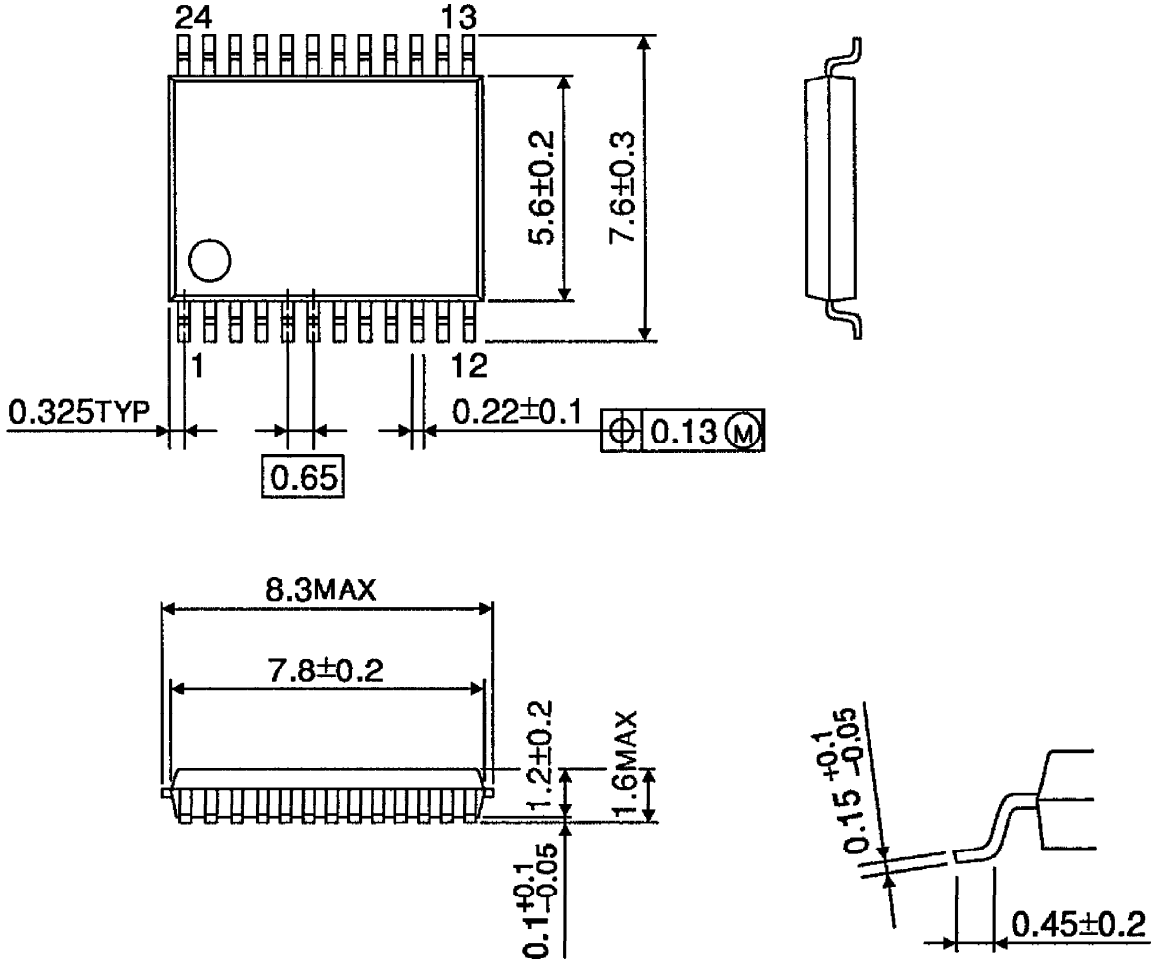
SSOP24-P-300-1.00 Unit : mm



Weight : 0.31g (Typ.)

PACKAGE DIMENSIONS

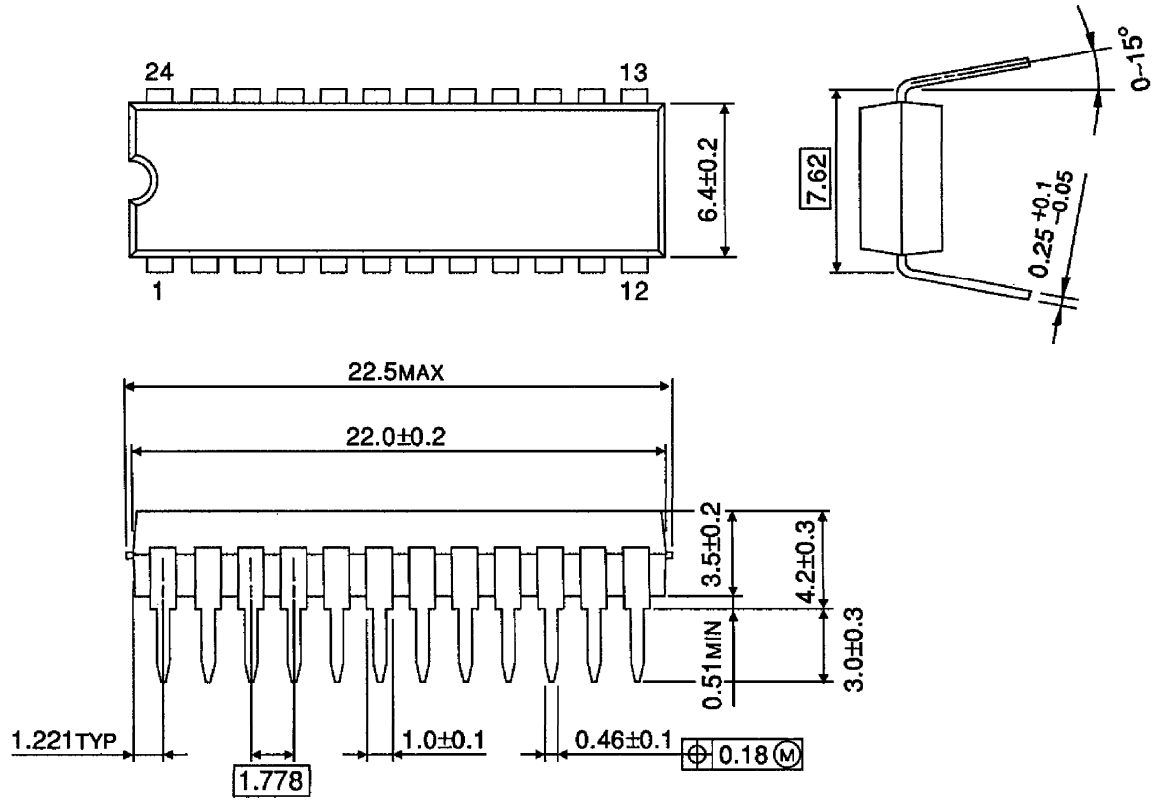
SSOP24-P-300-0.65A Unit : mm



Weight : 0.14g (Typ.)

PACKAGE DIMENSIONS

SDIP24-P-300-1.78 Unit : mm



Weight : 1.2g (Typ.)

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000707EBA

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