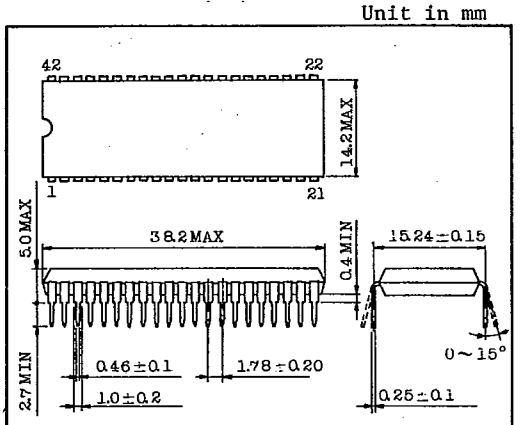
TC9301AN

T-49-19-57

DTS MICRO CONTROLLER CONTAINING HIGH VOLTAGE VACUUM FLUORESCENT INDICATION TUBE DRIVER

TC9301AN is 4-bit CMOS micro controller for digital tuning system use having built-in high voltage driver able to directly drive vacuum fluorescent indication tube.
CPU has 4-bit parallel adittion and subtractions (AI, SI instructions, etc.), logical operations (OR, AN instructions, etc.), plural bit judge and comparison instructions (TM, SL instructions, etc.) and time base function.
The equipment consists of shrink type DIP 42-pin and has abundant I/O ports and exclusive key input ports controlled by powerful input and output instruction (IO, KEY instructions, etc.), serial bus control function (SIO instruction) to control forcibly external PLL LSI and peripheral ICs.
Moreover, it has exclusive output terminals of 7-digit, 8-segment dynamic display type VFL indication tube driver and exclusive terminal for outputting eight kinds of reference frequency signal to be supplied to PLL LSI.
And TC9301AN is pin-compatible with TC9303AN (program memory capacity, 1K-step type).

Unit in mm



Lead pitch is 1.78 and tolerance is ±0.20 against theoretical center of each lead that is obtained on the basis of No.1 and No.42 leads.

JEDEC	—
TOSHIBA	6D42B-P

Weight : 4.0g

FEATURES:

- 4-bit micro controller for digital tuning system use.
- Built-in VFL indication tube driving circuit of dynamic display type.
- 5V±10% single power supply. CMOS structure and low power dissipation.
- Backup of data memory (RAM) and each port is easily made (by $\overline{INH}$ terminal).
- Program memory (ROM) : 16 bits X 2048 steps
- Data memory (RAM) : 4 bits X 128 words
- Powerful instruction sets of 62 kinds (all one-word instructions).
- Basic instruction executing time 44.4μs (7.2MHz crystal connection).
- Abundant addition and subtraction instructions (addition instructions 12 kinds, subtraction instructions 12 kinds).
- Powerful compound judge instruction (TMTR, TMFR, TMT, TMF instruction).

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- Data transfer in the same row address is possible.
- Indirect transfer of register is possible (MVRD, MVRS, MVGD, MVGS instructions).
- 16 powerful general registers (arranged in RAM).
- Stack level : 1 level
- Program memory (ROM) has no conception of page or field, and JUMP and CAL instructions can be freely made within 2048 steps.
- It is possible to freely refer to the contents, 16 bits, of optional address within 1024 steps in program memory (ROM) (DAL instruction).
- Built-in powerful exclusive serial bus control function.
- Powerful input and output instructions (6 kinds of instructions: IO, KEY, SIO, etc.).
- Exclusive terminal is provided for display and key input (7-digit, 8-segment dynamic display type).
- Direct drive of VFL indication tube is possible by both digit and segment.
- Built-in P-ch high breakdown voltage FET and load resistor (withstand voltage 32V MAX.) in both digits (D_0~D_6) and segments (a~h).
- Abundant 10 I/O ports (ports capable of input/output setting in 1-bit unit: 9, exclusive output port: 1).
- Clock stop is possible by instruction (during CKSTP instruction: supply current, 1μA or below).
- 2Hz timer F/F and 10Hz interval pulse output are contained (internal port for time base use).
- Reference frequencies of eight kinds to be supplied to PLL LSI can be selected with program (1kHz, 5kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 50kHz or 100kHz).
- Pin compatible with TC9303AN (ROM capacity: 16-bit X 1024 steps).

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3~6.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	800	mW
Operation Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~125	°C
Open Drain Output Breakdown Voltage	V_{BDS}	35 (Voltage between drain and source)	V
Key Input Voltage	V_{INK}	-V_{FL}-0.3~V_{DD}+0.3	V

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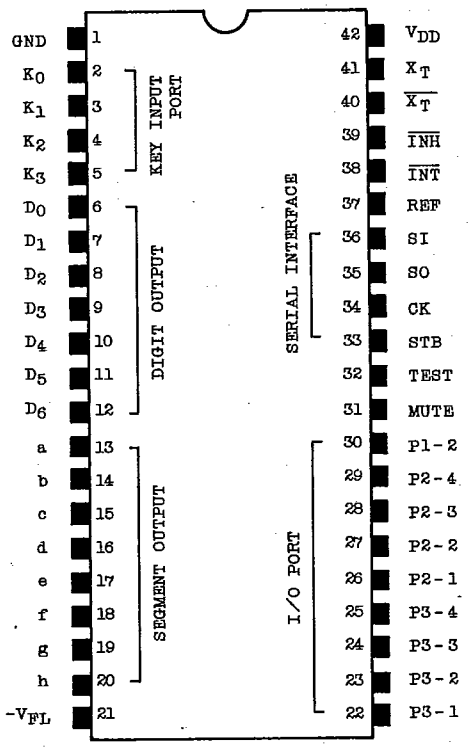
TERMINAL CONNECTION DIAGRAM



TOP VIEW SHRINK DIP-42 PIN

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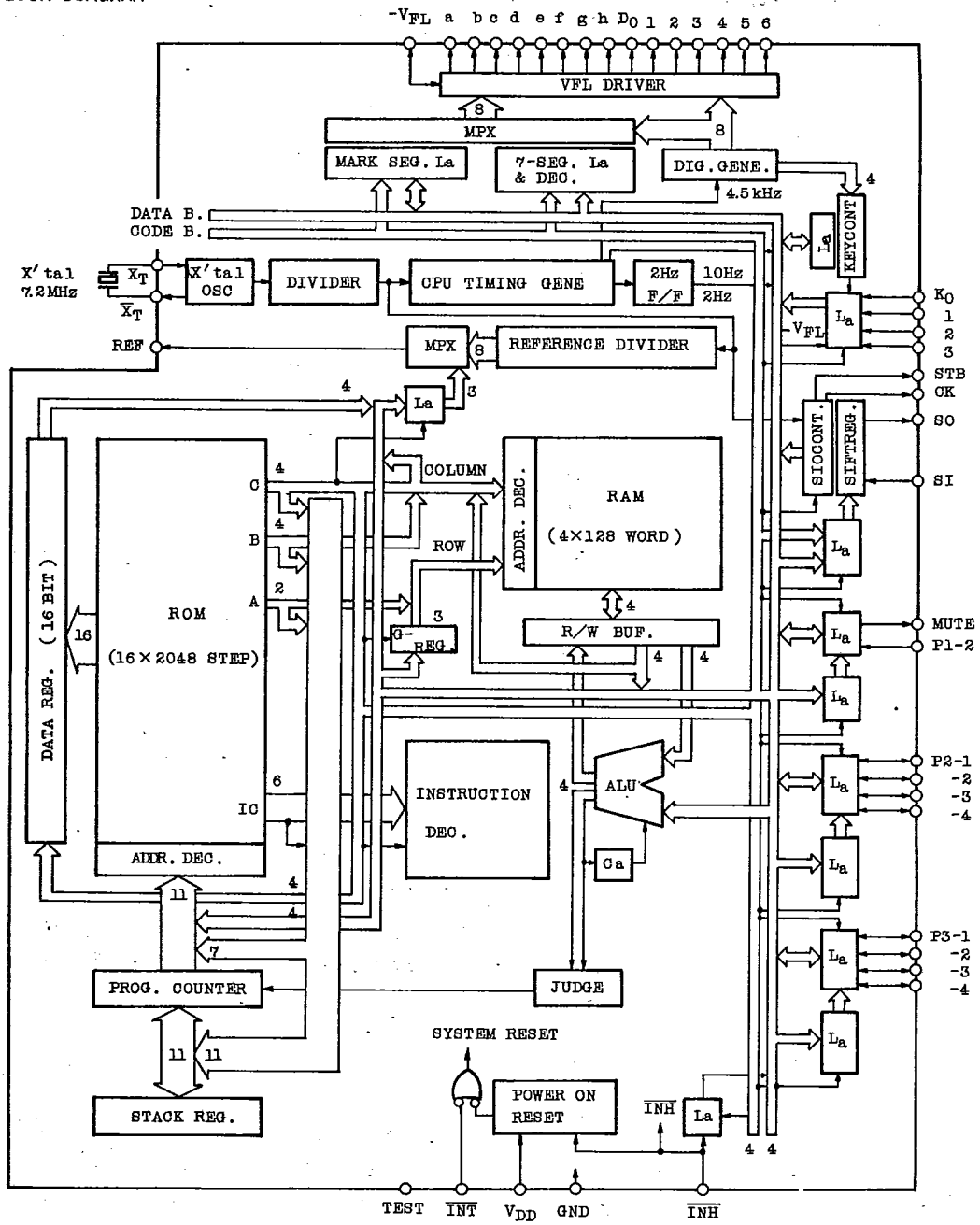
BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage Range	V_{DD}	*	4.5	5.0	5.5	V
Memory Holding Voltage Range	V_{HD}	Crystal oscillation stops*	2.0	~	5.5	V
$-V_{FL}$ Applied Voltage Range	$-V_{FL}$	*	-27	~	0	V
Operating Supply Current	I_{DD}	Normal operation (Output current exclude)	-	1.0	3.0	mA
Memory Holding Supply Current	I_{HD1}	V_{DD}=5V Crystal oscillation stops	-	0.07	1.0	μA
	I_{HD2}	V_{DD}=2V Crystal oscillation stops	-	-	0.5	
Crystal Oscillation Frequency	f_{XT}	*	-	7.2	-	MHz

KEY INPUT PORT (K_0~K_3)

High Level Input Voltage	V_{IH1}	$-V_{FL}$=-27V	-5	~	5	V
Low Level Input Voltage	V_{IL1}	$-V_{FL}$=-27V	-27	~	-17	V
Pulldown Resistor	R_{IN1}	$-V_{FL}$=-27V	50	110	200	kΩ

DIGIT (D_0~D_6), SEGMENT (a~h) OUTPUT

High Level Output Current (DIG.)	I_{OH1}	V_{OH}=2V, $-V_{FL}$=-27V	-10	-14	-	mA
High Level Output Current (SEG.)	I_{OH2}	V_{OH}=2V, $-V_{FL}$=-27V	-3.0	-9.5	-	mA
Output Off-leak Current	I_{OFF}	V_{OUT}=$-V_{FL}$=-27V	-	-	-10	μA
Load Resistor	R_L	$-V_{FL}$=-27V	50	110	200	kΩ

MUTE, REF OUTPUT, P1-2, P2-1~4, P3-1~4 PORT

High Level Output Current	I_{OH3}	V_{OH}=4.0V	-0.6	-1.4	-	mA
Low Level Output Current	I_{OL3}	V_{OL}=1.0V	0.6	1.4	-	mA

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SO, CK, STB OUTPUT						
High Level Output Current	I_{OH4}	V_{OH}=4.0V	-1.0	-2.0	-	mA
Low Level Output Current	I_{OL4}	V_{OL}=1.0V	1.0	2.0	-	mA
SI, $\overline{INH}$, $\overline{INT}$, P1-2, P2-1~4, P3-1~4 PORT						
High Level Input Voltage ($\overline{INH}$)	V_{IH2}		4.3	~	5.0	V
Low Level Input Voltage ($\overline{INH}$)	V_{IL2}		0	~	2.7	V
High Level Input Voltage (Others)	V_{IH3}		3.5	~	5.0	V
Low Level Input Voltage (Others)	V_{IL3}		0	~	1.5	V
High Level Input Current	I_{IH}	V_{IH}=5.0V	-	-	1.0	μA
Low Level Input Current	I_{IL}	V_{IL}=0V	-	-	-1.0	μA
X_T Input Feedback Resistor	Rf		250	500	1000	kΩ
TEST Terminal Pulldown Resistor	R_{IN2}		15	30	60	kΩ

Note : * Marked items are guaranteed within a range of V_{DD}=4.5~5.5V, Ta=-30~75°C.

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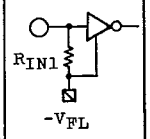
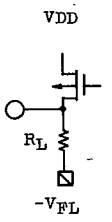
FUNCTIONS OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
1	GND	GND Terminal	This is a ground terminal of device.	-
2~5	K_0~K_3	Key Input Port	They are 4-bit input ports exclusively for inputting key matrix. They have input latches in which input data at digit timing designated by program are read. The read data is taken into data memory through executing KEY input instruction. These are terminals of high withstand voltage structure containing pulldown resistor in which voltage V_{DD} to $-V_{FL}$ can be input directly. For key return timing signal source, use digit outputs of D_0~D_6.	
6~12	D_0~D_6	Digit Output	They are seven output terminals exclusively for digit signal of display use. Signals of 1/10 duty are outputted to these terminals with cycle of 1.778ms on V_{DD}~$-V_{FL}$ voltage level. Output form is P-ch FET output of high breakdown voltage structured containing load resistor and is able to drive VFL indication tube directly. These terminals are used as key return timing signal outputs of key matrix. (Note) During system resetting and executing of CKSTP instruction, outputs are all automatically fixed to level "L" ($-V_{FL}$ voltage level).	

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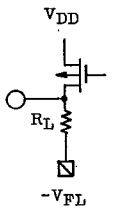
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
13~20	a~h	Segment Output	These are eight output terminals exclusivelly for segment signal of display use. Signals according to digit timing of D0~D6 are outputted to these terminals on V_{DD}~-V_{FL} voltage. 7-segment display data is outputted through decoder by the execution of SEG instruction, and mark segment display data is outputted by MARK instruction. Blanking of 1/5 duty per one digit are provided to these outputs and the control of dimmer function is also possible with program. Output form is the same as that of digit output, VFL indication tube is directly driven and dynamic display of 7-digit X 8-segment is performed. (Note) During system resetting and executing of CKSTP instruction, outputs are all automatically fixed to level "L" (-V_{FL} voltage level).	
21	-V_{FL}	High breakdown Voltage Portion Minus Power Supply Impressing Terminal	This is a terminal to be impressed with minus side power supply of high breakdown voltage portion in device (key input port, digit, segment output). Voltage within the range of 0~-27V is impressed according to the characteristics of VFL indicating tube. VFL indicating tube can be directly driven by digit and segment outputs.	-

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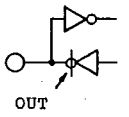
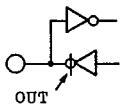
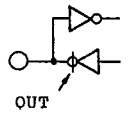
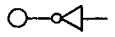
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
22~25	P3-1 ~ P3-4	I/O Port 3	These are 4-bit I/O ports. In these ports, input/output designation for every one bit can be made. This designation is performed with the contents of internal port called PORT-3 I/O CONTROL.	
26~29	P2-1 ~ P2-4	I/O Port 2	These are 4-bit I/O ports. In these ports, input/output designation for every one bit can be made. This designation is performed with the contents of internal port called PORT-2 I/O CONTROL.	
30	P1-2	I/O Port 1	This is a 1-bit port. In this port, input/output designation is possible. This designation is performed with the contents of internal port called PORT-1 I/O CONTROL.	
31	MUTE	Muting Signal Output Port	This is a 1-bit output port. It is usually used as the signal output of muting control. This port is arranged on the same port as I/O port 1. (Note) When $\overline{INH}$ input is changing as "H"↔"L", the output is automatically set to "H" level.	

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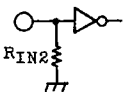
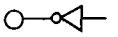
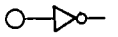
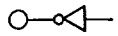
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
32	TEST	Test Mode Control Input	This is an input terminal for controlling test mode. Test mode is made with "H" level input, and normal operation is made with "L" level input or NC state. It contains pulldown resistor, and is usually fixed at "L" level or NC condition to be used. In test mode, the device functions as evaluator ship and program evaluation at EPROM base is possible when combined with external simulation board.	
33	STB	Strobe Pulse Output	These are serial interfaces. By executing SIO instruction, external PLL LSI and peripheral optional ICs connected to serial bus line can be controlled powerfully. As for serial transfer system, two kinds of $\overline{NCD}$/NCD modes can be selected by program.	
34	CK	Serial Clock Output		
35	SO	Serial Data Output		
36	SI	Serial Data Input		
37	REF	Reference Frequency Signal Output	This is an output terminal of reference frequency signal supplied to PLL LSI. It is possible to select eight kinds of reference frequency signals, 1kHz, 5kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 50kHz and 100kHz with the program. (Note) When $\overline{INH}$ input is at "L" level, output is automatically fixed at "L" level.	

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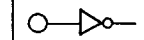
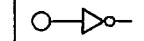
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
38	$\overline{INT}$	Initializing Input	This is a system reset signal input terminal of the device. While $\overline{INT}$ input is at "L" level, reset is applied, and when it becomes "H" level, the program starts from address zero. When the voltage, 0V→4.5V, is supplied to V_{DD} terminal, system reset is applied usually (power-on reset), and so this terminal is fixed at "H" level to be used. (Note) After system reset, all the I/O ports are set at input mode, however, since the contents of output port and internal port are indefinite, perform initialization with the program according to the necessity.	
39	$\overline{INH}$	Inhibit Input	This is a pulsing signal input port of radio mode. It judges the mode as radio-on mode at "H" level input and as radio off mode at "L" level input. When this terminal is at "L" level, REF output is automatically fixed at "L" level. Further, if CKSTP instruction is used in the program, and this CKSTP instruction is executed while $\overline{INH}$ input is at "L" level, the internal clock generator and CPU stop their operations and memory backup condition can be realised at low current consumption (1μA or less). At this time, all the output terminals (indication output, output port, etc.) are automatically fixed at "L" level.	

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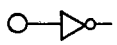
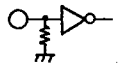
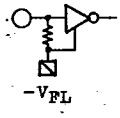
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	NOTE
			(Note) CKSTP instruction is effective when $\overline{INH}$ is at "L" level, and the same operation as that of NOOP instruction is made if executed when $\overline{INH}$ is at "H" level.	
40 41	$\overline{X_T}$ X_T	Crystal Oscillation Terminal	These are connecting terminals of crystal oscillator. 7.2MHz crystal is connected. Oscillation is automatically stopped at the execution of CKSTP instruction.	–
42	V_{DD}	Power Supply Terminal	This a power supply terminal of the device. Voltage of 5V±10% is supplied in the normal operation. In backup condition (during the execution of CKSTP instruction), voltage can be lowered down to 2V. When voltage, 0V→4.5V, is supplied to this terminal, system reset is applied to the device, and the program starts from address zero (power-on reset). (Note) Perform power-on reset from the condition of $\overline{INH}$="L" level. (Note) As the contents of each port(output port, internal port, etc.) are indefinite at putting the power supply on, carry out initialization according to the necessity.	–

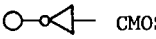
(Supplement)

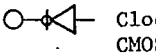

CMOS input


Built-in pulldown CMOS input



Built-in pulldown resistor
High breakdown voltage structured CMOS input (V_{SS}=$-V_{FL}$)


CMOS output


Clocked gate type CMOS output

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EXPLANATION OF OPERATION

○ CPU

CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, data resistor, carry F/F and judging circuit.

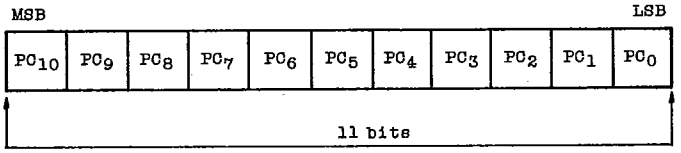
1. Program Counter (PC)

Program counter is the counter for addressing program memory (ROM), and is composed of 11-bit binary up counter.

This is cleared by system reset, and the program starts from address zero.

Usually, increment is made one by one everytime one instruction is executed, but when the instruction of JUMP or CAL is executed, the address designated at operand of that instruction is loaded.

Further, when the instruction (AIS, SLT, TMT, RNS instructions, or others) having skip function is executed, two increments of program counter are made if the result is the condition to be skipped, and the succeeding instruction is skipped.



2. Stack Register (STACK)

This is a register composed of 1 X 11 bits. During the execution of sub-routine call instruction, the value obtained by adding +1 to the contents of program counter, namely return address, is loaded.

The contents of stack register are loaded on the program counter by the execution of return instructions (RN, RNS instructions).

This stack level is 1 level and nesting is 1 level.

3. ALU

ALU has binary 4-bit parallel addition and subtraction, logical operation, comparison and plural bit judge functions.

This CPU has no accumulator, and all the operations directly treat the contents of data memory.

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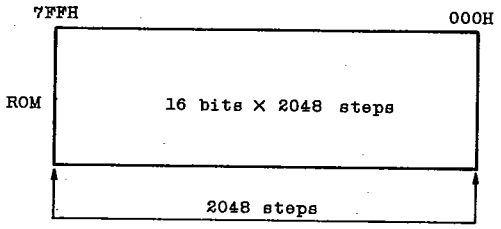
4. Program Memory (ROM)

Program memory is composed of 16 bit X 2048 steps and stares the program.
Applicable address range is 2048 steps of the address of 000H~7FFH.
Program memory has no concept of page or field, and JUMP and CAL instructions can be freely used among 2048 steps.
Optional address of program memory can be used as data area, and its contents, 16 bits, can be loaded on the data register by executing DAL instruction.

(Note) Provide the data area in the program memory at the address outside the Program loop.

(Note) In DAL instruction operation, the address of program memory can be designated as the data area becomes 1024 steps of 000H~3FFH.

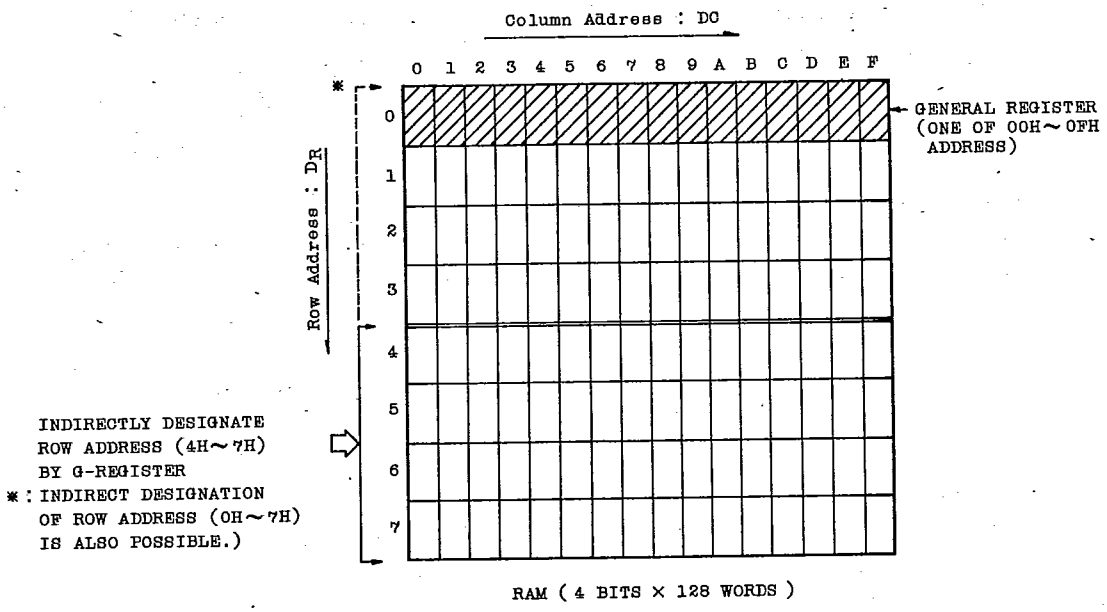


5. Data Memory (RAM)

Data memory is composed of 4 bits X 128 words and is used for storing the data. These 128 words are expressed with row address (3 bits) and column address (4 bits). 64 words (row address=4H~7H address) in the data memory are the indirect addressing by G-register. For this reason, it is necessary in advance to designate row address by G-register when carrying out data processing within this territory.
00H~0FH address in the data memory is called general register, and can be used only by designating column address (4 bits).
These 16 general registers can be used for operation and transfer between data memories. It can also be used as ordinary data memory.

(Note) The column address (4 bits) to designate general register becomes general register number.

(note) It is also possible to indirectly designate all the row addresses (0H~7H address) by G-register.



6. G-register (G-REG.)

G-register is a 3-bit register for addressing 64-word row address (DR=4H~7H address) of data memory. Contents of this register are effective at executing MVGD instruction and MVGS instruction, and are not related with the execution of other instructions. This register is treated as one of the ports, and its contents are set by the execution of IO instruction among input/output instructions.

(→Refer to register port item 1. P. 50.)

7. Data Register (DATA REG.)

This is a register composed of 1 X 16 bits. In this register, 16-bit data of optional address among program memory of 000H~3FFH is loaded at the execution of DAL instruction. This register is treated as one of the ports, and the contents are read in the data memory in 4-bit unit when the KEY instruction among input/output instructions is executed.

(→Refer to register port item 2. P. 51.)

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8. Carry F/F (C. F/F)

This is set when carry or borrow is produced as the result of executing the operational instruction, and is reset when it is not produced.

(Note) In all instruction operation, the contents of carry F/F always changes for the results.

9. Judge Circuit (J)

When skip function instruction is executed, this circuit judges its skip condition. When skip condition is satisfied, this circuit makes two steps increment of program counter, and skips the suceeding instruction.

29 kinds of instructions are available with abundant skip functions.

(→ Refer to *marked instructions in item 11, list of explanations of instruction function and operation.)

10. Instruction Set List

62 kinds of instructions in all consisting of 1-word instruction are available. These instructions are expressed with 6-bit instruction code.

HIGHER RANK 2 BITS / LOWER RANK 4 BITS		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	LD r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	ST M, r	SGEI M, I
0010	2	AIN M, I	ADN r, M	MVRD r, M	SEQI M, I
0011	3	SI M, I	SU r, M	MVRS M, r	SNEI M, I
0100	4	SIS M, I	SUS r, M	MVSR M1,M2	SLT r, M
0101	5	SIN M, I	SUN r, M	MVIM M, I	SGE r, M
0110	6	CAL ADDR1	ORR r, M	MVGD r, M	SEQ r, M
0111	7		ANDR r, M	MVGS M, r	SNE r, M
1000	8	AIC M, I	AC r, M	PLL M, C	TMTR r, M
1001	9	AICS M, I	ACS r, M	SEG M, C	TMFR r, M
1010	A	AICN M, I	ACN r, M	MARK M, C	TMT M, N
1011	B	SIB M, I	SB r, M	IO M, C	TMF M, N
1100	C	SIBS M, I	SBS r, M	KEY M, C	DAL ADDR2,r
1101	D	SIBN M, I	SBN r, M	SIO M, C	WAIT
1110	E	JUMP ADDR1	ORIM M, I	RN	CKSTP
1111	F		ANIM M, I	RNS	NOOP

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11. Explanation List of Function and Operation of Instructions
(Explanation of Symbols in the List)

M : data memory address
Normally, one of 00H~3FH addresses in data memory.

r : General register
One of 00H~0FH addresses in data memory.

PC : Program counter (11 bits)

STACK : Stack register (11 bits)

G : G-register (3 bits)

Data : Data register (16 bits)

I : Immediate data (4 bits)

N : Bit position (4 bits)

— : ALL "0"

C : Code No. of port (4 bits)

C_N : Lower rank 3 bits of port code No.

R_N : General register No. (4 bits)

ADDR1 : Program memory address in Page 0 or 1. (10 bits)

ADDR2 : Higher rank 6 bits of program memory address in page 0.

Ca : Carry

b : Borrow

PLL : Port treated at execution of PLL instruction

SEG : Port treated at execution of SEG instruction

MARK : Port treated at execution of MARK instruction

IO : Port treated at execution of IO instruction

KEY : Port treated at execution of KEY instruction

SIO : Port treated at execution of SIO instruction

( ) : Contents of register or data memory

[ ]C : Contents of port indicated with code No. C (4 bits)

[ ] : Contents of data memory indicated with contents of register or data memory

[ ]P : Contents of program memory (16 bits)

IC : Instruction code (6 bits)

* : Instruction with skip function

DC : Data memory column address (4 bits)

DR : Data memory row address (2 bits)

(Note) Address 000H~3FFH of program memory : Page 0 area

(Note) Address 400H~7FFH of program memory : Page 1 area

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
ADDITION INSTRUCTIONS	AI M,I		Add immediate data to memory	M←(M) + I	000000	D_R	Dc	I
	AIS M,I	*	Add immediate data to memory, then skip if carry	M←(M) + I Skip if carry	000001	D_R	Dc	I
	AIN M,I	*	Add immediate data to memory, then skip if not carry	M←(M) + I Skip if not carry	000010	D_R	Dc	I
	AIC M,I		Add immediate data to memory with carry	M←(M) + I + ca	001000	D_R	Dc	I
	AICS M,I	*	Add immediate data to memory with carry, then skip if carry	M←(M) + I + ca Skip if carry	001001	D_R	Dc	I
	AICN M,I	*	Add immediate data to memory with carry, then skip if not carry	M←(M) + I + ca Skip if not carry	001010	D_R	Dc	I
	AD r,M		Add memory to general register	r←(r) + (M)	010000	D_R	Dc	R_N
	ADS r,M	*	Add memory to general register, then skip if carry	r←(r) + (M) Skip if carry	010001	D_R	Dc	R_N
	ADN r,M	*	Add memory to general register, then skip if not carry	r←(r) + (M) Skip if not carry	010010	D_R	Dc	R_N
	AC r,M		Add memory to general register with carry	r←(r) + (M) + ca	011000	D_R	Dc	R_N
	ACS r,M	*	Add memory to general register with carry, then skip if carry	r←(r) + (M) + ca Skip if carry	011001	D_R	Dc	R_N

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INST. Gr.	MNEMONIC		EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
SUBTRACTION INSTRUCTION	ACN r,M	*	Add memory to general register with carry, then skip if not carry	r←(r) + (M) + ca Skip if not carry	011010	DR	Dc	RN
	SI M,I		Subtract immediate data from memory	M←(M) - I	000011	DR	Dc	I
	SIS M,I	*	Subtract immediate data from memory, then skip if borrow	M←(M) - I Skip if borrow	000100	DR	Dc	I
	SIN M,I	*	Subtract immediate data from memory, then skip if not borrow	M←(M) - I Skip if not borrow	000101	DR	Dc	I
	SIB M,I		Subtract immediat data from memory with borrow	M←(M) - I - b	001011	DR	Dc	I
	SIBS M,I	*	Subtract immediate data from memory with borrow, then skip if borrow	M←(M) - I - b Skip if borrow	001100	DR	Dc	I
	SIBN M,I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M←(M) - I - b Skip if not borrow	001101	DR	Dc	I
	SU r,M		Subtract memory from general register	r←(r) - (M)	010011	DR	Dc	RN
	SUS r,M	*	Subtract memory from general register, then skip if borrow	r←(r) - (M) Skip if borrow	010100	DR	Dc	RN
	SUN r,M	*	Subtract memory from general register, then skip if not borrow	r←(r) - (M) Skip if not borrow	010101	DR	Dc	RN

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
SUBTRACTION INSTRUCTION	SB r,M		Subtract memory from general register with borrow	r←(r) - (M) - b	011011	D_R	Dc	R_N
	SBS r,M	*	Subtract memory from general register with borrow, then skip if borrow	r←(r) - (M) - b Skip if borrow	011100	D_R	Dc	R_N
	SBN r,M	*	Subtract memory from general register with borrow, then skip if not borrow	r←(r) - (M) - b Skip if not borrow	011101	D_R	Dc	R_N
COMPARISON INSTRUCTION	SLTI M,I	*	Skip if memory is less than immediate data	Skip if (M) <I	110000	D_R	Dc	I
	SGEI M,I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧I	110001	D_R	Dc	I
	SEQI M,I	*	Skip if memory is equal to immediate data	Skip if (M)=I	110010	D_R	Dc	I
	SNEI M,I	*	Skip if memory is not equal to immediate data	Skip if (M)≠I	110011	D_R	Dc	I
	SLT r,M	*	Skip if general register is less than memory	Skip if (r) <(M)	110100	D_R	Dc	R_N
	SGE r,M	*	Skip if general register is greater than or equal to memory	Skip if (r) ≧(M)	110101	D_R	Dc	R_N
	SEQ r,M	*	Skip if general register is equal to memory	Skip if (r)=(M)	110110	D_R	Dc	R_N
	SNE r,M	*	Skip if general register is not equal to memory	Skip if (r)≠(M)	110111	D_R	Dc	R_N

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
TRANSFER INSTRUCTION	LD r,M		Load memory to general register	r ← (M)	100000	DR	DC	RN
	ST M,r		Store general register to memory	M ← (r)	100001	DR	DC	RN
	MVRD r,M		Move memory to destination memory referring to general register in the same row	[DR, (r)] ← (M)	100010	DR	DC	RN
	MVRS M,r		Move source memory referring to general register to memory in the same row	M ← [DR, (r)]	100011	DR	DC	RN
	MVSR M1,M2		Move memory to memory in the same row	(DR,DC1) ← (DR,DC2)	100100	DR	DC1	DC2
	MVIM M,I		Move immediate data to memory	M ← I	100101	DR	DC	I
	MVGD r,M		Move memory to destination memory referring to G-register and general register	[(G),(r)] ← (M)	100110	DR	DC	RN
	MVGS M,r		Move source memory referrring to G-register and general register to memory	M ← [(G), (r)]	100111	DR	DC	RN

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
INPUT/OUTPUT INSTRUCTION	PLL M,C		Input PLL port data to memory	M ←[PLL]C	101000	DR	DC	0 CN
			Output contents of memory to PLL port	[PLL]C ←(M)		DR	DC	1 CN
	SEG M,C		Input SEG port data to memory	M ←[SEG]C	101001	DR	DC	0 CN
			Output contents of memory to SEG port	[SEG]C ←(M)		DR	DC	1 CN
	MARK M,C		Input MARK port data to memory	M ←[MARK]C	101010	DR	DC	0 CN
			Output contents of memory to MARK port	[MARK]C ←(M)		DR	DC	1 CN
	IO M,C		Input IO port data to memory	M ←[IO]C	101011	DR	DC	0 CN
			Output contents of memory to IO port	[IO]C ←(M)		DR	DC	1 CN
	KEY M,C		Input KEY port data to memory	M ←[KEY]C	101100	DR	DC	0 CN
			Output contents of memory to KEY port	[KEY]C ←(M)		DR	DC	1 CN
	SIO M,C		Serial input port data of external device to memory	M ←[SIO]C	101101	DR	DC	0 CN
			Serial output contents of memory to port of external device	[SIO]C ←(M)		DR	DC	1 CN

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
LOGICAL OPERATION INSTRUCTION	ORR r,M		Logical OR of general register and memory	r ← (r) ∨ (M)	010110	DR	Dc	RN
	ANDR r,M		Logical AND of general register and memory	r ← (r) ∧ (M)	010111	DR	Dc	RN
	ORIM M,I		Logical OR of memory and immediate data	M ← (M) ∨ I	011110	DR	Dc	I
	AMIM M,I		Logical AND of memory and immediate data	M ← (M) ∧ I	011111	DR	Dc	I
BIT JUDGE INSTRUCTION	TMTR r,M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r[N(M)]=all "1"	111000	DR	Dc	RN
	TMFR r,M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r[N(M)]=all "0"	111001	DR	Dc	RN
	TMT M,N	*	Test memory bits, then skip if all bits specified are true	Skip if M(N)=all "1"	111010	DR	Dc	N
	TMF M,N	*	Test memory bits, then skip if all bits specified are false	Skip if M(N)=all "0"	111011	DR	Dc	N

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INST. Gr.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bits) IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
SUB-ROUTINE INSTRUCTION	CAL ADDR1		Call subroutine in page 0	STACK ← (PC) + 1 and PC ← ADDR1 in page 0 or 1	000110	ADDR1 (10 bits)		
			Call subroutine in page 1		000111			
	RN		Return to main routine	PC ← (STACK)	101110	-	-	-
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	101111	-	-	-
JUMP INST.	JUMP ADDR1		Jump to the address specified in page 0	PC ← ADDR1 in page 0 or 1	001110	ADDR1 (10 bits)		
			Jump to the address specified in page 1		001111			
OTHER INSTRUCTIONS	DAL ADDR2,r		Load program memory in page 0 to DATA register	DATA ← [ADDR2+(r)]P in page 0	111100	ADDR2 (6 bits)		R_N
	WAIT		Wait conditionally	Wait until key in or timer F/F set up etc.	111101	-	-	-
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH}$="0"	111110	-	-	-
	NOOP		No operation	-	111111	-	-	-

(Note 1) During the execution of input/output instruction, control of input/output of instruction is automatically carried out at the most significant bit value of code No.(C) of port.

- MSB="1" of code No.(C) : output instruction
- MSB="0" of code No.(C) : input instruction

(Note 2) Basically, the execution of SIO instruction is treated in the same way as the execution of other input/output instructions (PLL instruction, SEG instruction, etc.), but it differs in the following points.

- It is necessary for the first time to select an external device which is to become the transfer address of serial data by chip select code ((C)=FH). (→Refer to Serial Interface Item 1. P.55)
- Execution time for SIO instruction is 88.8μs.

(Note 3) In TC9301AN, the input port to be treated by the execution of SEG instruction does not exist and this input instruction can not be applied.

(Note 4) The lower rank 4 bits among the program memory address in page 0 10 bits assined by DAL instruction become indirect addressing based on the contents of general register.
Executing time of DAL instruction is 88.8μs equally to that of SIO instruction.

(Note 5) When WAIT instruction is executed, the program keeps its waiting condition at that address until the instruction is released under the following conditions:

- When input (K_0~K_3 ports) is made to key input port.
- When $\overline{INH}$ input changes.
- When 2Hz timer F/F is set.

When WAIT mode is released, the instruction of next address is executed.
If WAIT instruction is executed during the above conditions, same operation as that of NOOP instruction is made.

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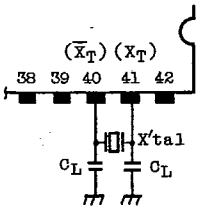
○CONNECTION OF CRYSTAL OSCILLATOR

Connect 7.2MHz crystal oscillator with the crystal oscillator terminals ($\overline{X_T}$, X_T terminals) of the device as shown below.
This oscillation signal is supplied to clock generator and reference frequency divider, and produces various kinds of timing signals of CPU and reference frequency signals.
Adjust crystal oscillation frequency with the reference frequency output terminal monitored.



X'tal=7.2MHz

C_L=10~50pF (30pF TYP.)

(Note) Use crystal oscillator of low CI value and satisfactory starting characteristics.

○SYSTEM RESET

System reset is applied to the device when "L" level is given to $\overline{INT}$ terminal, or when the voltage of 0V→4.5V is supplied to V_{DD} terminal (power-on reset).
After stand-by time of 10ms from system reset, program starts from address zero.
Since power-on reset function is usually provided, $\overline{INT}$ terminal is fixed at "H" level.

(Note 1) During system reset time and its succeeding stand-by time, digit output and segment output are fixed at "L" level ($-V_{FL}$ level).

(Note 2) After system reset, I/O ports 1~3 are all set at input mode, however, the initialization of output port or internal port is not carried out. Since the contents of these ports become indefinite especially at power-on stage, it is recommended to make initialization with program if necessary.

(Note 3) Carry out power-on reset from $\overline{INH}$="L" level condition.

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○ BACKUP MODE

If CKSTP instruction is executed while $\overline{INH}$ terminal is at "L" level, clock generator and CPU in the device stop operation completely, and memory backup state can be realized at low consumption current (1μA MAX. at V_{DD}=5V).

At this time, display output terminals and output ports are all fixed at "L" level automatically, and therefore the processing of output terminal by program is usually not required.

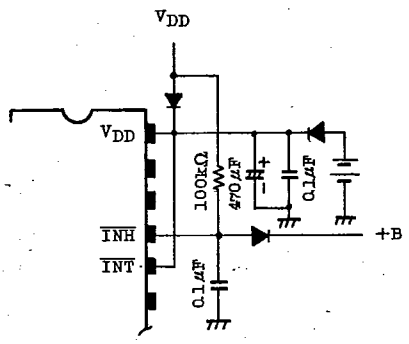
With this backup mode, supply voltage can be lowered down to 2V.

In backup mode, program stops at the execution address of CKSTP instruction, backup mode is released at $\overline{INH}$="H" level, and the next address is executed after the standby time of 10ms.

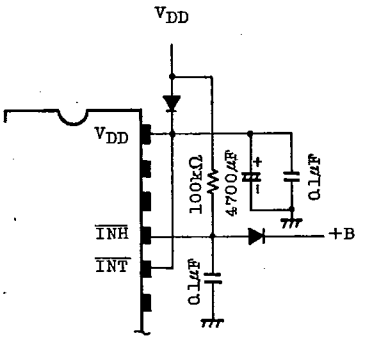
(Note 1) In backup mode, the states of output terminals are all fixed at "L" level, however, as the contents of output port, the data of just before backup mode is held.

(Note 2) When CKSTP instruction is executed during $\overline{INH}$="H" level, the same operation as that of NOOP instruction is made. (Backup mode is not entered.)

EXAMPLE OF BACKUP CIRCUIT



BACKUP BY BATTERY



BACKUP BY CAPACITOR

+B shall be connected to a fast fall power supply when the power switch of a set is turned off.

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I/O MAP

CODE (K) / I/O PORT	PLL (Ø1) Y1	PLL (Ø1) Y2	PLL (Ø1) Y4	PLL (Ø1) Y8	SEG (Ø2) Y1	SEG (Ø2) Y2	SEG (Ø2) Y4	SEG (Ø2) Y8	MARK (Ø5) Y1	MARK (Ø5) Y2	MARK (Ø5) Y4	MARK (Ø5) Y8	IO (Ø4) Y1	IO (Ø4) Y2	IO (Ø4) Y4	IO (Ø4) Y8	KEY (Ø5) Y1	KEY (Ø5) Y2	KEY (Ø5) Y4	KEY (Ø5) Y8	SIO (Ø6) Y1	SIO (Ø6) Y2	SIO (Ø6) Y4	SIO (Ø6) Y8
INPUT PORT (K) 0									a (D6)	b (D6)	c (D6)	d (D6)	MUTE	P1-2	0	0	KEY RETURN TIMING INPUT							
																	D0	D1	D2	D3				
1									e (D6)	f (D6)	g (D6)	h (D6)	-1	-2	-3	-4	KEY RETURN TIMING INPUT				SERIAL INPUT CODE No. (C) = 0H~7H			
														I/O PORT 2			D4	0	D5	D6				
2									d (D0)	e (D0)	f (D0)	g (D0)	-1	-2	-3	-4	KEY INPUT							
														I/O PORT 3			K0	K1	K2	K3				
3									c (D4)	d (D4)	e (D4)	f (D4)					SIO NCD	0	0	0				
4									h (D0)	h (D1)	h (D2)	h (D3)	INH	0	0	0	DATA REGISTER							
																	d0	d1	d2	d3				
5	REF. SELECT #0 #1 #2			0					h (D4)	0	h (D5)	F-DIM	2Hz F/F	10Hz	KO	KEY ON	DATA REGISTER							
																	d4	d5	d6	d7				
6													KEY RETURN TIMING SELECT				DATA REGISTER							
													#0	#1	#2	#3	d8	d9	d10	d11				
7													KEY RETURN TIMING SELECT				DATA REGISTER							
													#4	#5	#6	#7	d12	d13	d14	d15				
OUTPUT PORT (L) 8					CH (D5) #0	#1	#2	#3	a (D6)	b (D6)	c (D6)	d' (D6)	MUTE	P1-2	*	*	*	P1-2 I/O	*	*	SERIAL OUTPUT CODE No. (C) = 8H~EH			
9									e (D6)	f (D6)	g (D6)	h (D6)	-1	-2	-3	-4	PORT-2 I/O CONTROL							
A					0/5 (D4) #0	#1	#2	#3	d (D0)	e (D0)	f (D0)	g (D0)	-1	-2	-3	-4	PORT-3 I/O CONTROL							
B					× 1 (D3) #0	#1	#2	#3	c (D4)	d (D4)	e (D4)	f (D4)					SIO NCD	*	*	*				
C					× 10 (D2) #0	#1	#2	#3	h (D0)	h (D1)	h (D2)	h (D3)	G-REGISTER #0	#1	#2	*	DISP OFF	*	*	*				
D	REF. SELECT #0 #1 #2			*	× 100 (D1) #0	#1	#2	#3	h (D0)		h (D2)	h (D4)	2Hz F/F RESET	CLOCK RESET	KHY RESET	INH STB								
E					× 1000 (D0) #0	#1	#2	#3			h (D5)	F-DIM	KEY RETURN TIMING SELECT #0	#1	#2	#3								
F													KEY RETURN TIMING SELECT #4	#5	#6	#7	T.	T	*	*	CHIP SELECT #0	#1	#2	#3

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○ I/O MAP

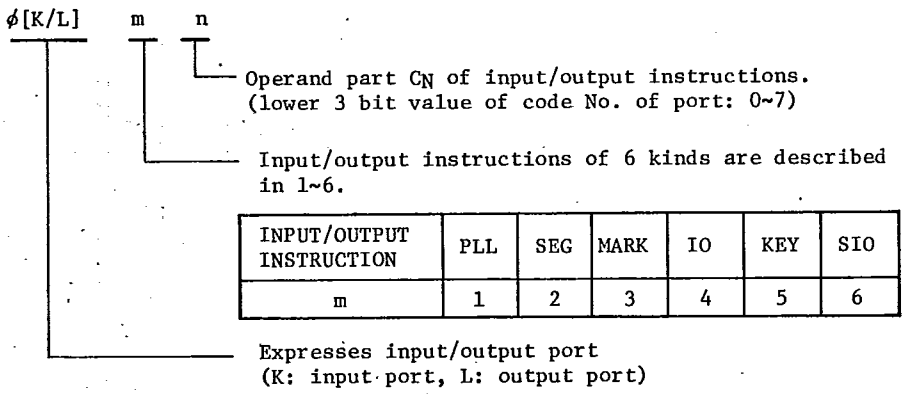
All ports in the device are expressed by six input/output instructions (PLL instruction, SEG instruction, MARK instruction, IO instruction, KEY instruction and SIO instruction) and 4-bit matrix of code No.C. Assignment of these ports is indicated previously as I/O map. In the I/O map, port names treated in the execution of each input/output instruction are assigned horizontally, while code No. of port are assigned vertically. G-register and data register are also treated as port. Basically, the data is treated at each port as 4-bit unit, and code No.(C)=0H~7H are assigned to input ports, while code No.(C)=8H~FH to output ports.

(Note 1) The port indicated with oblique line on I/O map is a port not existing in the device. In the execution of output instruction, when data is outputted to non-existing output port, no effect is given to the contents of other port or data memory. When non-existing input port is designated during the execution of input instruction, the contents read into the data memory become indefinite.

(Note 2) Among the output ports on I/O map, *marked port is an unused port. The data outputted here becomes "don't care".

(Note 3) Regarding the contents of port expressed with 4-bit, Y1 corresponds to the least significant bit of the data in data memory, and Y8 to the most significant bit. Data of each port are all treated with positive logic.

(Note 4) Each port assigned by six input/output instructions and code No.C is coded as follows.



INPUT/OUTPUT INSTRUCTION	PLL	SEG	MARK	IO	KEY	SIO
m	1	2	3	4	5	6

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○ REFFRENCE FREQUENCY DIVIDER

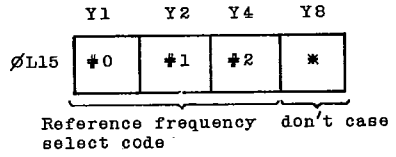
This unit divides oscillating frequency of external 7.2MHz crystal, and produces eight kinds of PLL reference frequency signals, 1kHz, 5kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 50kHz, 100kHz. Such selection is carried out with the data of REF select port.

The selected signal is supplied to PLL LSI from REF output terminal.

The reference frequency divider is reset with $\overline{INH}$="L" level input, and REF output is fixed at "L" level.

1. REF Select Port (ØKL15)

   This is an internal port to select eight kinds of reference frequency signals. Normally this port is accessed by PLL output instruction designating [C_N=5] at operand part. (ØL15). By the execution of PLL input instruction designating [C_N=5] at operand part, the contents of the data presently outputted is read into the data memory (ØK15).



REF. Code Table

#2	#1	#0		REFERENCE FREQUENCY
0	0	0	0	1 kHz
0	0	1	1	50 kHz
0	1	0	2	5 kHz
0	1	1	3	100 kHz
1	0	0	4	9 kHz
1	0	1	5	10 kHz
1	1	0	6	12.5 kHz
1	1	1	7	25 kHz

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o I/O PORT

1. I/O Ports 1~3

I/O port 1 is 1-bit, and I/O ports 2 and 3 are 4-bit ports, all of which are capable of making input/output setting with 1-bit unit. In the case of I/O port-1, input/output settings are made by the contents of port-1 I/O control internal port, while in the case of I/O port-2, they are made by the contents of port-2 I/O control internal port. And in I/O port-3, input/output settings are made by the contents of port-3 I/O control internal port.

Setting to input port can be made by setting "0" to the bit of corresponding I/O control port, and setting to output port can be made by setting "1" to the same location.

At setting to input port, the data inputted to I/O port at present is read into the data memory by the execution of IO input instruction designating [C_N=0~2] at operand part (ϕK40~ϕK42).

At this time, the contents of output side latch (ϕL40~ϕL42) give no effect to input port.

(Note) I/O port-1 (P1-2) and MUTE port are located on the same port (ϕKL40). Therefore, P1-2 and MUTE port are simultaneously treated by the execution of IO input/output instruction designating [C_N=0] at operand part.

During output port setting, output condition of I/O port is controlled by the execution of IO output instruction designating [C_N=0~2] at operand part (ϕL40~ϕL42). Setting of data "1" makes output "H" level and setting of "0" makes output "L" level.

Further, by the execution of IO input instruction, the contents of currently outputted data are read into the data memory (ϕK40~ϕK42).

(Note) IO control port is accessed by KEY output instruction designating [C_N=0~2] at the operand part. After system reset, the contents of this port are all reset to "0" and I/O ports are all set at input mode.

(Note) During backup mode, the output conditions of I/O port set at output mode are all fixed at "L" level automatically, however, the preceeding data is held in the contents of each output latch.

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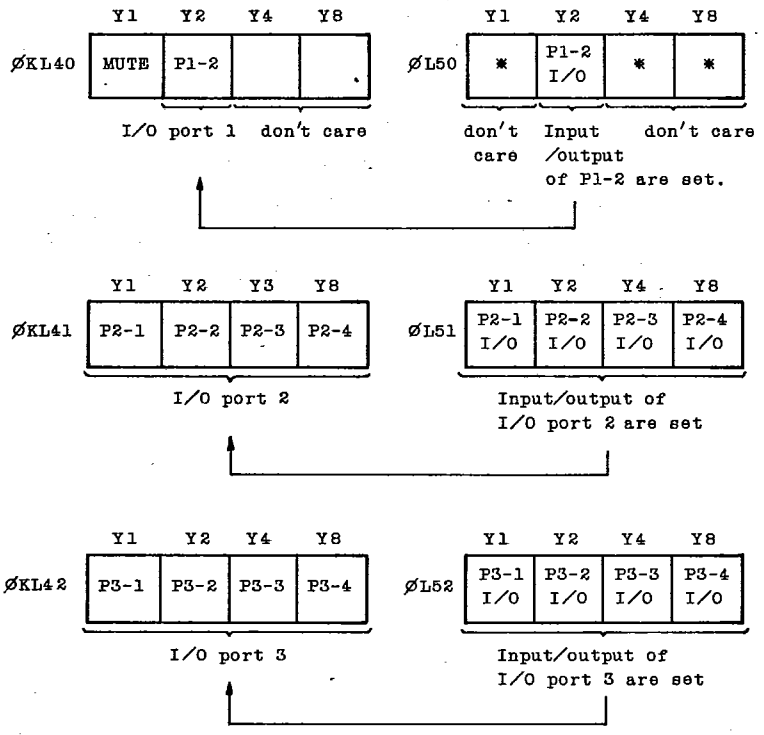

2. MUTE Port (ØKL40)

This is 1-bit CMOS type exclusive output port for muting control use. Normally, it is accessed by IO output instruction designating [C_N=0] at operand part (ØL40). By the execution of IO input instruction designating [C_N=0] at operand part, the contents of currently outputted data are read into data memory (ØK40).

(Note) When $\overline{INH}$ input has changed to "H"↔"L" level, the contents of MUTE port are automatically set at "1". Care must be taken because in this case, "0" data setting by program can not be applied to the contents of MUTE

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port until the changed $\overline{INH}$ input data is read into $\overline{INH}$ input latch by program ($\overline{INH}$ STB bit setting of ØL45).

Especially at power-on time, be sure to make access of MUTE port at least one time after setting "1" at $\overline{INH}$ STB bit by program.

(Note) During backup mode, MUTE output is automatically fixed at "L" level, however, the contents of port are set at "1" by the change of $\overline{INH}$ input.

(Note) MUTE port and I/O port-1 (P1-2) are located on the same port (ØKL40).

	Y1	Y2	Y4	Y8
ØL40	MUTE	P1-2	*	*

don't care

○ VACUUM FLUORESCENT INDICATION TUBE (VFL) DRIVER

TC9301AN contains high breakdown voltage structured VFL driver able to directly drive vacuum fluorescent indication tube.

With seven digit display signal outputs of D_0~D_6 (digit output) and eight segment display signal outputs of a~h, the dynamic display of 7 digits X 8 segments is performed. The structure of these terminals is P-ch FET drain output, and vacuum fluorescent indication tube is driven with the voltage level between V_{DD} voltage and minus voltage impressed to $-V_{FL}$ terminal. During no-load, to these terminals, V_{DD} voltage level is outputted at "H" level output and $-V_{FL}$ voltage level at "L" level output.

For the generation of dynamic display timing of each output of digit and segment, efficient support has been made by hardware.

The timing of digit output is generated by hardware requiring no support of program.

Regarding segment output, it is enough only to output segment display data to the segment port allotted with 4-bit unit, and decode operation and dynamic timing generation after that are performed automatically by hardware.

7-segment display data is controlled by the execution of SEG output instruction and mark segment display data is controlled by the execution of MARK output instruction.

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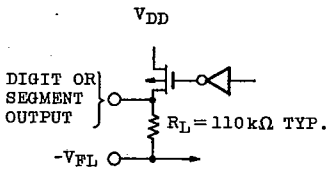
(Note) For both digit output and segment output, external load resistor is not required.

(Note) The range of minus voltage able to be impressed to $-V_{FL}$ terminal is 0~-27V.



VFL DRIVER TERMINAL EQUIVALENT CIRCUIT

1. Timing Chart of Digit Output

The timing of digit output waveform of D_0~D_6 is shown below.
Each digit output having 1.778ms cycle is the signal of 1/10 duty.
As shown in the figure, output is seven digits of D_0~D_6, however, it is composed of eight digits from the view point of timing.
In other words, there is a time in which all the display turn off during the time equivalent to one digit.
A cycle of digit output is 40-instruction cycle (an instruction cycle=44.4μs) and the time one digit of display lights (equivalent to one digit) is equivalent to 4-instruction cycle.

(Note) During system resetting and backup mode (at execution of CKSTP instruction), all the digit outputs are automatically fixed at "L" level ($-V_{FL}$ voltage level). When display off mode is set with program, all the digits are also set at "L" level. (→Refer to Item 6, Display off function. P.44).

(Note) Digit output is used also for key return timing signal source of key matrix. (→Refer to Item, Key input. P.45).

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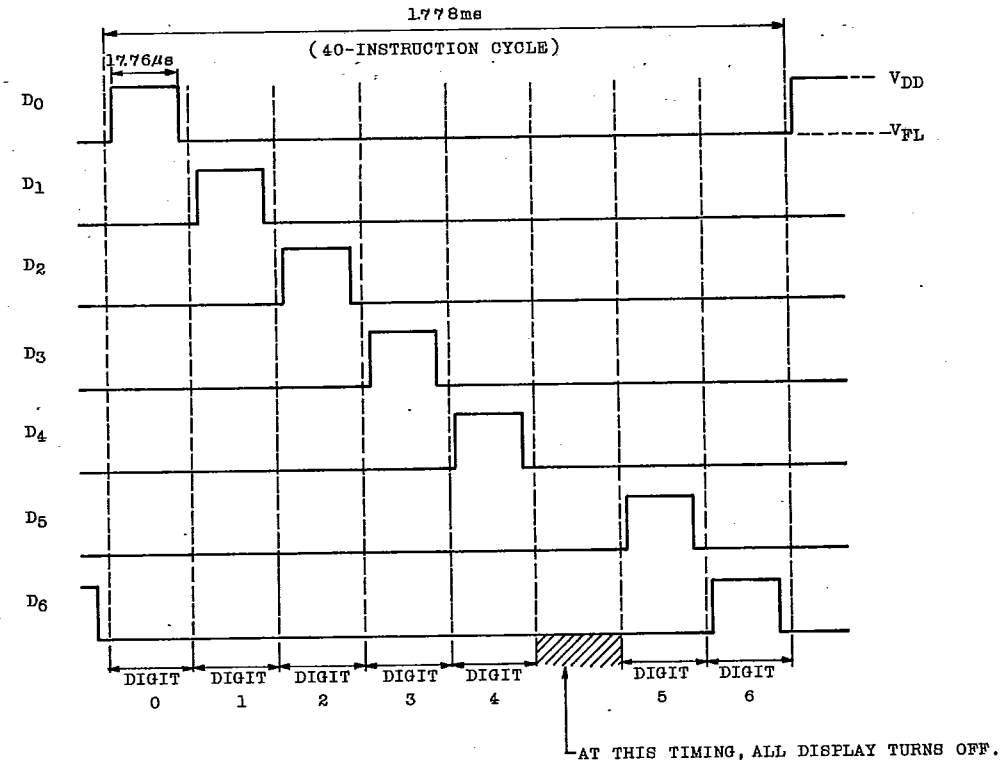
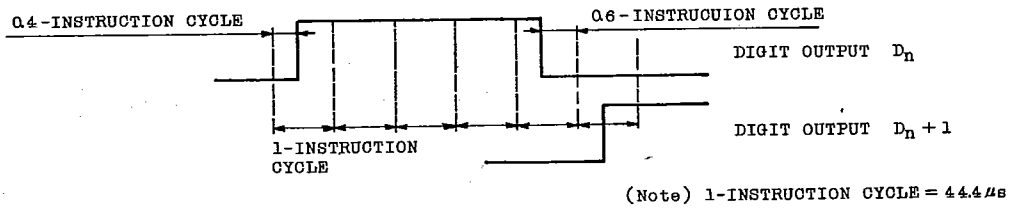


During the period each digit output waveform is at "H" level, one digit of vacuum fluorescent indication tube corresponding to that digit output lights, and turns off during the period of "L" level.



RELATION BETWEEN DIGIT OUTPUT SIGNAL TIMING AND INSTRUCTION CYCLE

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2. Dynamic Display Form

In TC9301AN, in order to make the most appropriate display form for realizing the function as DTS, totally 56 segments performing the dynamic display of 7 digit X 8 segments are in advance allotted to 7-segments and mark segments for every digit.

7-segments and mark segment display form allotted for every digit are shown in the following.

(Note) The allotment of these segments decided by hardware can not be changed.

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TC9301AN DYNAMIC DISPLAY FORM

(Note 1) ▭ means mark display segment. S( ) means the name of segment output which light mark segment.

(Note 2) Segment allotment is made of 7-segment + 1 mark display segment (totally 8 segments). (during the timing of D1~D3,D5).
However, segment allotment of each timing of D0, D4 and D6 is as fallows.

- At D0 timing, mark display segments are five segments of d~h, and 7-segment display is performed with three segments of a,b and c. Therefore, 7-segment data capable of display are three kinds, 1,2 and BLANK (all display turns off).
- At D4 timing, mark display segments are five segments of c~f and h, and 7-segment display is performed with three segments of a,b and g. Therefore, 7-segment data capable of display are three kinds of 0,5 and BLANK.
- At D6 timing, eight segments of a~h are all allotted to mark display segment.

7-SEGMENT
DISPLAY FORM

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3. 7-segment Display Ports (ϕL20, ϕL22~ϕL26)

These are the group of ports for outputting 7-segment display data of 6-digit at each timing D0~D5.

It is accessed with SEG output instruction.

4-bit data of 0H~FH set in these port are outputted to the segment terminals a~g with dynamic timing through built-in segment decoder.

The decode patterns of 7-segment decoder are shown below.

Table of 7-segment Display Pattern of Segment Decoder

7-Segment Port					Segment Output Display Pattern							Display Character Form
#3	#2	#1	#0		a	b	c	d	e	f	g	
0	0	0	0	0	H	H	H	H	H	H	L	0
0	0	0	1	1	L	H	H	L	L	L	L	1
0	0	1	0	2	H	H	L	H	H	L	H	2
0	0	1	1	3	H	H	H	H	L	L	H	3
0	1	0	0	4	L	H	H	L	L	H	H	4
0	1	0	1	5	H	L	H	H	L	H	H	5
0	1	1	0	6	H	L	H	H	H	H	H	6
0	1	1	1	7	H	H	H	L	L	L	L	7
1	0	0	0	8	H	H	H	H	H	H	H	8
1	0	0	1	9	H	H	H	H	L	H	H	9
1	0	1	0	A	H	L	L	H	H	H	H	C
1	0	1	1	B	L	H	H	L	H	H	H	H
1	1	0	0	C	H	H	L	L	H	H	H	P
1	1	0	1	D	H	H	H	L	H	H	H	D
1	1	1	0	E	L	L	L	L	L	L	H	—
1	1	1	1	F	L	L	L	L	L	L	L	BLANK (All display turns off)

(Note) "H"=V_{DD} voltage level and "L"=$-V_{FL}$ voltage level of segment output are shown. (providing at no-load)

. CH Port (ØL20)

This is a data output port of 7-segment to be displayed at digit timing D5. It is accessed with the execution of SEG output instruction designating [C_N=0] at operand part.

This 7-segment port is mainly used for displa/ the channel number of per-set memory.

	Y1	Y2	Y4	Y8
ØL20	#0	#1	#2	#3

7-segment data at D5 timing (0H~FH) is set.

. O/5 Port (ØL22)

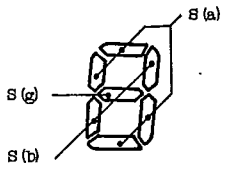
This is an output port of 7-segment data to be displayed at digit timing D4. It is accessed with the execution of SEG output instruction designating [C_N=2] at operand part. This 7-segment port is used exclusively for display 50kHz digit of receiving frequency at FM band. Therefore, 7-segment at D4 timing performs three kinds of display 0, 5, BLANK, with three segments, a,b,c. The data able to set to this port are only three kinds, 0H, 5H and FH. The display of 8 and - is possible with data 8H, EH set.

(Note) Care must be taken becouse if the data other than 0H, 5H, 8H, EH or FH is set to this port, correct 7-segment display can not be obtained.

(Note) Seven segments of vacuum fluorescent indication tube to be lighted at digit 4 timing are used through connecting with each segment.

	Y1	Y2	Y4	Y8
ØL22	#0	#1	#2	#3

7-segment display data at D4 timing is set. (Basically, three kinds, 0H, 5H, FH)



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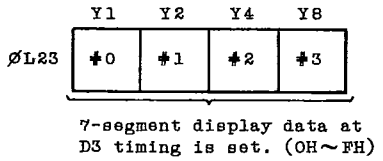
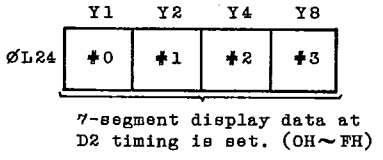
. X1 Port (ØL23)

This is an output port of 7-segment data to be displayed at digit timing D_3. It is accessed with the execution of SEG output instruction designating [C_N=3] at operand part. This 7-segment port is usually used for X1-digit display of receiving frequency of radio or for 1-minute digit of clock.



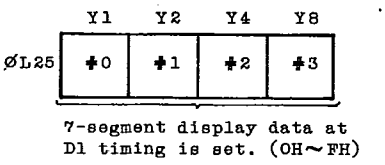
. X10 Port (ØL24)

This is an output port of 7-segment data to be displayed at digit timing D_2. It is accessed with the execution of SEG output instruction designating [C_N=4] at operand part. This 7-segment port is usually used for X10-digit display of receiving frequency of radio or for 10-minute digit of clock.



. X100 Port (ØL25)

This is an output port of 7-segment data to be displayed at digit timing D_1. It is accessed with the execution of SEG output instruction designating [C_N=5] at operand part. This 7-segment port is usually used for X100-digit display of receiving frequency of radio or for 1-hour digit of clock.

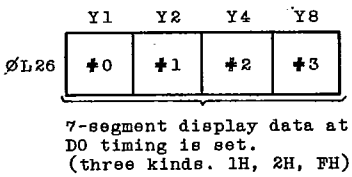


. X1000 Port (ϕL26)

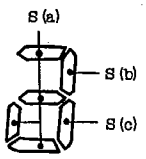
This is an output port of 7-segment data displayed at digit timing D0.
This is accessed with the execution of SEG output instruction designating [C_N=6] at operand part. This port is used for display of X1000-digit of radio receiving frequency, or for 10-hour digit of clock. Therefore, 7-segment at D0 timing performs three kinds of display, 1, 2, BLANK, with three segments, a,b,c.
The data able to set to this port are only three kinds, 1H, 2H, FH.

(Note) Care must be taken because if the data other than 1H, 2H or FH is set to this port, correct 7-segment display can not be obtained.

(Note) Seven segments of vacuum fluorescent indication tube to be lighted with digit 0 timing are used through connecting with each segment.



7-segment display data at D0 timing is set.
(three kinds. 1H, 2H, FH)



(Note)
If "2" display of 7-segment is not required, segment S(a) is needless.

4. Mark Segment Display Ports (ϕKL30~ϕKL35)

These are the group of ports for controlling 22 kinds of mark segment display at D0~D6 timing. This is accessed with the execution of MARK input/output instruction. Data is set from data memory to each port with the execution of MARK output instruction, and each port contents presently outputted are read into data memory with the execution of MARK input instruction.
To these segment ports, the segment output to be used for mark display and its digit timing are allotted in 1-bit unit. When data "1" is set to each port bit, the corresponding segment output becomes "H" level at allotted digit timing, and lights mark segment. When data "0" is set, segment output becomes "L" level at its digit timing, and mark segment turns off.

. a~h (at D_6) mark segment (ϕKL30, ϕKL31)

These are the ports for controlling eight mark segments to be displayed with segment outputs a~h at digit timing D_6. This is accessed with the execution of MARK input/output instructions designating [C_N=0 or 1] at operand part.

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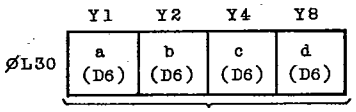
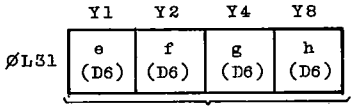


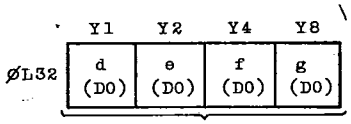
Data of mark segment displayed with segment output a~d at D6 timing is set.



Data of mark segment displayed with segment outputs e~h at D6 timing is set.

. d~g (at D_0) mark segment port (ØKL32)

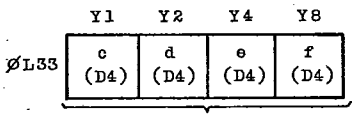
This is a port for controlling four mark segments to be displayed with segment outputs d~g at digit timing D_0. This is accessed with the execution of MARK input/output instructions designating [C_N=2] at operand part.



Data of mark segment displayed with segment output d~g at D0 timing is set.

. c~f (at D4) mark segment port (ØKL33)

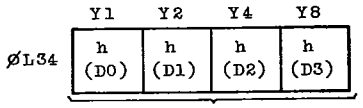
This is a port for controlling four mark segments displayed with segment outputs c~f at digit timing D4. This is accessed with the execution of MARK input/output instructions designating [C_N=3] at operand part.



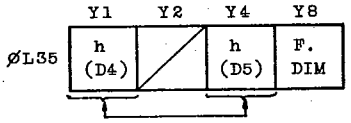
Data of mark segment displayed with segment outputs c~f at D4 timing is set.

. h (at D0~D5) mark segment ports (ØKL34, ØKL35)

These are the ports for controlling six mark segments displayed with segment output h at each digit timing D0~D5. This is accessed with the execution of MARK input/output instructions designating [C_N=4 or 5] at operand part.



Data of mark segment displayed with segment output h at each timing of D0~D3 is set.



Data of mark segment displayed with segment output h at each timing of D4 and D5 is set.

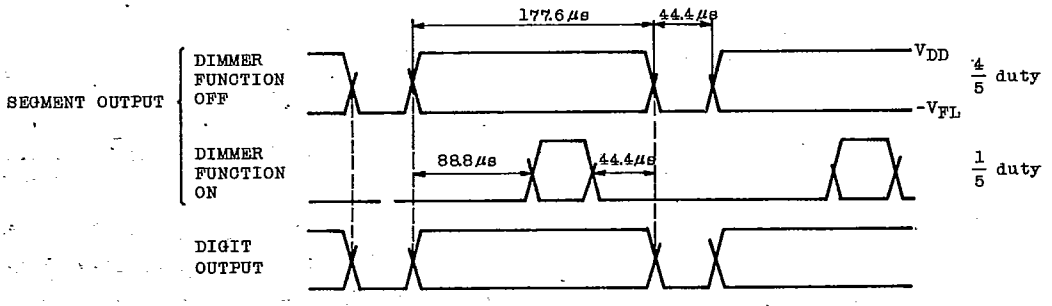
5. Blanking Time and Dimmer Function

For preventing display blur produced at dynamic lighting, a constant blanking time is provided at the timing of changing the display data output.

This blanking time is provided at segment output and the time is equivalent to 1/5 of one digit output. Therefore, segment output waveform is outputted at 4/5 duty for one digit output.

Dimmer function can be realized also by program. When dimmer function is set on, blanking time becomes 4/5 per one digit, and segment output waveform is outputted at 1/5 duty per one digit. By means of this procedure, the brightness of this display can be varied.

The blanking timing chart of dimmer function at on/off is shown the following.



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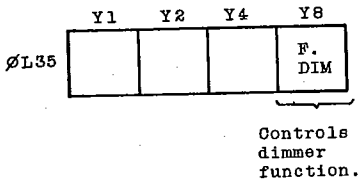
. F.DIM bit (ØKL35)

ON/OFF of dimmer function is controlled by the contents of this bit. This bit is allotted to mark segment port (ØKL35). When data "1" is set to this bit, dimmer function is turned on, and when data "0" is set, dimmer function is turned off.

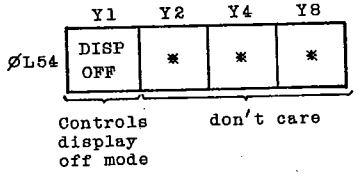
Normal display is performed with dimmer function off mode.



6. Display-off Function

It is possible to stop all the display function and to set the display completely at the condition all lights put off with the contents of DISP OFF internal port. This port is accessed with the execution of KEY output instruction designating [C_N=4] at operand part. When data "1" is set to this port, digit output D_0~D_6 and segment outputs a~h are all fixed at "L" level (-V_{FL} voltage level), and display turns into all-off condition.

When data "0" is set, each output of digit/segment operates normally and dynamic display is performed.



(Note) After system reset and execution of CKSTP instruction, the contents of this port are reset to "0" automatically.

(Note) During display-off mode, since digit output is also fixed at "L" level, key input of key matrix turns out unacceptable.

(Note) During system reset and backup mode (at execution of CKSTP instruction), each output of digit/segment is fixed at "L" level automatically, however, the contents of each port excepting DISP OFF port keep the previous data.

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○ KEY INPUT

4-bit key input terminals (K_0~K_3) exclusively for key matrix are provided. It is possible to use digit output D_0~D_6 signals as key return timing signals, and basically the key switches of $4 \times 7 = 28$ or diode jumper can be connected on key matrix. Four input terminals are of high breakdown voltage structure containing pulldown resistor, and data can be inputted within the range of voltage V_{DD}~V_{FL}. Regarding also key input procedure, the support by hardware is made similarly to the case of V_{FL} driver.

1. Key Input Port (ϕK52)

This is an exclusive key input port of 4-bit latch mode, of which data is read into data memory by the execution of KEY input instruction designating [C_N=2] at operand part.

	Y1	Y2	Y4	Y8
ϕK52	K0	K1	K2	K3

Output of key input latch

When "H" level is inputted to one or more of the terminals, K_0~K_3, at the digit timing assigned by the contents of key return timing select port (ϕL46, ϕL47), K_0~K_3 input data at that time are latched to key input port latch. Key input data is sampled by the strobe signal pulse (ϕSW) located approximatelly at the middle of "H" level period of designated digit output.
When the data "1" is set at KEY RESET bit, strobe signal is produced at the above timing, and when the data of 1H~FH is read into key input port, strobe signal production is stopped and the contents of key input port are kept.
When the data OH is read into key input port, the sampling of key input data by strobe signal is continued after that.

2. Key Status Bit (ϕK45)

Key status bit (K_0, KEY ON) is provided for the purpose of making it possible to monitor on program the present key input status.
The contents of these bits are read into data memory by the execution of IO input instruction designating [C_N=5] at operand part.

	Y1	Y2	Y4	Y8
ϕK45			K0	KEY ON

Key status bit

. KEY ON bit

When data "1" is set to KEY RESET bit, the output of this bit is reset at "0", and when the data of 1H~FH is read into key input port, it is set to "1". This bit output can be used for judging the key input for presence.

(Note) As the data except for OH is read into key input port, whether key input exists or not is checked at all key return timing (D0~D6) and KEY ON bit is set at "1".
Therefore, when the key input is set, KEY ON bit is set at "1" after 35-instruction cycle.
Period of key return timing signal is equivalent to 40-instruction cycle, even in the case key input usually exists, maximum 75-instruction cycle is required for the period in which KEY ON bit is set at "1" after it is reset.

. K0 bit

This bit is output of K0 input terminal condition and can monitor K0 input terminal signal.

3. Key Return Timing Select Port (ϕKL46, ϕKL47) and Key Return Timing Input Port (ϕK50, ϕK51)

Key Return Timing Select Port (ϕL46, ϕL47)

Digit output can be used as key return timing signal. The data inputted to K0~K3 terminals with the timing of digit output signal designated by this port contents is read into key input port. The data inputted with other digit timing can not be read into key port. This is the internal port for selecting, on key matrix, the key input digit line for data reading.
Normally, it is accessed by IO output instruction designating [CN=6 or 7] at operand part (ϕL46, ϕL47). The data presently outputted is read into data memory by the execution of IO input instruction designating [CN=6 or 7] at operand part (ϕK46, ϕK47).
As the relation between each bit of this port and key return timing signal (D0~D6) is one to one, optional key return timing line is able to designate plurality at the same time.

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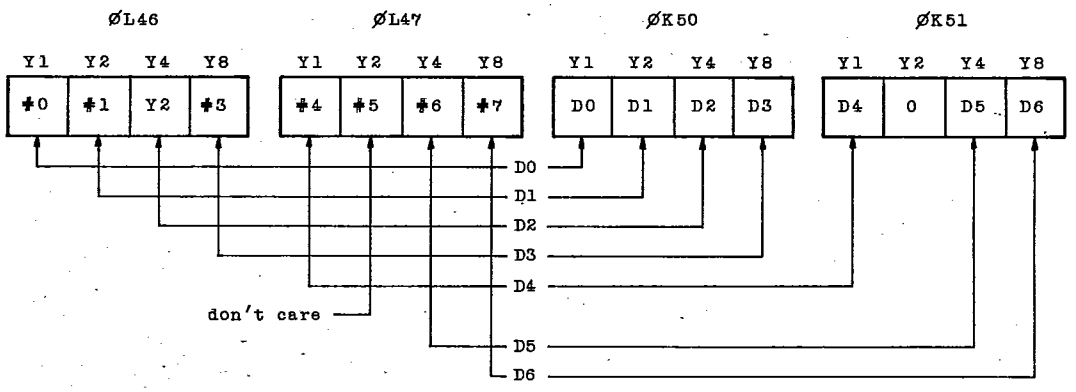
When each bit of this port is set at data "1", the key input of key return timing line corresponding to the bit is able to be read, and when each bit of this port is set at data "0", it is not.

. Key Return Timing Input Port

As the data except for OH is read into key input port, wheter key input exists or not is checked at all key return timing and these results are set at this port. In other words, data "1" is set at the bit corresponding to the key return timing line with being the key input, otherwise "0".

The contents is read into data memory by the execution of KEY input instruction designating [C_N=0 or 1] at operand part.

(Note) The bit corresponding to key return timing line designated as not to read the key input by the contents of the above key return timing select port becomes data "0" automatically.



RELATION BETWEEN EACH BIT AND KEY RETURN TIMING LINE

(Note) When plurality of digit line can be assigned at key return timing select port and key inputs on plural digit lines exist, care must be taken because the digit line of key input data read into key input becomes unable to discrimerate.

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4. KEY RESET Bit (ϕL45)

This is a bit for controlling the strobe signal of key input port latch. This is located in ϕL45 internal port and is accessed by the execution of IO output instruction designating [C_N=5] at operand part. When data "1" is set at this bit, strobe signal pulse is produced with the timing mentioned above, and the reading of data into key input port is started.

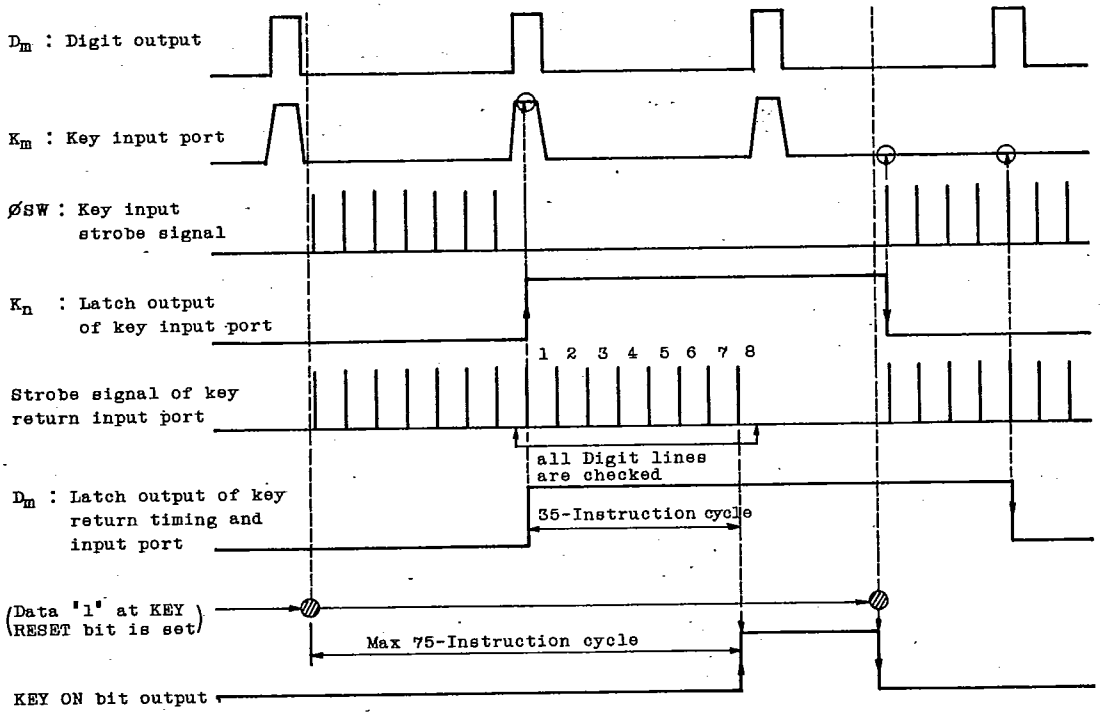
At the same time, output of KEY ON bit is reset at "0". Since WAIT mode is released when KEY ON bit is set at "1", it is also required to set data "1" at KEY RESET bit and to reset KEY ON bit prior to the execution of WAIT instruction.

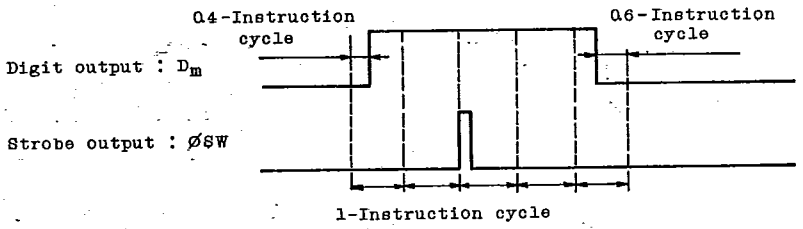
In addition, prior to the execution of WAIT instruction, in order to reset each condition to break WAIT mode, set data "1" at $\overline{\text{INH}}$ STB bit and 2Hz F/F RESET bit (both are bits in ϕL45 port).

	Y1	Y2	Y4	Y8
ϕL45			KEY RESET	

5. Internal Timing Chart During Key Input Operation

Timing is shown below concerning the key input operation for the data to be inputted to key input Kn at timing of digit line Dm, when all digit lines are designated as possible reading key input by key return timing select port. Dm express an optional one among D0~D6, and Kn among K0~K3 respectively.





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. Outline of key input operation

(1) Set the digit line code of key input for reading data into the key return timing select port, and designate digit line.

(2) Next, when data "1" is set to KEY RESET bit, strobe signal pulse is produced and data reading into key input port starts.

(3) When the data of 1H~FH is inputted to key input port with the digit timing designated at (1) (Key input exists), key input data is latched to key input port. When the data of OH is inputted (key input does not exist), the reading of input data is continued.

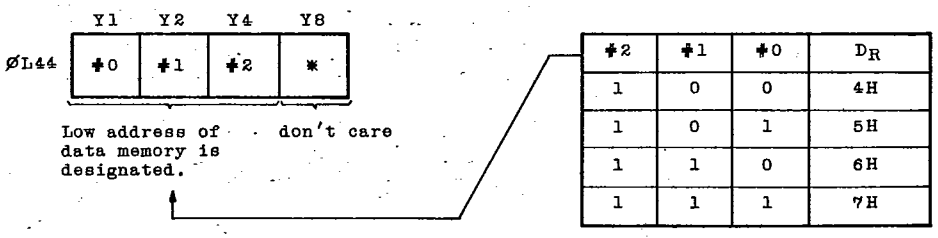
(4) As the data is latched to key input port, whether key input exists or not is checked at all digit lines and these results are set to key return timing select port. KEY ON bit is set at "1" after this operation.
The contents of latched data to key input port and return timing input port are kept stored until data "1" is set to KEY RESET bit and the reading of key input is started again.

○ REGISTER PORT

G-register and data register stated in the explanation of CPU are also treated as one of internal ports.

1. G-register (ØL44)
This is a register to make addressing of low address (D_R=4H~7H) of data memory during the execution of MVGD instruction and MVGS instruction.
This register is accessed by IO output instruction designating [C_N=4] at operand part.

(Note) Contents of this register are effective only during the execution of MVGD instruction and MVGS instruction, and give no effect during the execution of other instructions.



✱2	✱1	✱0	D_R
1	0	0	4H
1	0	1	5H
1	1	0	6H
1	1	1	7H

(Note) It is possible to indirectly designate all low addresses of data memory by setting data OH~7H on G-register, (D_R=OH~7H).

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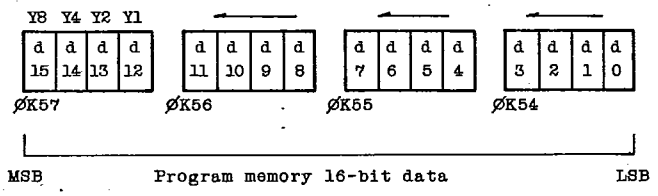
2. Data Register (øK54~øK57)

This is a 16-bit register on which the data of program memory is loaded during the execution of DAL instruction.

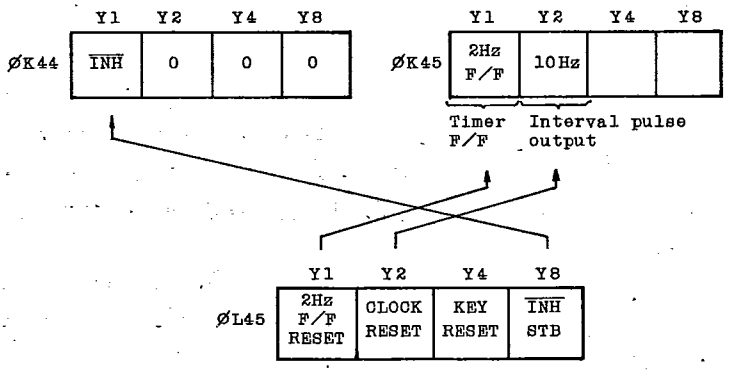
Contents of the register are read into data memory in 4-bit unit by the execution of KEY input instruction designating [C_N=4~7] at operand part.

This register can be used for the decoding of segment, or for the taking of band edge data of radio and of coefficient data during binary-to-BCD conversion.



o INTERNAL CONTROL PORT

Internal control port is used for reading into data memory the inside condition of device which must be known in the execution of program, or for resetting the inside condition of device.



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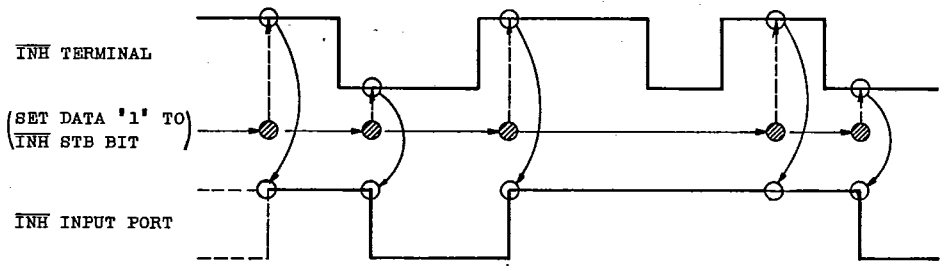
1. $\overline{\text{INH}}$ Input Port (ϕK44)

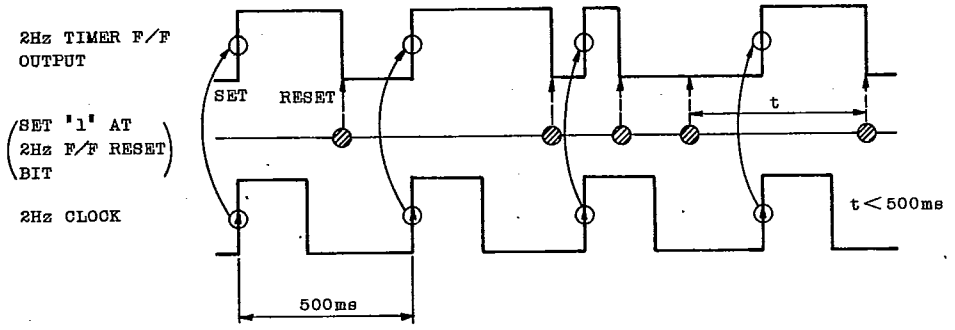
This is an input port having latch mode for inputting the data of $\overline{\text{INH}}$ input terminal. Contents of this port are read into the data memory by executing IO input instruction designating [C_N=4] at operand part. Data "1" and "0" represent radio "ON" mode and radio "OFF" mode, respectively.
This input port has input latch, and by the execution of IO output instruction designating [C_N=5] at operand part, the status of $\overline{\text{INH}}$ terminal is taken into the port every time data "1" is set in $\overline{\text{INH}}$ STB bit.



2. 2Hz Timer F/F (ϕK45)

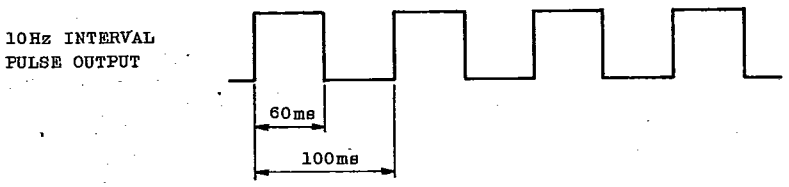
2Hz timer F/F is set by 2Hz (500ms) signal. By the execution of IO output instruction designating [C_N=5] at operand part, this timer is reset by setting data "1" at 2Hz F/F reset bit. This F/F output is read into the data memory by the execution of IO input instruction designating [C_N=5] at operand part.
As timer F/F is automatically set every 500ms, it is usually used counting of clock time.
Since timer F/F is reset only with 2Hz F/F RESET bit, count error rakes place unless data "1" is set at 2Hz F/F RESET bit within 500ms cycle, and correct timer is not obtainable.

(Note) Condition of timer F/F output becomes uncertain at power-on time or after the execution of CKSTP instruction.



3. 10Hz Interval Pulse (ϕK45)

10Hz interval pulse is outputted to 10Hz bit with 100ms period duty 60% pulse. This is read into data memory by the execution of IO input instruction designating [C_N=5] at operand part. This output has no flip-flop and can be used for counting muting time.



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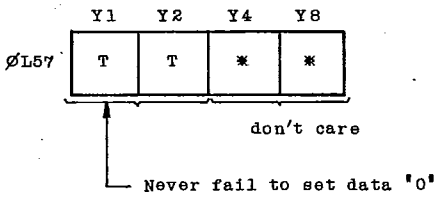
4. Other Control Bit and Port

. CLOCK RESET BIT (ϕL45)

Each time data "1" is set in this bit, clock of below 50Hz is reset (10Hz interval pulse is also reset). This bit is used for adjusting time of clock, accuracy of clock at this time is $\pm^{0}_{0.02}$ second. This bit is also accessed by IO instruction designating [C_N=5] at operand part.

. T Port (ϕL57)

This is an internal port for testing function of device. It is accessed by KEY output instruction designating [C_N=7] at operand part.
Never fail to set data "0" in ordinary program.



○ SERIAL INTERFACE

This is an exclusive serial I/O for strongly controlling external PLL LSI and peripheral option IC group. Serial I/O terminals are four terminals of SO, SI, CK, STB. Data transfer is conducted by connecting these terminals and external devices with four serial bus lines. Extension of function can be easily made by freely connecting peripheral optional ICs on this bus line, depending upon the system. External devices comprises abundant items including PLL LSI, I/O port extending IC, and static display driver.
Serial transfer is conducted by the execution of SIO instruction, the transfer of all data are completed during the execution time of this instruction (88.8μs). In this way, port contained in each external device can simply be treated like the port treated by the execution of other input and output instructions.
Two kinds of serial transfer formats can be selected by program.

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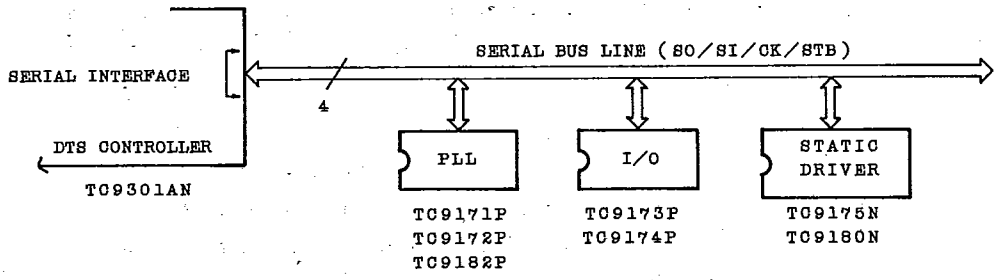
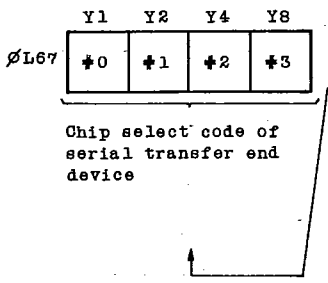


1. Chip Select

As shown above, many external devices can be freely connected with serial bus line. Hence, when conducting serial transfer, first of all it is necessary to select the device of opposite transfer party.

Address of opposite party expressed with 4-bit data called chip select code is assigned to each external device on serial bus line.

By assigning this chip select code, data transfer is carried out with external device corresponding to that code number.



CORRESPONDING TABLE OF EXTERNAL DEVICE CHIP SELECT CODES

CHIP SELECT CODE No.					EXTERNAL DEVICE	
#3	#2	#1	#0		PRODUCTS NAME	FUNCTION
0	0	0	0	0	-	-
0	0	0	1	1	TC9171P/82P	PLL *
0	0	1	0	2	TC9172P	
0	0	1	1	3	TC9173P	I/O port extension use
0	1	0	0	4	TC9174P	Output port extension use
0	1	0	1	5	TC9175N	V_{FL} static display driver
0	1	1	0	6		
0	1	1	1	7	TC9180N	General purpose static display driver (LED/LCD)
1	0	0	0	8		
1	0	0	1	9	TC9189F	Dynamic display driver * (LCD/VFL/LED)
1	0	1	0	A	TC9190N	
1	0	1	1	B	TC9191P	
1	1	0	0	C		

(Note) Chip select code No. of* marked product is same in all cases.

Chip select port (ϕL67) is an internal port for designating this chip select code, and is accessed by SIO output instruction designating [C_N=7] at operand part. Maximum 16 kinds of external devices can be selected by 4-bit chip select code. (In actual case, some device has more than two chip select code numbers.
Example : TC9171P...2, TC9189F...3.)

(Note) When executing SIO instruction, first, designate chip select code of the opposite transfer party device by SIO output instruction.
Since chip select code number once set maintains that code unless designated otherwise, select code need not be designated at each execution of SIO instruction.

(Note) It is impossible to simultaneously connect the devices having the same chip select code on serial bus line.

(Note) After the designation of chip select code number, data is outputted to the port of external device corrsponding to the code number designated at operand part, by the execution of SIO output instruction. Then, by the execution of SIO input instruction, contents of external device port is read into data memory.

(Note) Care must be taken because it is prohibited to program SIO input instruction for the instruction to be executed next to SIO output instruction.
When programing SIO input instruction after SIO output instruction, insert an instruction, for example NOOP instruction, between them.

2. Serial Transfer Format

Two kinds of serial teansfer format can be selected depending upon the contents of SIO NCD port. This internal port is accessed by KEY output instruction designating [C_N=3] at operand part. By the execution of KEY input instruction, the contents of this port are read into data memory.
When data "0" is set at SIO NCD port, serial transfer type of $\overline{\text{NCD}}$ mode is realized. In the case of $\overline{\text{NCD}}$ mode, Code No. of the port designated at the operand part of SIO instruction is serially transferred together with the data.
When data "1" is set, NCD mode is realized. In NCD mode, code No. is not transferred and data alone is sent and received. (C_N value of operand part of SIO instruction becomes don't care).

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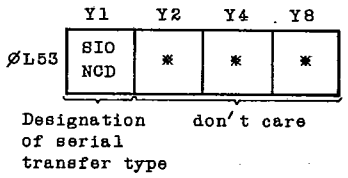
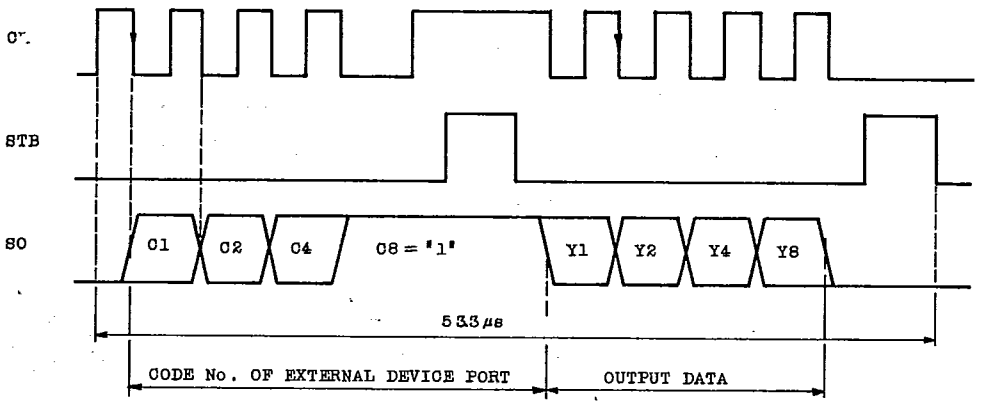
(Note) Serial transfer with the previously denoted external device is all conducted with $\overline{NCD}$ mode.

(Note) In the serial transfer during NCD mode, designation of chip select code is meaningless. That is to say, transferring address can not be selected.



3. Serial Input and Output Timing Chart

. $\overline{NCD}$ mode output timing



In the above indicated timing, code No. (C1~C8 : 4-bit) of destination device port and data (Y1~Y8 : 4-bit) are serially outputted from LSB by the trailing of CK signal.

(Note) During the execution of SIO output instruction ($\overline{NCD}$ mode), C8 bit of code No. is fixed at "1" continually.

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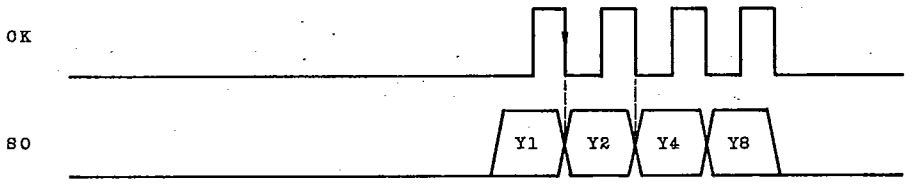
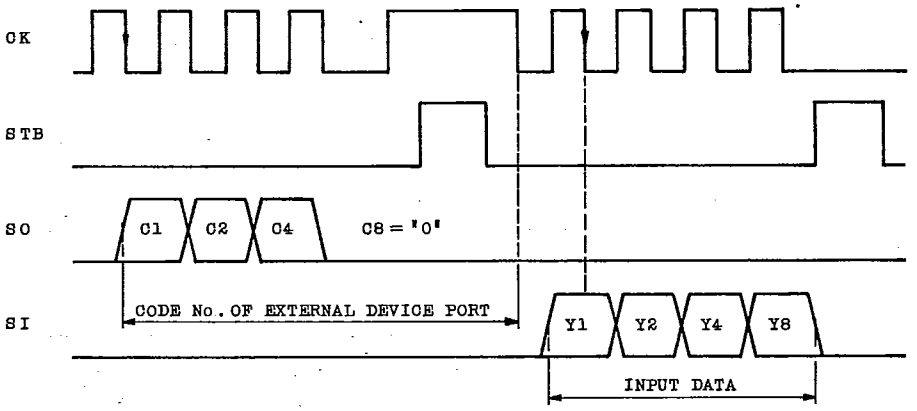
. NCD mode output timing



Serial output of NCD mode becomes 4-bit data alone. STB output is continually fixed at "L" level.

. $\overline{\text{NCD}}$ mode input timing



In the above timing, when code No. (C1~C8 : 4-bit) of input port of destination device is outputted from SO terminal, the contents of that input port (Y1~Y8 : 4-bit) are serially inputted from LSB to SI terminal.
SO data is outputted with trailing of CK signal, while SI data is inputted with trailing of the same signal.

(Note) During the execution of SIO input instruction ($\overline{\text{NCD}}$ mode), C8 bit of code No. is fixed at "0" at all times.

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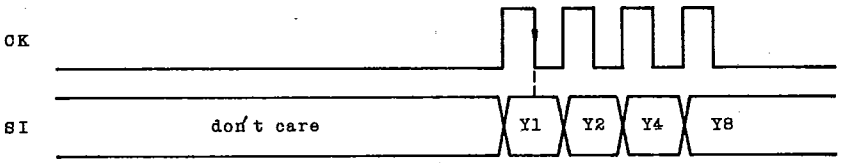
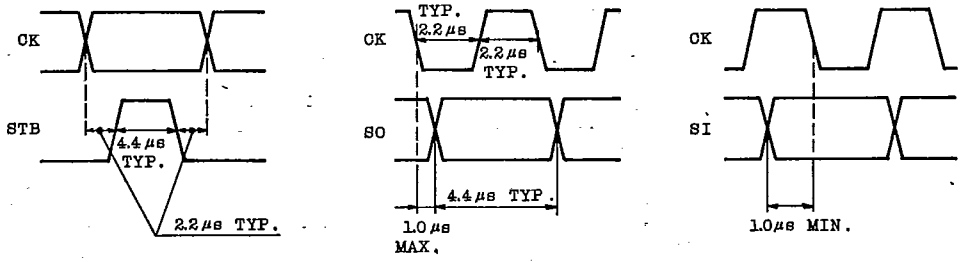
. NCD mode input timing



During serial inputting of NCD mode, STB output and SO output are always fixed at "L" level. SI data is inputted by the trailing CK signal.

4. Serial Timing Pulse Width

Pulse width of each timing signal is shown below.



○ APPLICATION TO EVALUATOR CHIP

When "H" level is supplied to TEST terminal, device operates as evaluator chip, and function evaluation of developing program can be made by utilizing external simulation board and EPROM (test mode). In the test mode, the device operates by the program written in EPROM, irrespective of the contents of program memory in device. At this time, since digit outputs (D0~D6) are changed to controlling input and output terminal of simulation board, actual D0~D6 digit outputs are outputted from the simulation board side.

For system reset in test mode, $\overline{INT}$ input is employed.

In the following is shown the connection diagram of device and simulation board when the unit is used as an evaluator chip.

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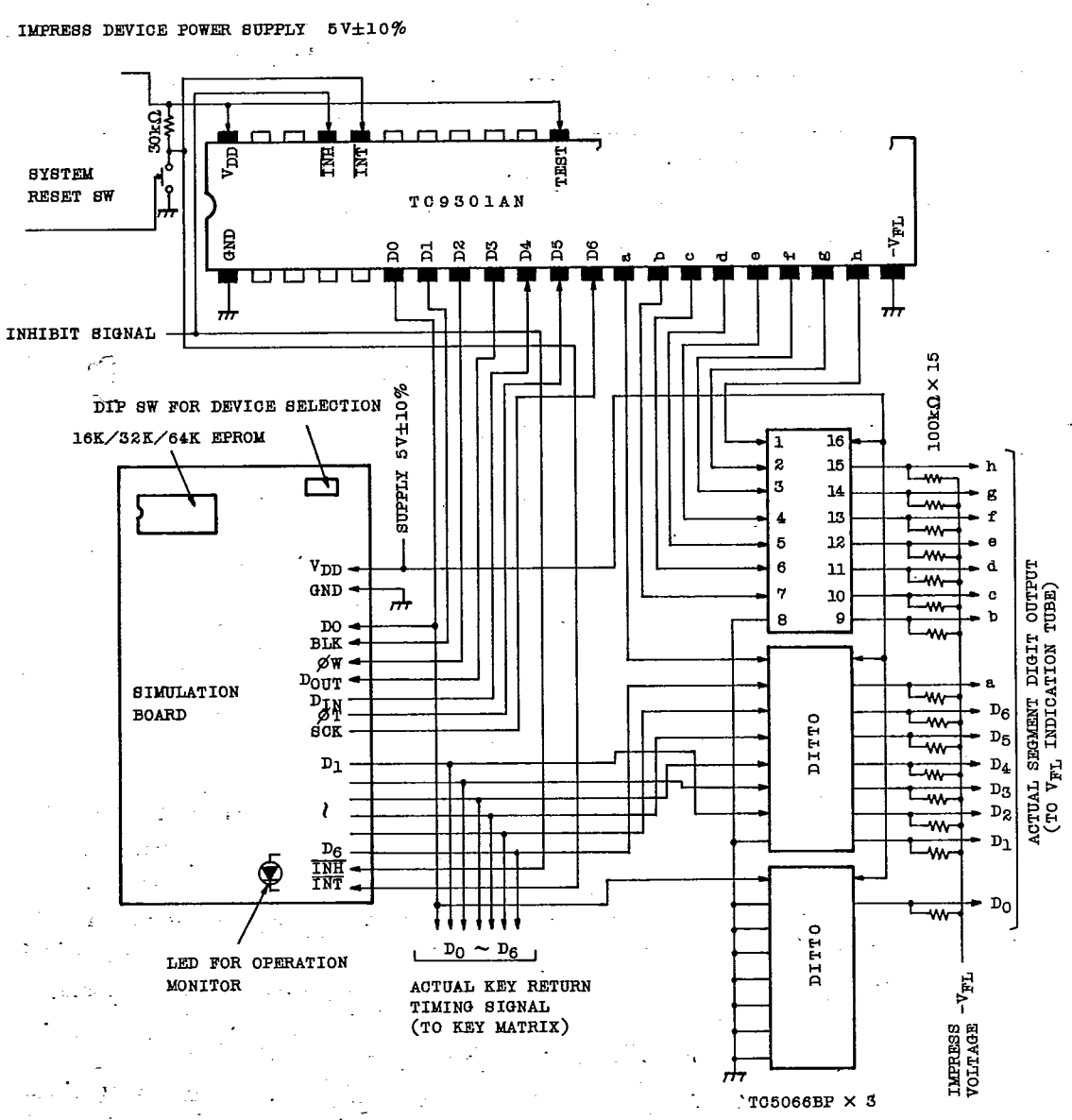

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(Note) Select the device TC9301AN by a dip switch on the simulation board.

(Note) Supply 5V±10% voltage on the device and simulation board even during backup mode. In the test mode, it is impossible to reduce the supply voltage of the device to 2V.

(Note) In backup mode (execution of CKSTP instruction), operation monitor LED on simulation board turns off.

(Note) Each terminal of the device other than that indicated above can be used in usual way.

(Note) Use $-V_{FL}$ terminal of device at GND level. Therefore, in order to drive V_{FL} indication tube, high breakdown voltage buffer (TC5066BP) is necessary to be provided to each output of digit, segment as shown in the above diagram.