TC9302AF

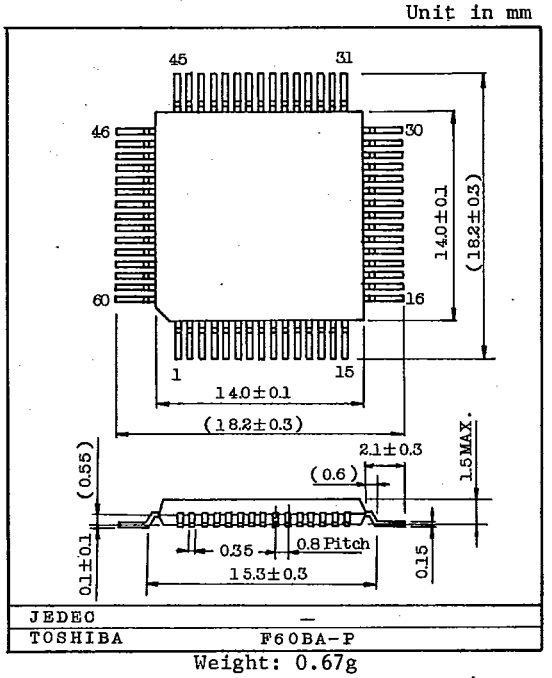
DTS MICRO CONTROLLER CONTAINING LCD DRIVER

The TC9302AF is 4 bit CMOS micro controller for digital tuning system use having built-in LCD driver.

CPU has 4 bit parallel addition and subtraction (AI, SI instructions, etc.), logical operation (OR, AN instructions, etc.), plural bit judge and comparison instruction (TM, SL instructions, etc.), and timer function.

The equipment consists of 60 pin, mini-flat package, and has abundant I/O port and exclusive key input port controlled by powerful input and output instruction (IO, KEY instruction, etc.), and serial bus control function (SIO instruction) to control forcibly external PLL LSI and peripheral ICs. Further, it contains 4 bit A/D converter, and is capable of measuring electric field strength by inputting signal meter ouput.

Unit in mm



Weight: 0.67g

Also, it has abundant exclusive LCD output terminal of 1/2 duty, 1/2 bias driving, and exclusive terminal to output eight kinds of reference frequency signal to be supplied to PLL LSI

FEATURES

- 4 bit micro controller for digital tuning system use.
- Built-in LCD driver (1/2 duty, 1/2 bias driving, driving frequency: 50 Hz)
- 5V ±10% single power supply. CMOS structure and low power dissipation.
- Back-up of data memory (RAM) and each port is easily made (by $\overline{INH}$ terminal).
- Program memory (ROM) : 16 bit × 1024 steps
- Data memory (RAM : 4 bit × 128 words
- Powerful instruction set of 62 kinds (all one word instruction).
- Instruction executing time 44.4 μs (7.2 MHz crystal connection).
- Abundant addition and subtraction instructions (addition instructions 12 kinds, subtraction instructions 12 kinds).
- Powerful compound judge statement (TMTR, TMFR, TMT, TMF instructions).

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- Data transfer in same low address is possible.
- Indirect transfer of register is possible. (MVRD, MVRS, MVGD, MVGS instructions)
- 16 powerful general registers (arranged in RAM).
- Stock level : 1 level
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instruction can be freely made among 1024 steps.
- It is possible to freely refer to the content,16 bits,of optional address within 1024 steps in program memory (ROM), (DAL instruction).
- Contains powerful exclusive serial bus control function.
- Powerful input and output instruction (IO, KEY, SIO instructions).
- Exclusive input port (K0 ∿ K3) for key input use, and abundant 29 exclusive LCD driving terminals.
- Abundant 14 I/O port (port capable of setting input or output in 1 bit unit : 6, exclusive output port : 8).
- Clock stop is possible by instruction. (During CKSTP instruction : Supply current, 1 μA or below).
- 2 Hz timer F/F and 10 Hz interval pulse output are contained (Internal port for time base use).
- Built-in 4 bit A/D converter
- Reference frequencies of eight kinds to be supplied to PLL LSI can be selected depending upon program. (1 KHz, 5 KHz, 9 KHz, 10 KHz, 12.5 KHz, 60 KHz, 100KHz).

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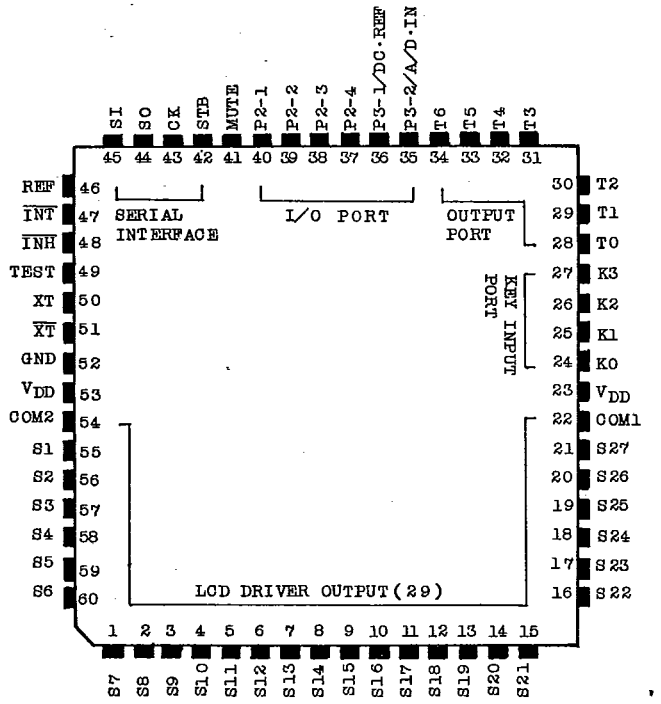
MAXIMUM RATINGS

(Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ∿ 6.0	V
Input Voltage	V_{IN}	-0.3 ∿ V_{DD}+0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{opr}	-30 ∿ 75	°C
Storage Temperature	T_{stg}	-55 ∿ 125	°C

TERMINAL CONNECTION DIAGRAM



TOP VIEW MINI FP-60PIN

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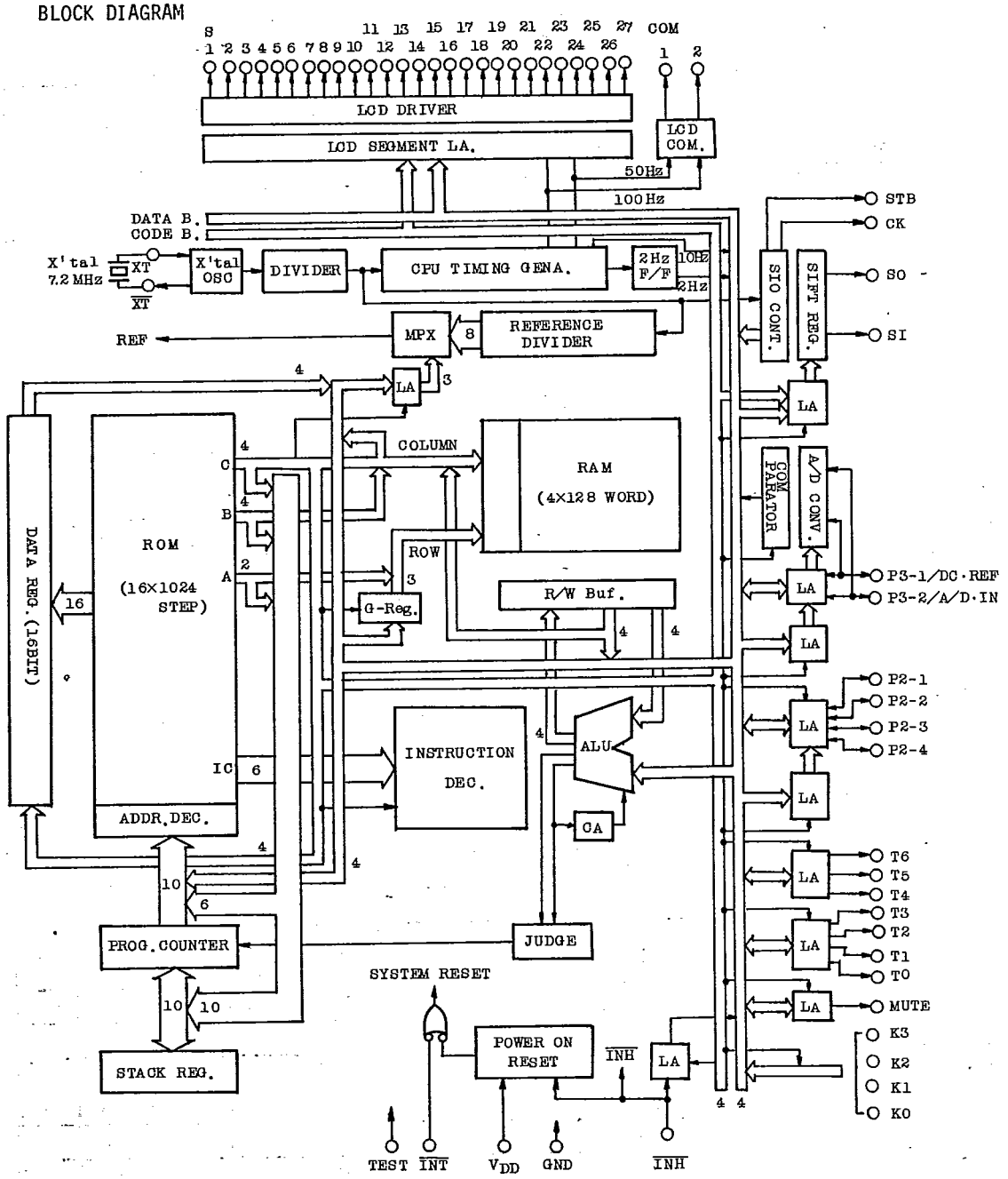
BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Except otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage Range	V_{DD}	*	4.5	5.0	5.5	V
Memory Holding Voltage Range	V_{HD}	Crystal Oscillation stops *	2.0	∿	5.5	V
Operating Supply Current	I_{DD}	Normal Operation (Encluding output current)		1.0	3.0	mA
Memory Holding Supply Current	I_{HD1}	V_{DD}=5V Crystal Oscillation stops	-	0.07	1.0	μA
	I_{HD2}	V_{DD}=2V Crystal Oscillation stops	-	-	0.5	μA
Crystal Oscillation Frequency	f_{XT}	*	-	7.2	-	MHz
LCD Common Output (COM1, COM2)						
High Level Output Current	I_{OH1}	V_{OH}=4.5V	-200	-500	-	μA
Low Level Output Current	I_{OL1}	V_{OL}=0.5V	200	500	-	μA
1/2 Bias Voltage	V_{BS}		2.40	2.50	2.60	V
LCD Segment Output (S1 ∿ S27)						
High Level Output Current	I_{OH2}	V_{OH}=4.5V	-50	-160	-	μA
Low Level Output Current	I_{OL2}	V_{OL}=0.5V	50	160	-	μA
MUTE, T0 ∿ T6 Port						
High Level Output Current	I_{OH3}	V_{OH}=4.5V	-0.7	-1.7	-	mA
Low Level Output Current	I_{OL3}	V_{OL}=0.5V	0.5	1.2	-	mA
REF Output, P2-1 ∿-4, P3-1 ∿-2 Port						
High Level Output Current	I_{OH4}	V_{OH}=4.0V	-0.6	-1.4	-	mA
Low Level Output Current	I_{OL4}	V_{OL}=1.0V	0.6	1.4	-	mA
SO, CK, STB Output						
High Level Output Current	I_{OH5}	V_{OH}=4.0V	-1.0	-2.0	-	mA
Low Level Output Current	I_{OL5}	V_{OL}=1.0V	1.0	2.0	-	mA
Key Input Port (K0 ∿ K3)						
High Level Input Voltage	V_{IH1}		3.5	∿	5.0	V
Low Level Input Voltage	V_{IL1}		0	∿	1.5	V
Pulldown Resistance	R_{IN1}		50	100	150	kΩ

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CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SI, $\overline{INH}$, $\overline{INT}$, P2-1 ∿ -4, P3-1 ∿-2 Port						
High Level Input Voltage($\overline{INH}$)	V_{IH2}		4.3	∿	5.0	V
Low Level Input Voltage ($\overline{INH}$)	V_{IL2}		0	∿	2.7	V
High Level Input Voltage(Others)	V_{IH1}		3.5	∿	5.0	V
Low Level Input Voltage(Others)	V_{IL1}		0	∿	1.5	V
High Level Input Leak Current	I_{IH}	V_{IH}=5.0V	-	-	1.0	μA
Low Level Input Leak Current	I_{IL}	V_{IL}=0V	-	-	-1.0	μA
A/D Converter (DC · REF, A/D IN)						
DC·REF Built-in Ladder Resistance	$\overline{RL}$		30	50	80	kΩ
DC·REF Input Voltage Range	V_{REF}		1.0	∿	3.0	V
Resolution	V_{RES}		-	$V_{REF}/16$	-	V
Others						
XT Input Feedback Resistance	R_f		250	500	1000	kΩ
Test Input Pulldown Resistance	R_{IN2}		15	30	60	kΩ

Note: *Marked items are guaranteed within a range of V_{DD} = 4.5 ∿ 5.5V, Ta = -30 ∿ 75°C

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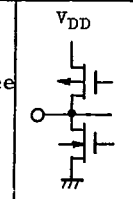
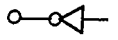
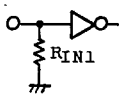
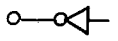
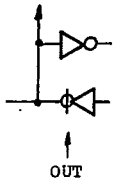
FUNCTIONS OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
22 54	COM1 COM2	LCD Common Output	This is a common signal output terminal to LCD. Indication of maximum 54 segments is possible with matrix made with S1∿S27. To this terminal are outputted three value levels of V_{DD}, $1/2V_{DD}$, GND, at intervals of 50 Hz. (Note) During system reset and CKSTP instruction execution, output is automatically fixed at 'L' level.	
55 ∿ 60 1 ∿ 21	S1 ∿ S6 S7 ∿ S27	LCD Segment Output	This is a segment signal output terminal to LCD. Indication of maximum 54 segments is possible with matrix mode with COM1, COM2. Data is outputted to these terminals by the execution of SEG instruction (COM1 system) and MARK instruction (COM2 system). Decoding of segment can be done by making that decode pattern within ROM territory and executing it by using DAL instruction. (Note) During system reset and CKSTP instruction execution, output is automatically fixed at 'L' level.	
24 ∿ 27	K0 ∿ K3	Key Input Port	This is a 4 bit input port for inputting key matrix. By executing KEY instruction designating this port at operand port, data of these terminals is read in RAM. All terminals contain pull-down resistance. Usually, output port of T0∿T6 is used for key return timing signal output.	
28 ∿ 34	T0 ∿ T6	Key Timing Output Port	This is an output port of 4 bit (T0∿T3) and 3 bit (T4∿T6). Usually, it is used as key return timing signal output of key matrix.	
35 36	P3-2 / A/D IN P3-1 DC REF	I/O Port 3 A-D /Analog Voltage Input /Reference Voltage Input	This is a two bit I/O port. This port is capable of making input and output assignment for each bit, and the assignment is made with the content of internal port called PORT-3 I/O CONTROL. This terminal combines analog input of built-in 4 bit A/D Converter. Change-over to A/D Converter input is also controlled by the content of PORT-3 I/O CONTROL port. The built-in A/D converter is of successive comparison system by program, P3-1 being reference voltage input, and P3-2 analog comparison voltage input.	To A/D Converter 

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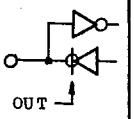
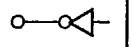
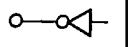
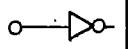
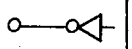
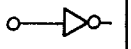
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
37 ~ 40	P2-4 ~ P2-1	I/O Port 2	This is a 4 bit I/O port. This port is capable of designating input and output of each bit, and the designation is performed with the content of internal port called PORT-2 I/O CONTROL.	
41	MUTE	Muting Signal Output Port	This is a 1 bit output port. It is usually used as a muting control signal output. (Note) When $\overline{INH}$ input is changing as 'H' ↔ 'L', the output is automatically set at 'H' level.	
42	STB	Strobe Pulse Output	Serial interface. By executing SIO instruction, external PLL, LSI and peripheral optional ICs can be controlled powerfully. As for serial transfer system, two kinds of $\overline{NCD}$/NCD mode can be selected by program.	
43	CK	Serial Clock Output		
44	SO	Serial data Output		
45	SI	Serial data Input		
46	REF	Reference Frequency Signal Output	This is an output terminal of reference frequency signal supplied to PLL, LSI. It is possible to select eight kinds of reference frequency signal, 1 KHz, 5 KHz, 9 KHz, 10 KHz, 12.5 KHz, 25 KHz, 50 KHz, 100 KHz, depending upon the program. (Note) When $\overline{INH}$ input is at 'L' level, output is automatically fixed at 'L' level.	
47	$\overline{INT}$	Initializing Input	This is a system reset signal input terminal of the device. While $\overline{INT}$ is at 'L' level, reset is applied, and when it becomes 'H' level, the program starts from zero address. When the voltage, OV → 4.5V, is supplied to V_{DD} terminal, system reset is applied (power on reset), and so this terminal usually is fixed at 'H' level when used. (Note) After system reset, I/O port is set at input mode, but the output port must be initialized by program according to your use, as its output condition is indefinite.	

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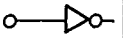
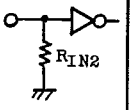
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
48	$\overline{INH}$	Inhibit Input	This is a pulsing signal input port of radio mode. It judges as radio on mode at 'H' level input and radio off mode at 'L' level input. When this terminal is at 'L' level, REF output is automatically fixed at 'L' level. Further, if CKSTP instruction is used in the program and this CKSTP instruction is executed while $\overline{INH}$ is at 'L' level, the internal clock generator and CPU stop their operations, and memory back up condition can be realized at low current consumption (less than 1 μA). At this time, all output terminals (indicated output, output port, etc.) are fixed to 'L' level, automatically. (Note) CKSTP instruction is effective when $\overline{INH}$ is at 'L' level, and makes the same operation as NOOP instruction if executed when $\overline{INH}$ is at 'H'level.	
49	TEST	Test Mode Control Input	This is an input terminal for a test mode control. It is brought to test mode with 'H' level input and normal operation with 'L' level or NC condition. It contains pull down resistance, and usually fixed at NC or 'L' level when used. In the test mode, the device operates as evaluator chip, and program evaluation at EPROM base is possible when combined with external simulation board.	
50 51	XT $\overline{XT}$	Crystal Oscillation Terminal	This is a connecting terminal of crystal oscillator. 7.2 MHz crystal is connected. Oscillation is automatically stoppes during the execution of CKSTP instruction.	—
52	GND	Ground Terminal	This is a device ground terminal.	—
23 53	V_{DD}	Power Supply Terminal	This is a power supply terminal of the device. Voltage of 5V ±10% is impressed in the normal operation. Under back up condition (during the execution of CKSTP instruction), voltage can be lowered down to 2V. When voltage, OV → 4.5V, is supplied to this terminal, system reset is applied to the device, and the program starts from zero address. (power on reset). (Note) Carry out power on reset from the condition of $\overline{INH}$='L' level. (Note) As the content of each port (output port, internal port, etc.) is indefinite at the time of closing of supply power, initialization by program must be made, according to your use.	—

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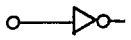
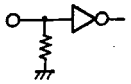
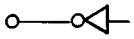
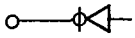
(Supplement)


CMOS input


Built-in pulldown resistance
CMOS input


CMOS output


Clocked gate type
CMOS output

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EXPLANATION OF OPERATION

o CPU

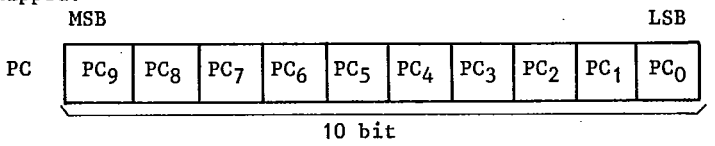
CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, data register, carry F/F and judging circuit.

1. Program Counter (PC)

Program counter is a device to address program memory (ROM), and is composed of 10 bits binary up counter. This is cleared by system reset, and the program starts from zero address.

Usually, increment is made one by one everytime the one instruction is executed, but when JUMP instruction, or CAL instruction is executed, the address designated at operand port of that instruction is loaded.

Further, when the instruction (AIS, SLT, TMT, RNS instructions, etc.) having skip function, is executed, two increment of program counter is made if the result is the condition to be skipped, and the succeeding instruction is skipped.



2. Stack Register (STACK)

This is a register composed of 1 × 10 bits.
During the execution of sub-routine call instruction, the value obtained by adding +1 to the content of program counter, namely return address, is housed. The content of stack register is loaded on the program counter by the execution of return instruction (RN, RNS instructions).

This stack level is 1 level, and nesting is 1 level.

3. ALU

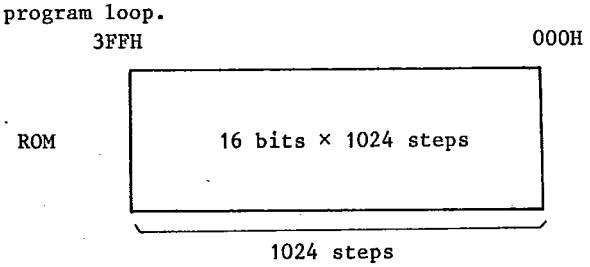
ALU has binary 4 bit parallel addition and subtraction, logical operation, comparison and plural bit judge functions. This CPU has no accumulator, and all operations directly treat the content of data memory.

4. Program Memory (ROM)

Program memory is composed of 16 bit × 1024 steps, of 000H ∿ 3FFH address. Program memory has no concept of page or field, and JUMP instruction and CAL instruction can be freely used among 1024 steps.

Further, it is possible to use optional address of program memory as data area, and its content,16 bits,can be loaded to the data register by executing DAL instruction.

(Note) Provide the data area in the program memory at the address outside the program loop.



5. Data Memory (RAM)

Data memory is composed of 4 bit × 128 words and used for storing data. This 128 words are expressed with row address (3 bit) and column address (4 bit). 64 words (row address = 4H ∿ 7H address) among the data memory are indirect addressing by G-register. For this reason, when carrying out data processing within this territory, it is necessary to designate row address by G-register beforehand.

00H ∿ 0FH address in the data memory is called general register, and can be used only by designating column address (4 bit). These 16 general registers can be used for operation and transfer between data memories. Further, it can also be used as ordinary data memory.

(Note) The column address (4 bit) to designate general register becomes register number of the general register.

(Note) It is also possible to indirectly designate all (0H ∿ 7H address) row address by G-register.

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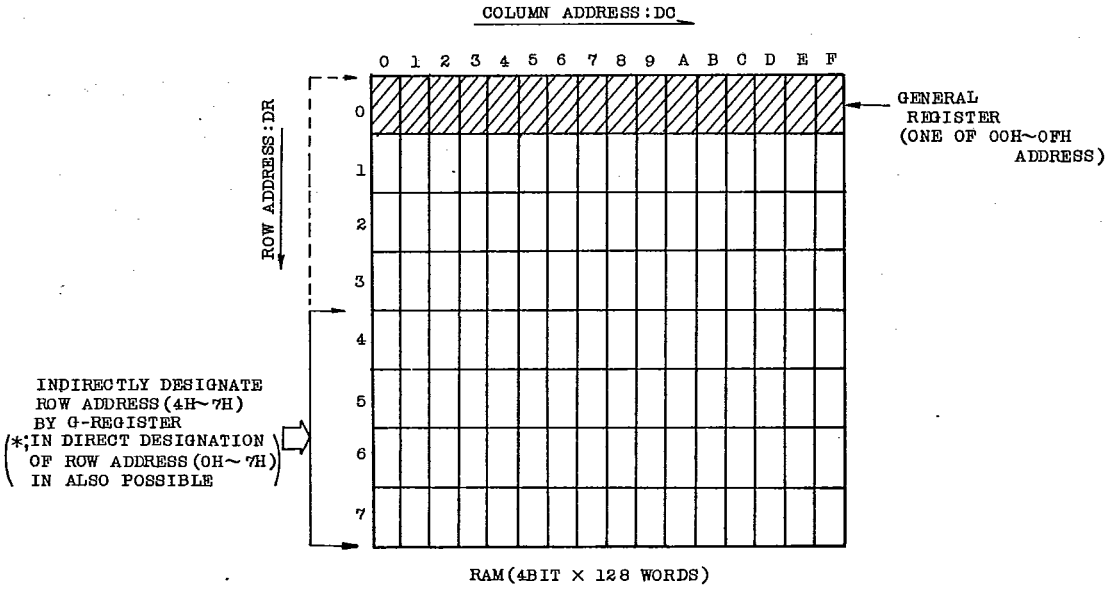

6. G-register (G-REG.)

G-register is a 3 bit register for addressing 64 word row address (DR= 4H ∿ 7H address) of data memory. Content of this register is effective when executing MVGD instruction, MVGS instruction, and is not related with the execution of other instructions.

This register is treated as one of the port, and its content is set by the execution of IO instruction among input and output instructions.

(refer to register port item 1)

7. Data Register (DATA REG)

This is a register composed of 1 × 16 bits. In this register, 16 bit data of optional address among the program memory is loaded during executing of DAL instruction. This register is treated as one of the port, and when key instruction among input and output instructions is executed, its content is read in the data memory in 4 bit unit.

(refer to register port item 2)

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8. Carry F/F (C·F/F)

This is set when carry or borrow is produced as a result of executing operational instruction, and is reset when it is not produced. Content of carry F/F changes only when addition and subtraction instruction is executed, and does not change during the execution of other instructions.

9. Judge Circuit (J)

When skip function instruction is executed, this circuit judges its skip condition. When skip condition is satisfied, this circuit makes increment of two program counters, and skips the succeeding instruction.

It is provided with 29 kings of instructions having abundant skip function. (Refer to Item, 11, list of explanations of instruction function and operations, * marked instruction).

10. Instruction Set List

62 kinds of instruction set are included, all of which consisting of one word instruction. These instructions are expressed with 6 bit instruction code.

Higher rank 2 bits / Lower rank: 4 bits		00	01	10	11
		0	1	2	3
0000	0	AI M,I	AD r,M	LD r,M	SLTI M,I
0001	1	AIS M,I	ADS r,M	ST M,r	SGEI M,I
0010	2	AIN M,I	ADN r,M	MVRD r,M	SEQI M,I
0011	3	SI M,I	SU r,M	MVRS M,r	SNEI M,I
0100	4	SIS M,I	SUS r,M	MVSR M_1,M_2	SLT r,M
0101	5	SIN M,I	SUN r,M	MVIM M,I	SGE r,M
0110	6	CAL ADDR1	ORR r,M	MVGD r,M	SEQ r,M
0111	7	—	ANDR r,M	MVGS M,r	SNE r,M
1000	8	AIC M,I	AC r,M	PLL M,C	TMTR r,M
1001	9	AICS M,I	ACS r,M	SEG M,C	TMFR r,M
1010	A	AICN M,I	ACN r,M	AMRK M,C	TMT M,N
1011	B	SIB M,I	SB r,M	IO M,C	TMF M,N
1100	C	SIBS M,I	SBS r,M	KEY M,C	DAL $ADDR_2$,r
1101	D	SIBN M,I	SBN r,M	SIO M,C	WAIT
1110	E	JUMP ADDR1	ORIM M,I	RN	CKSTP
1111	F	—	ANIM M,I	RNS	NOOP

11. Explanation List of Function and Operation of Instructions

(Explanation of Symbols)

M : Data memory address
, Normally, one of 00H ∿ 3FH address of data memory
. One of 00H ∿ 7FH address during the execution of MVGD instruction and MVGS instruction (G-register is used).

r : General register
. One of 00H ∿ 0FH address of data memory

PC : Program counter (10 bit)

STACK : Stack register (10 bit)

G : G-register (3 bit)

DATA : Data register (16 bit)

I : Immediate data (4 bit)

N : Bit position (4 bit)

— : All '0'

C : Cord No. of port (4 bit)

CN : Lower rank 3 bit of port code No.

RN : General register No. (4 bit)

ADDR1 : Program memory address (10 bit)

ADDR2 : Higher rank 6 bit of program memory address

Ca : Carry

b : Borrow

PLL : Port treated during the execution of PLL instruction

SEG : Port treated during the execution of SEG instruction

MARK : Port treated during the execution of MARK instruction

IO : Port treated during the execution of IO instruction

KEY : Port treated during the execution of KEY instruction

SIO : Port treated during the execution of SIO instruction

( ) : Register or data memory content

( )c : Content of port indicated by code No. C. (4 bit)

[ ] : Content of data memory indicated by the content of register or data memory

[ ]p : Content of program memory (16 bit)

IC : Instruction code (6 bit)

* : Instruction having skip function

DC : Data memory column address (4 bit)

DR : Data memory row address (2 bit)

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Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	·Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
Addition Instruction	AI M,I		Add immediate data to memory	M ← (M) + I	000000	D_R	D_C	I
	AIS M,I	*	Add immediate data to memory, then skip if carry	M ← (M) + I Skip if carry	000001	D_R	D_C	I
	AIN M,I	*	Add immediate data to memory, then skip if not carry	M ← (M) + I Skip if not carry	000010	D_R	D_C	I
	AIC M,I		Add immediate data to memory with carry	M ← (M) + I + ca	001000	D_R	D_C	I
	AICS M,I	*	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + ca Skip if carry	001001	D_R	D_C	I
	AICN M,I	*	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + ca Skip if not carry	001010	D_R	D_C	I
	AD r,M	*	Add memory to general register	r ← (r) + (M)	010000	D_R	D_C	R_N
	ADS r,M	*	Add memory to general register, then skip if carry	r ← (r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN r,M	*	Add memory to general register, then skip if not carry	r ← (r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC r,M	*	Add memory to general register with carry	r ← (r) + (M) + ca	011000	D_R	D_C	R_N
	ACS r,M	*	Add memory to general register with carry, then skip if carry	r ← (r) + (M) + ca Skip if carry	011001	D_R	D_C	R_N
	ACN r,M	*	Add memory to general register with carry, then skip if not carry	r ← (r) + (M) + ca Skip if not carry	011010	D_R	D_C	R_N

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Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
Subtraction Instruction	SI M,I		Subtract immediate data from memory	M ← (M) - I	000011	D_R	D_C	I
	SIS M,I	*	Subtract immediate data from memory, then skip if borrow	M ← (M) - I Skip if borrow	000100	D_R	D_C	I
	SIN M,I	*	Subtract immediate data from memory, then skip if not borrow	M ← (M) - I Skip if not borrow	000101	D_R	D_C	I
	SIB M,I		Subtract immediate data from memory with borrow	M ← (M) - I - b	001011	D_R	D_C	I
	SIBS M,I	*	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) - I - b Skip if borrow	001100	D_R	D_C	I
	SIBN M,I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) - I - b Skip if not borrow	001101	D_R	D_C	I
	SU r,M		Subtract memory from general register	r ← (r) - (M)	010011	D_R	D_C	R_N
	SUS r,M	*	Subtract memory from general register, then skip if borrow	r ← (r) - (M) Skip if borrow	010100	D_R	D_C	R_N
	SUN r,M	*	Subtract memory from general register then skip if not borrow	r ← (r) - (M) Skip if not borrow	010101	D_R	D_C	R_N
	SB r,M		Subtract memory from general register with borrow	r ← (r) - (M) - b	011011	D_R	D_C	R_N
	SBS r,M	*	Subtract memory from general register with borrow, then skip if borrow	r ← (r) - (M) - b Skip if borrow	011100	D_R	D_C	R_N

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Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
Comparison Instruction	SBN r,M	*	Subtract memory from general register with borrow, then skip if not borrow	r ← (r) − (M) − b Skip if not borrow	011101	D_R	D_C	R_N
	SLTI M,I	*	Skip if memory is less-than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI M,I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI M,I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI M,I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SLT r,M	*	Skip if general register is less than memory	Skip if (r) < (M)	110100	D_R	D_C	R_N
	SGE r,M	*	Skip if general register is greater than or equal to memory	Skip if (r) ≧ (M)	110101	D_R	D_C	R_N
	SEQ r,M	*	Skip if general register is equal to memory	Skip if (r) = (M)	110110	D_R	D_C	R_N
	SNE r,M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	110111	D_R	D_C	R_N
Transfer Instruction	LD r,M	*	Load memory to general register	r ← (M)	100000	D_R	D_C	R_N
	ST M,r	*	Store general register to memory	M ← (r)	100001	D_R	D_C	R_N
	MVRD r,M		Move memory to destination memory referring to general register in the same row	[D , (r)] ← (M)	100010	D_R	D_C	R_N

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Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)	
Transfer Instruction	MVRS M,r		Move source memory referring to general register to memory in the same row	M ← [D_R, (r)]	100011	D_R	D_C	R_N	
	MVSR M1,M2		Move memory to memory in the same row	(D_R,D_{C1}) ← (D_R,D_{C2})	100100	D_R	D_C	D_{C2}	
	MVIM M,I		Move immediate data to memory	M ← I	100101	D_R	D_C	I	
	MVGD r,M		Move memory to destination memory referring to G-register and general register	[(G),(r)] ← (M)	100110	D_R	D_C	R_N	
	MVGS M,r		Move source memory referring to G-register and general register to memory	M ← [(G),(r)]	100111	D_R	D_C	R_N	
Input and Output Instruction	PLL M,C		Input PLL port data to memory	M ← [PLL]$_C$	101000	D_R	D_C	0	C_N
			Output contents of memory to PLL port	[PLL]$_C$ ← (M)		D_R	D_C	1	C_N
	SEG M,C		Input SEG port data to memory	M ← [SEG]$_C$	101001	D_R	D_C	0	C_N
			Output contents of memory to SEG port	[SEG]$_C$ ← (M)		D_R	D_C	1	C_N
	MARK M,C		Input MARK port data to memory	M ← [MARK]$_C$	101010	D_R	D_C	0	C_N
			Output contents of memory to MARK port	[MARK]$_C$ ← (M)		D_R	D_C	1	C_N
	IO M,C		Input IO port data to memory	M ← [IO]$_C$	101011	D_R	D_C	0	C_N
			Output contents of memory to IO port	[IO]$_C$ ← (M)		D_R	D_C	1	C_N

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Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
Input and Output Instruction	KEY M,C		Input KEY port data to memory	M ← KEY C	101100	D_R	D_C	0 C_N
			Output contents of memory to KEY port	KEY C ← (M)		D_R	D_C	1 C_N
	SIO M,C		Serial input port data of external device to memory	M ← [SIO]C	101101	D_R	D_C	0 C_N
			Serial output contents of memory to port of external device	[SIO]C ← (M)		D_R	D_C	1 C_N
Logical Operation Instruction	ORR r,M		Logical OR of general register and memory	r ← (r) ∨ (M)	010110	D_R	D_C	R_N
	ANDR r,M		Logical AND of general register and memory	r ← (r) ∧ (M)	010111	D_R	D_C	R_N
	ORIM M,I		Logical OR of memory and immediate data	M ← (M) ∨ I	011110	D_R	D_C	I
	ANIM M,I		Logical AND of memory and immediate data	M ← (M) ∧ I	011111	D_R	D_C	I
Bit Judge Instruction	TMTR r,M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r[N(M)] = all '1'	111000	D_R	D_C	R_N
	TMFR r,M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r[N(M)] = all '0'	111001	D_R	D_C	R_N
	TMT M,N	*	Test memory bits, then skip if all bits specified are true	Skip if M(N) = all '1'	111010	D_R	D_C	N
	TMF M,N	*	Test memory bits, then skip if all bits specified are false	Skip if M(N) = all '0'	111011	D_R	D_C	N

Inst. Gr.	Mnemonic	Skip Func.	Explanation of Function	Explanation of Operation	Machine Language (16 bit) IC (6 bit)	A (2 bit)	B (4 bit)	C (4 bit)
Subroutine Instruction	CAL $ADDR_1$		Call subroutine	STACK ← (PC) + 1 and PC ← $ADDR_1$	000110	$ADDR_1$ (10 bit)		
	RN		Return to main routine	PC ← (STACK)	101110	—	—	—
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	101111	—	—	—
Jump Inst.	JUMP $ADDR_1$		Jump to the address specified	PC ← $ADDR_1$	001110	$ADDR_1$ (10 bit)		
Other Instructions	DAL $ADDR_2$,r		Load program memory to DATA register	DATA←$[ADDR_2+(r)]_P$	111100	$ADDR_2$(6 bit)		R_N
	WAIT		Wait conditionally	Wait until key in or timer F/F set up etc.	111101	—	—	—
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH}$='0'	111110	—	—	—
	NOOP		No operation	——	111111	—	—	—

(Note 1) During the execution of input and output instruction, control of input/output of instruction is automatically carried out at the highest rank bit value of Code No. (C) of port.

- MSB = '1' of Code No. (C) : output instruction
- MSB = '0' of Code No. (C) : input instruction

(Note 2) Basically, the execution of SIO instruction is treated in the same way as the execution of other input and output instruction (PLL instruction, SEG instruction, etc.), but it differs in the following points:

- It is necessary in the first place to select an external device which becomes the transfer address of serial data by the chip select code ((C) = FH). (Refer to Serial Interface Item 1).
- Execution time of SIO instruction is 88.8 μS.

(Note 3) In the TC9302AF, the input port treated by the execution of SEG instruction and MARK instruction does not exist, and so these input instructions can not be used.

(Note 4) Among the program memory address 10 bits assigned by DAL instruction, the lower rank 4 bits become indirect addressing based on the content of general register. DAL instruction executing time is 88.8 μS just like the executing time of SIO instruction.

(Note 5) When WAIT instruction is executed, the program keeps waiting condition at that address until the instruction is released under the following conditions:

- When there is an input (K0 ∿ K3 ports) to key input port.
- When $\overline{\text{INH}}$ input has changed.
- When 2HZ timer F/F is set.

When WAIT mode is released, instruction of next address is executed.
If WAIT instruction is executed during the above conditions, same operation as NOOP instruction is made.

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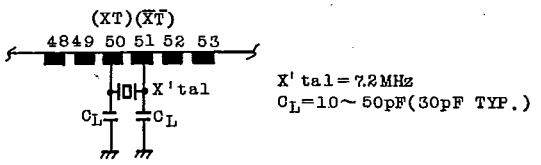
CONNECTION OF CRYSTAL OSCILLATOR

Connect 7.2 MHz crystal oscillator with the crystal oscillator terminals (X_T, $\overline{X_T}$ terminal) of the device as shown below. This oscillation signal is supplied to clock generator and reference frequency divider, and produces each timing signal of CPU and reference frequency signal.

Adjust the crystal oscillation frequency while monitoring reference frequency output terminal or LCD segment output terminal.



(Note) Use crystal oscillator of low CI value and satisfactory starting characteristics.

SYSTEM RESET

System reset is applied to the device when 'L' level is given to $\overline{INT}$ terminal, or when the voltage, OV → 4.5V, is supplied to VDD terminal (power on reset). After the lapse of 10 mS stand-by time succeeding to the system reset, program starts from zero address.

As power on reset function if imployed usually, $\overline{INT}$ terminal is fixed at 'H' level.

(Note 1) During the system reset time and the succeeding stand-by time, LCD common output and segment output are fixed at 'L' level.

(Note 2) After the system reset, I/O port 2 and 3 are both set at input mode, but initialization of output port and internal port (G-register, etc.) is not carried out. Especially, at the initial power on stage, content of these ports is indefinite, and therefore it is necessary to make initialization with program according to your use.

(Note 3) Carry out power on reset after establishing $\overline{INH}$ = 'L' level condition.

BACK UP MODE

If CKSTP instruction is executed when $\overline{INH}$ terminal is at 'L' level, clock generator and CPU internal of the device stop operation completely, and memory back up state can be realized at low consumption current (1 μA MAX at V_{DD} = 5V). At this time, LCD indicating output terminals and output ports are all fixed at 'L' level automatically, and therefore processing of output terminal by program is not required.

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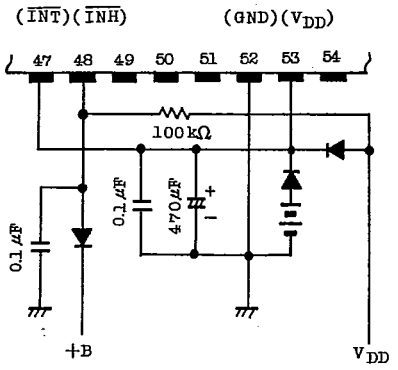
With this back up mode, supply voltage can be lowered down to 2V. In the back up mode, program stops at the execution address of CKSTP instruction, back up mode is released at $\overline{INH}$ = 'H' level, and the next address is executed after the lapse of stand-by time of 10 mS.

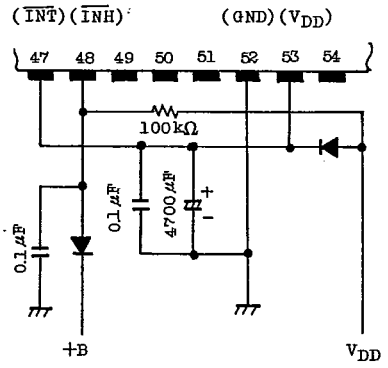
(Note 1) In the back-up mode, the condition of output terminals is all fixed at 'L' level, but the content of output port is held in the data just before back up mode.

(Note 2) When CKSTP instruction is executed when $\overline{INH}$ is at 'H' level, the same operation as NOOP instruction is made : (Back up mode is not entered).

EXAMPLE OF BACKUP CIRCUIT



BACKUP BY BATTERY



BACKUP BY CAPACITOR

+B shall be connected to a fast fall power supply when the power switch of a set turned off.

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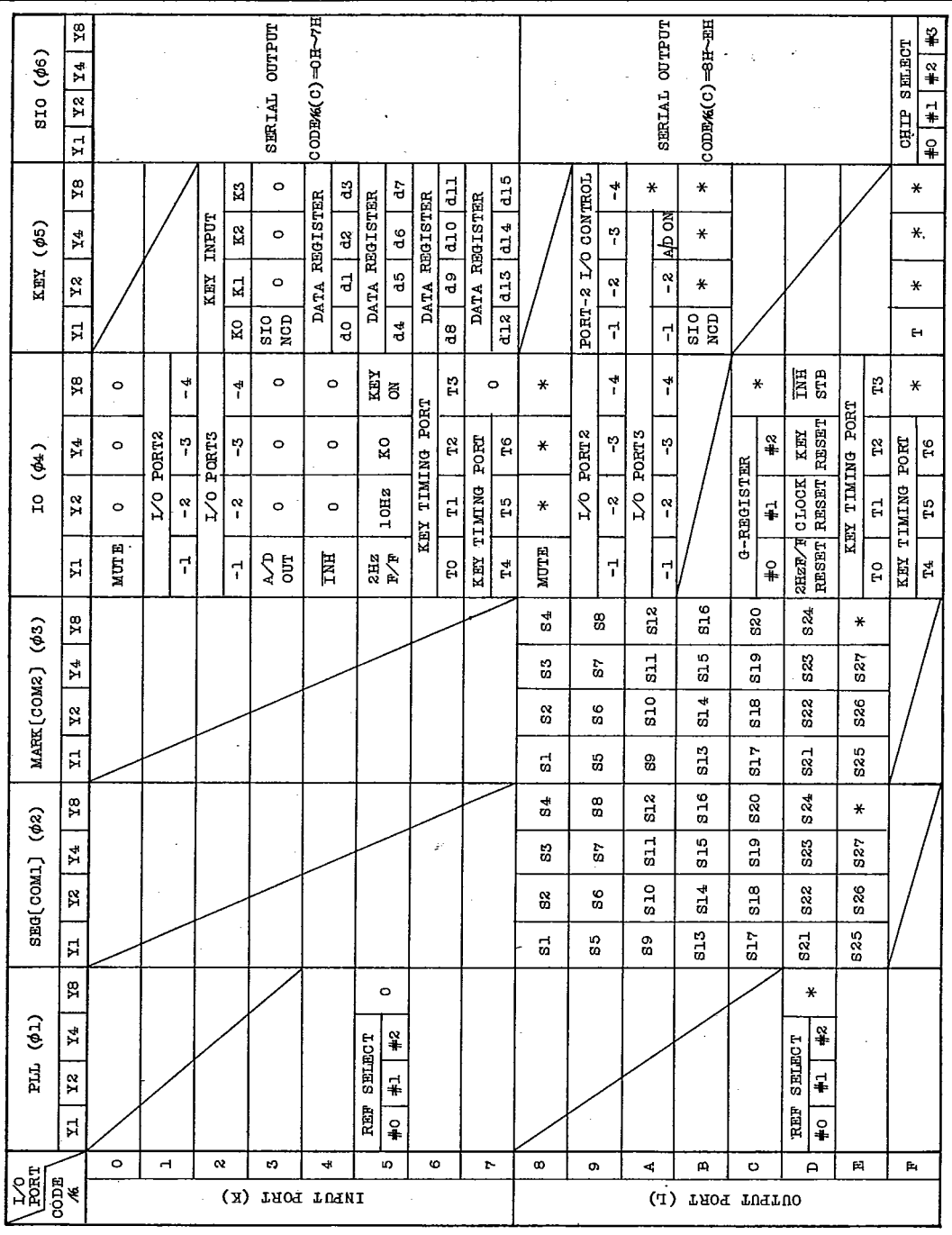

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I/O MAP

All ports in the device are expressed by six input and output instructions (PLL instruction, SEG instruction, MARK instruction, IO instruction, KEY instruction, SIO instruction) and 4 bit matrix of code No. C. Assignment of these ports is indicated previously as I/O map. In the I/O map, port names treated in the execution of each input and output instruction are assigned horizontally, while code Nos. of port are assigned vertically. G-register and data register are also treated as port.

Basically, the data is treated at each port as 4 bit unit, and code No.(C)= 0H ∿ 7H are assigned to input ports, while code No.(C)= 8H ∿ FH are assigned to output ports.

(Note 1) The port indicated with oblique line on I/O map is a port not existing in the device. In the execution of output instruction, when data is outputted to the non-existing output port, no effect is given to the content of other port or data memory. When non-existing input port is designated during the execution of input instruction, the content read into the data memory becomes indefinite.

(Note 2) Among the output ports on I/O map, * marked port is unused port. The data outputted here becomes "don't care".

(Note 3) Regarding the content of port expressed in 4 bit, Y1 corresponds to the lowest ranking bit of the data of data memory, and Y8 to the highest ranking bit. Data of each port is all treated with positive logic.

(Note 4) Each port assigned by six input and output instructions and code No. C is coded as follows:

ϕ[K/L] m n

- n: Operand port CN of input and output instruction (Lower 3 bit value of code No. of port : 0 ∿ 7)
- m: Input and output instructions of 6 kinds are described in 1 ∿ 6.

Input and Output Instruction	PLL	SEG	MARK	IO	KEY	SIO
m	1	2	3	4	5	6

- [K/L]: Expresses input/output port (K : input port, L : output port)

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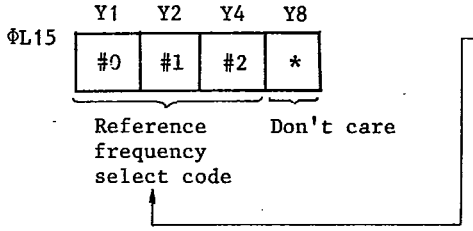
REFERENCE FREQUENCY DIVIDER

This unit divides oscillating frequency of external 7.2 MHz crystal, and produces eight kinds of PLL reference frequency signal, 1 KHz, 5 KHz, 9 KHz, 10 KHz, 12.5 KHz, 25 KHz, 50 KHz, 100 KHz. Such selection is carried out with the data of REF select port.

The selected signal is supplied to PLL LSI from REF output terminal. The reference frequency divider is reset with $\overline{INH}$ = 'L' level input, and REF output is fixed at 'L' level.

1. REF Select Port (ϕKL15)

This is an internal port to select eight kinds of reference frequency signal. Normally, this port is accessed by PLL output instruction designated [C_N = 5] at the operand part.(ϕL15) By the execution of PLL input instruction designating [C_N = 5] at the operand part, the content of the data presently outputted is read into the data memory. (ϕK15)



Code Table

#2	#1	#0		Reference Frequency
0	0	0	0	1 KHz
0	0	1	1	50 KHz
0	1	0	2	5 KHz
0	1	1	3	100 KHz
1	0	0	4	9. KHz
1	0	1	5	10 KHz
1	1	0	6	12.5 KHz
1	1	1	7	25 KHz

LCD DRIVER

The TC9302AF contains LCD driver of 1/2 duty, and 1/2 bias driving(frame frequency = 50 Hz)

Two common outputs (COM1, COM2) output three potentials of voltage, V_{DD},1/2 V_{DD},GND level respectively, at 1/4 phase difference. 54 segments can be lighted by the combination of this common output and 27 segment output (S1 ∿ S27). That is to say, both COM1 system segment and COM2 system segment can be lighted by one segment output, what is called dynamic display method.

LCD driver does not contain segment decoder, so 54 segments can be freely used by program for 7 segment indication or mark segment indication.
COM1 system segment output is controlled by execution of SEG instruction and COM2 system segment output is by execution MARK instruction.

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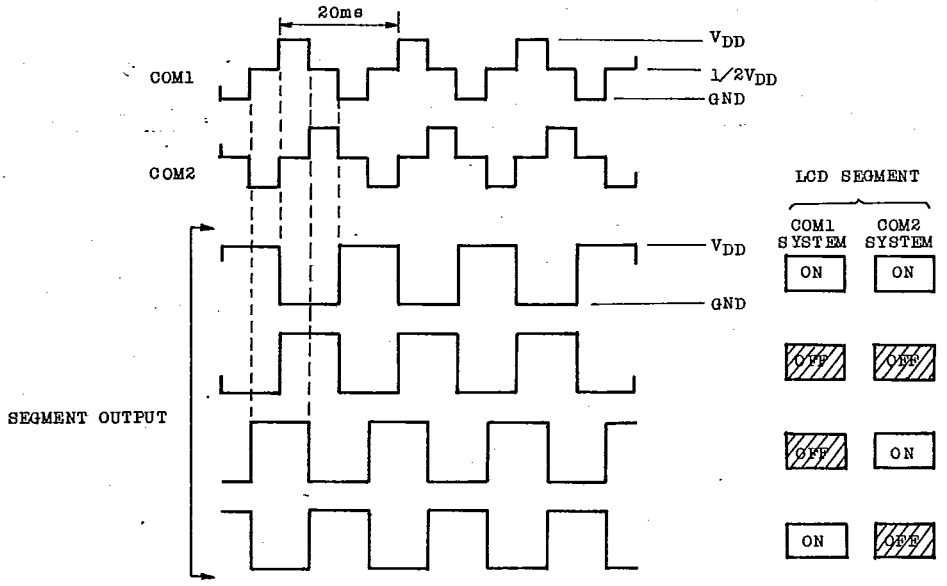
1. Timing Chart of LCD Driver

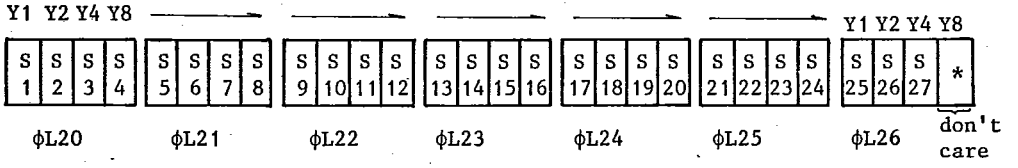
Below are shown the timing of COM1, COM2 output wave form and four kinds of segment output wave form.



(Note) During system reset and back up mode (CKSTP instruction executing time) common output and segment output are all fixed at 'L' level, automatically.

2. COM1 System Segment Port (ϕ120 ∿ ϕ126)

This is a port group to output 27 segment data of COM1 system. It is accessed by SEG output instruction. Segment data is treated with 4 bit unit, and COM1 system segment turns "ON" when data '1' is outputted, while COM1 system segment turns "OFF" when data '0' is outputted.



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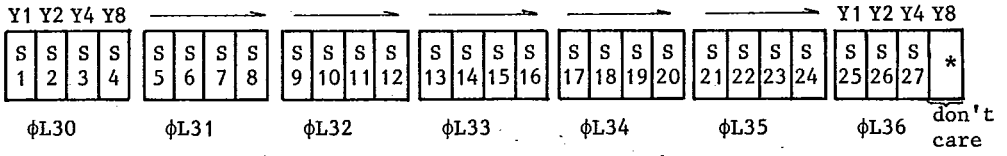
2. COM2 System Segment Port (φL30 ∿ φL36)

This is a port group to output 27 segment data of COM2 system. It is accessed by MARK output instruction. Segment data is treated with 4 bit unit, and COM2 system segment turns "ON" when data '1' is outputted, while COM2 segment turns "OFF" when data '0' is outputted.



(Note) Names of each port of COM1 system and COM2 system correspond to the names of segment output terminals, respectively.

(Note) Decoding of segment can be made by providing the segment decode pattern in the program memory and reading it into the data memory by using DAL instruction. Hence, LCD driver does not contain segment decoder. As DAL instruction refers to the data in the program memory with 16 bit unit, assignment of segment port appropriated to the 7 segment indication is continuously performed with 8 bit unit (7 segment + 1. mark) for example port S1∿S4, port S5 ∿S8 both in COM1 system and COM2 system in common.

I/O PORT 2, I/O PORT 3

1. I/O Port 2, I/O Port 3

I/O port 2 is 4 bit and I/O port 3 is 2 bit port, both of which are capable of making input and output setting with 1 bit unit. In the case of I/O port 2, input and output setting are made by the content of port-2 I/O control internal port, while in the case of I/O port 3, it is made by the content of port-3 I/O control internal port. Setting to input port can be made by setting '0' to the bit of corresponding I/O control port, while setting to output port can be made by setting '1' to the same.

I/O port 3 combines analog input of 4 bit A/D converter.

At the time of input port setting, the data inputted to I/O port at present is read into the data memory by the execution of IO input instruction designating [C_N = 1 or 2] at the operand part. (φK41 or φK42). At this time, content of output side latch (φL41, φL42) gives not effect to the input data.

(Note) Data of output side latch P3-3, P3-4 is inputted from input port P3-3, P3-4, respectively.

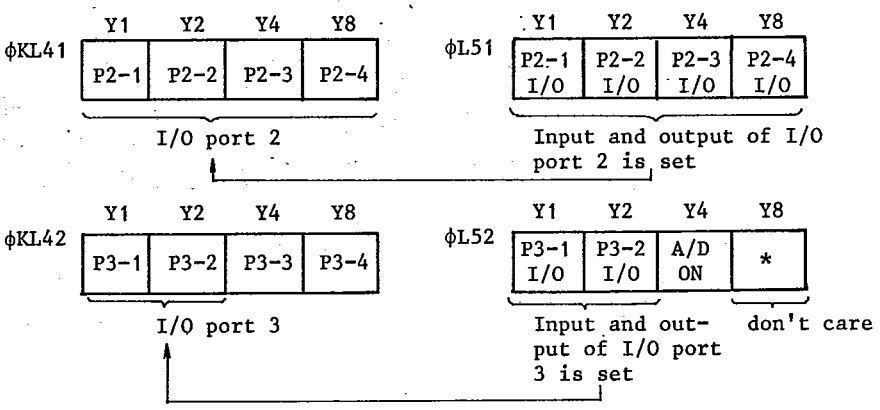
During the output port setting, output condition of I/O port is controlled by the execution of IO output instruction assigning [C_N = 1 or 2] at operand part. (φL41 or φL42).

Further, by the execution of IO input instruction, the content of currently outputted data is read into the data memory (φK41, φK42).

(Note) Data of P3-3, P3-4 of output side latch becomes effective only during the operation of A/D converter.

(Note) IO control port is accessed by KEY output instruction designating [C_N = 1 or 2] at the operand part. After system reset, the content of this port is all reset to '0', and I/O port is all set at input mode.

(Note) During back up mode, the output condition of I/O port set at output mode is all fixed at 'L' level automatically, but the preceding data is held in the content of each output latch just before the back-up mode.



• A/D ON bit

This bit controls enable/disenable of built-in 4 bit A/D converter operation and the transfer to A/D converter input of I/O port three terminals.

I/O port 3 terminal combines analog input of built-in 4 bit A/D converter. When '0' is set at A/D ON bit, I/O port 3 becomes ordinary input and output port, and when '1' is set, A/D converter operates and I/O port 3 terminal is connected to A/D converter input (See A/D converter item)

2. Key Timing Output Port (T0 ∿ T6)

T0 ∿ T6 is exclusive output port of 7 bit, CMOS type. Normally, it is used as an output of key return timing signal of key matrix. It is accessed by IO output instruction designating [C_N = 6 or 7]at operand part. (φL46 or φL47). Further, by the execution of IO input instruction designating [C_N = 6 or 7] to operand part, content of the presently outputted data is read into the memory. (φK46, φK47).

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(Note) During the back up mode, T0 ∿ T6 output is automatically fixed at 'L' level, but the content of port remains to be former data.

	Y1	Y2	Y4	Y8
φL46	T0	T1	T2	T3

	Y1	Y2	Y4	Y8
φL47	T4	T5	T6	*

don't care

3. MUTE Port (φKL40)

This is 1 bit CMOS type exclusive output port for muting control use. Normally, it is accessed by IO output instruction designating $C_N = 0$ at operand part. (φL40) Further, by the execution of IO input instruction designating [$C_N = 0$] at operand part, content of presently outputted data is read into data memory. (φK40).

(Note) When $\overline{INH}$ input has changed to 'H'↔ 'L' level, content of MUTE port is automatically set at '1'. In this case, '0' data setting by program cannot be applied to the content of MUTE port until the changed $\overline{INH}$ input data is read into $\overline{INH}$ input latch by program ($\overline{INH}$ STB bit set of φL45). Especially at power on time, be sure to make access of MUTE port after setting '1' at $\overline{INH}$ STB bit by program.

(Note) During the back up mode, MUTE output is automatically fixed at 'L' level, but content of port is set at '1' by the change of $\overline{INH}$ input.

	Y1	Y2	Y4	Y8
φL40	MUTE	*	*	*

don't care

REGISTER PORT

G-register and data register stated in the explanation of CPU are also treated as one of internal ports.

1. G-register (φL44)

This is a register to make addressing of low address (D_R = 4H ∿ 7H) of data memory during the execution of MVGD instruction and MVGS instruction. This register is accessed by IO output instruction designating [$C_N = 4$] at the operand part.

(Note) Content of this register is effective only during the execution of MVGD instruction and MVGS instruction, and gives no effect during the execution of other instructions.

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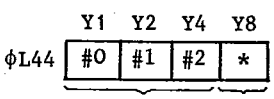


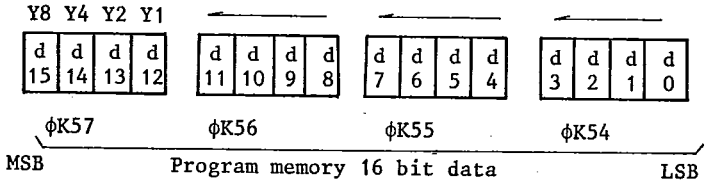
#2	#1	#0	D_R
1	0	0	4H
1	0	1	5H
1	1	0	6H
1	1	1	7H

(Note) It is possible to indirectly designate all low addresses of data memory by setting data 0H ∿ 7H on G-register. (D_R = 0H ∿ 7H)

2. Data Register (φK54 ∿ φK57)

This is a 16 bit register on which the data of program memory is loaded during the execution of DAL instruction. Content of this register is read into the data memory in 4 bit unit by the execution of key input instruction designating [C_N = 4 ∿ 7] at the operand part.

This register can be used for the decoding of LCD segment, or for the taking of band edge data of radio and of coefficient data during binary to BCD conversion.

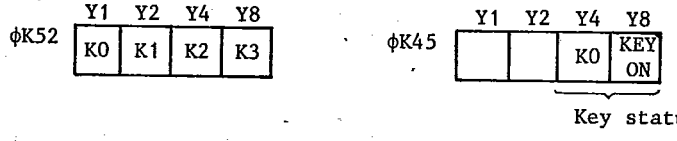


KEY INPUT

Exclusive 4 bit key input terminal for key matrix inputting is provided. Four terminals contain pulldown resistance.

1. Key input Port (φK52)

In this exclusive key input port of 4 bit, the data of key input terminal is read into the data memory by the execution of key input instruction designating [C_N = 2] at operand part.



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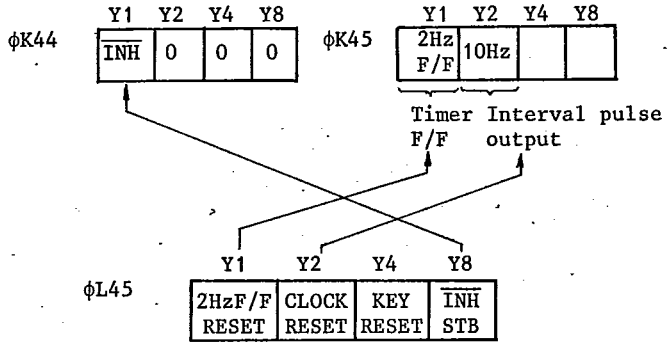
2. Key Status Bit (φK45)

Key status bit (KO KEY ON) is provided for the purpose of knowing the outline of the present key input status. Content of these bits is read into data memory by the execution of IO input instruction designating [C_N = 5] at operant part.

- KO bit
  Status of KO input terminal is outputted. (Same data as KO bit of key input port).
- KEY ON bit
  Logical OR of four input data of KO ∿ K3 terminals is outputted.
  This can be used for judging existence of key input.

INTERNAL CONTROL PORT

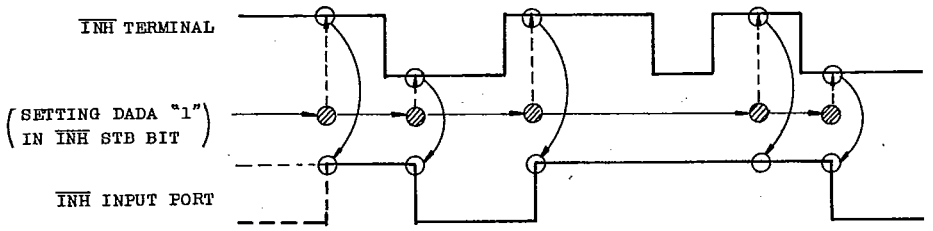
Internal control port is used for reading into data memory the inside condition of device which must be known in the execution of program, or for resetting the inside condition of device.



1. $\overline{INH}$ Input Port (φK44)

This is an input port having latch mode for inputting the data of $\overline{INH}$ input terminal. Content of this port is read into the data memory by executing IO input instruction in which [C_N = 4] is designated at operand part. Data '1' and '0' represent radio"ON"mode and radio"OFF"mode, respectively.

This input port has input latch, and by the execution of IO output instruction designating [C_N = 5] at operand part, the status of $\overline{INH}$ terminal is taken into the port every time data '1' is set in $\overline{INH}$ STB bit.



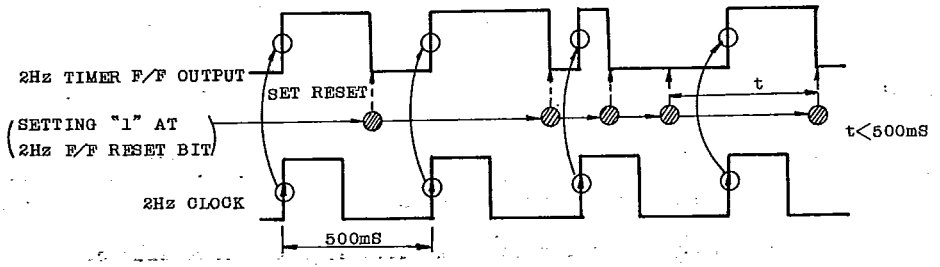
2. 2 Hz Timer F/F (φK45)

2 Hz timer F/F is reset by 2 Hz (500 mS) signal. By the execution of IO output instruction designating [C_N = 5] at operand part, this timer is reset by setting data '1' at 2 Hz F/F RESET bit. This FF output is read into the data memory by the execution of IO input instruction designating [C_N = 5] at operand part.

As timer F/F is automatically set every 500mS, it is usually used for counting of watch.

Since timer F/F is reset only with 2 Hz F/F RESET bit, count error takes place unless data '1' is set at 2 Hz F/F RESET bit within 500 mS cycle, and correct times is not obtainable.

(Note) Condition of timer F/F output becomes uncertain at power on time or after the execution of CKSTP instruction.



3. 10 Hz Interval Pulse (φK45)

10 Hz interval pulse is outputted to 10 Hz bit with 100 mS period duty 50% pulse. This is read into the data memory by the execution of IO input instruction designating [C_N = 5] at operand part. This output has no flip flop and can be used for counting muting time.

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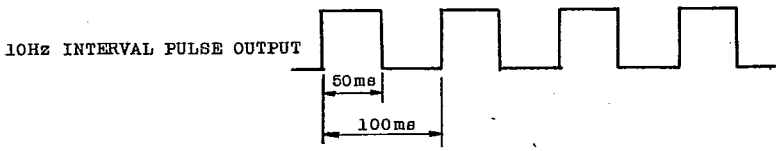

4. Other Control Bit (ϕL45)

- Clock reset bit

  Each time data '1' is set in this bit, clock of below 50 Hz is reset. (10 Hz interval pulse is also reset). This bit is used for adjusting time of clock. Accuracy of clock at this time is $^{+0}_{-0}$.002 second.

- KEY RESET bit

  When data '1' is set in this bit, KEY ON signal to break WAIT mode is reset. This is effective when executing WAIT instruction immediately after key inputting. Beside the above, it is necessary to set data '1' at $\overline{\text{INH}}$ STB bit and 2 Hz F/F reset bit before executing WAIT instruction. This is for resetting each condition to break WAIT mode.

  The above bit is also accessed by IO output instruction in which [C_N = 5] is designated at operand part.

5. T Port (ϕL57)

This is an internal port for testing function of device. It is accessed by KEY output instruction designating [C_N = 7] at operand part. Never fail to set data '0' in ordinary program.

A/D CONVERTER

The TC9302AF has built-in 4 bit A/D converter of successive comparison system by program. As analog input terminal I/O port 3 (P2-1, P3-2) terminal is used. Transfer control of these terminals can be made with program.

This A/D converter can be used for measuring electric field intensity or judging stop level during auto tuning by inputting signal meter output. Further, A/D IN (P3-2) terminal can also be used as one bit input port which can freely set threshold level with program.

Operation of A/D converter and analog input transfer control of I/O port 3 are carried out with A/D ON bit of PORT-3 I/O CONTR internal port. (Refer to Input output port Item 1).

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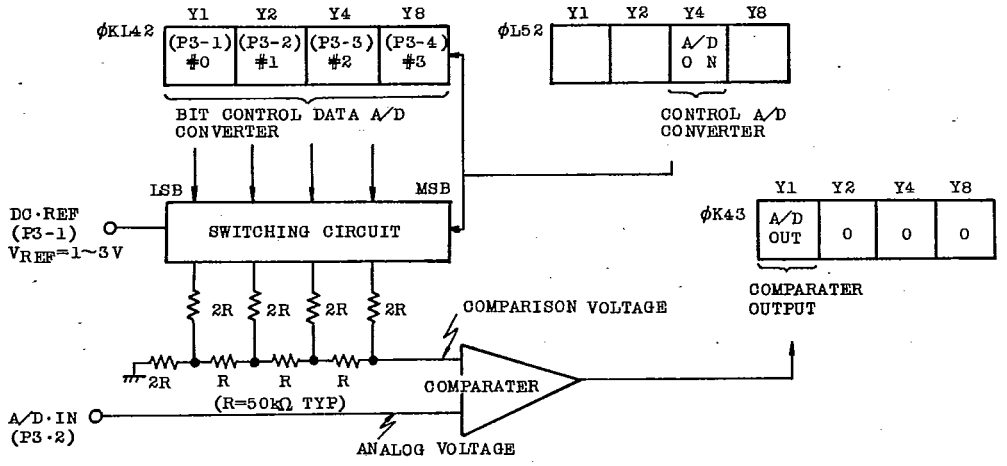
When data '1' is set at A/D ON bit, P3-1 is transferred to reference voltage input and P3-2 is transferred to analog voltage input, and A/D converter operates. At this time, 4 bit data of output side latch (PL42) of I/O port 3 becomes bit control data of A/D converter. Bit control data of present A/C converter can be read from input port (ϕK42) I/O port 3.



Construction of A/D converter

Construction of A/D converter is indicated above. A/D converter produces 16 kinds of comparison voltage obtained by dividing reference voltage (V_{REF}) from bit control data value of 4 bit by means of R-2R type resistance ladder network system. This comparison voltage and analog voltage are inputted to comparator and compared. Result of comparison is outputted to A/D OUT port (ϕK43). The data of this port is read into the data memory by the execution of IO input instruction designating [C_N = 3] at operand part.

The following data is outputted to A/D OUT port:

Data '1' ... When analog voltage > comparison voltage

Data '0' ... When analog voltage < comparison voltage

Value of comparison voltage is calculated by the following formula.

$$\text{Comparison voltage} = V_{REF} \times \frac{N}{16}$$

(Note) N value is bit control data value (Decimal number)

$15 \geq N \geq 1$

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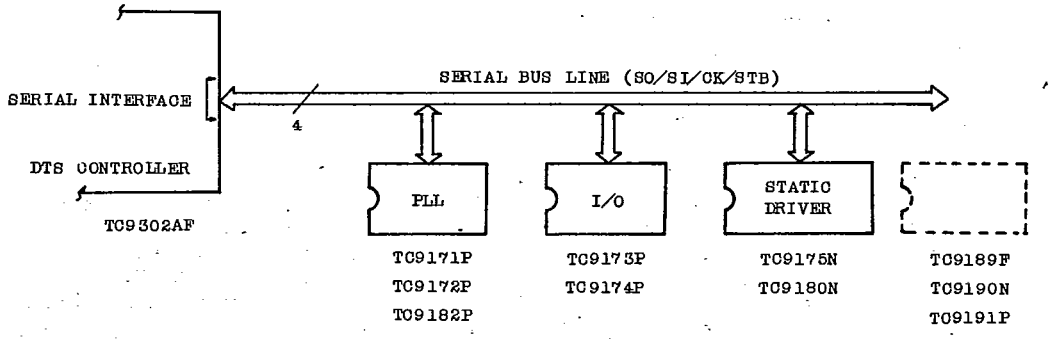
(Note) During A/D converter operating time (when setting data '1' at A/D ON bit), P3-1, P3-2 I/O control bits of PORT-3 I/O control port are automatically reset at '0'.

(Note) After system resetting, A/D ON bit is reset at '0'.

SERIAL INTERFACE

This is exclusive serial I/O for strongly controlling external PLL LSI and peripheral option IC group. Serial I/O terminals are four terminals of SO, SI, CK, STB. Data transfer is conducted by connecting these terminals and external devices with four serial bus lines. Extension of function can easily be made by freely connecting peripheral optional ICs on this bus line, depending upon the system. External devices comprises abundant items including PLL LSI, I/O port extending IC, and static indicating driver.

Serial transfer is conducted by the execution of SIO instruction, and transfer of all data is completed during the execution time of this instruction (88.8 μS). In this way, port having each external device can simply be treated like the port treated by the execution of other input and output instructions. Further, two kinds of serial transfer format can be selected by program.



1. Chip Select

As shown above, many external devices can be freely connected with serial bus line. Hence, when conducting serial transfer, first of all it is necessary to select the device of opposite transfer party. Address of opposite party expressed with 4 bit data called chip select code is assigned to each of external device on serial bus line. By assigning this chip select code, data transfer is carried out with the external device corresponding to that code number.

Chip select port (φL67) is an internal port for designating this chip select code, and is accessed by SIO output instruction designating [C_N = 7] at operand part. Maximum 16 kinds of external device can be selected by 4 bit code. (In actual case, some device has more than two chip select code numbers. Example : TC9171P ... 2, TC9189F ... 3)

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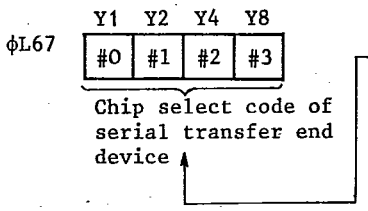

#3	#2	#1	#0		Products Name	Functions
0	0	0	0	0	———	———
0	0	0	1	1	TC9171P/82P	PLL *
0	0	1	0	2	TC9172P	
0	0	1	1	3	TC9173P	I/O port extension use
0	1	0	0	4	TC9174P	Output port extension use
0	1	0	0	5	TC9175N	FL static indication driver
0	1	1	0	6		
0	1	1	1	7	TC9180N	General purpose static indication driver (LED/LC)
1	0	0	0	8		
1	0	0	1	9	TC9189F	Dynamic indication driver * (LCD/LED)
1	0	1	0	A	TC9190N	
1	0	1	1	B	TC9191P	
1	1	0	0	C		

(Note) Chip select code No. of * marked products is same in all cases.

(Note) When executing SIO instruction, firstly designate chip select code of the opposite party device by SIO output instruction. Chip select code number once set maintains that code unless designated otherwise, and so, select code need not be designated at each execution of SIO instruction.

(Note) It is impossible to simultaneously connect the devices of same chip select code on the serial bus line.

(Note) After the designation of chip select code number, data is outputted to the port of external device corresponding to the code number designated at operand part, by the execution of SIO output instruction. Then, by the execution of SIO input instruction, content of external device port is read into the data memory.

(Note) It is prohibited to program SIO input instruction for the instruction to be executed next to SIO output instruction.
When programming SIO input instruction after SIO output instruction, insert a instruction, for example NOOP instruction, between them.

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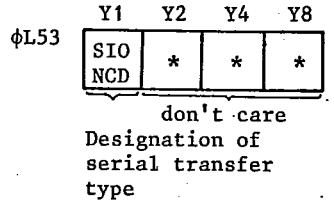
2. Serial Transfer Format

Two kinds of serial transfer format can be selected depending upon the content of SIO NCD port. This internal port is accessed by KEY output instruction designating [C_N = 3] at operand part. By the execution of KEY input instruction, content of this port is read into data memory.

When data '0' is set at SIO NCD port, serial transfer type of $\overline{NCD}$ mode is realized. In the case of $\overline{NCD}$ mode, code No. of the port designated at the operand part of SIO instruction is serial transferred together with the data. When data '1' is set, NCD mode is realized. In NCD mode, code No. is not transferred and data alone is sent and received. (C_N value of operand part of SIO instruction becomes (don't care)).

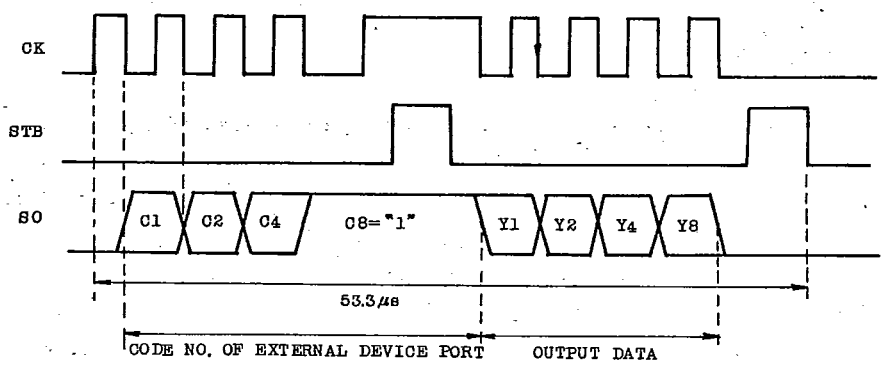
(Note) Serial transfer with the previously denoted external device is all conducted with NCD mode.



(Note) In the serial transfer during NCD mode, designation of chip select code is meaningless. That is to say, transferring address cannot be selected.

3. Serial Input and Output Timing Chart

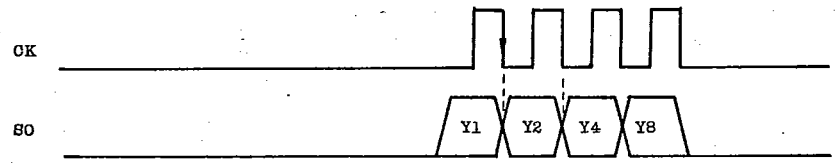
- $\overline{NCD}$ mode output timing



In the above indicated timing, code No. (C1 ∿ C8 : 4 bit) of the destination device port and data (Y1 ∿ Y8 : 4 bit) are serially outputted from LSB by the trailing of CK signal.

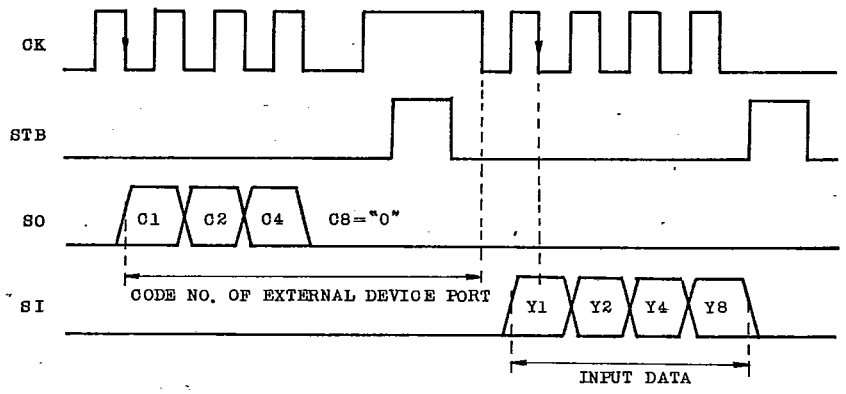
(Note) During the execution of SIO output instruction ($\overline{NCD}$ mode), C8 bit of Code No. is fixed '1' continually.

- NCD mode output timing



Serial output of NCD mode becomes 4 bit data alone. STB output is continually fixed at 'L' level.

- $\overline{NCD}$ mode input timing



In the above timing, when Code No. (C1 ∿ C8 : 4 bit) of input port of destination device is outputted from SO terminal, content of that input port (Y1 ∿ Y8 : 4 bit) is serially inputted from LSB to SI terminal. SO data is outputted with trailing of CK signal, while SI data is inputted with trailing of the same signal.

(Note) During the execution of SIO input instruction ($\overline{NCD}$ mode), C8 bit of Code No.is fixed '0' at all times.

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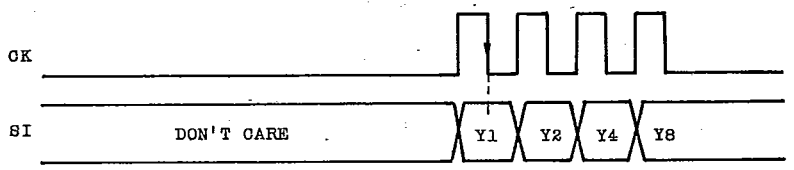
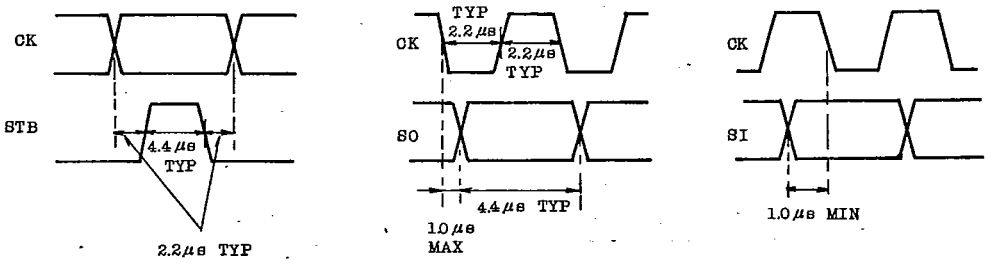
• NCD mode input timing



During serial inputting of NCD mode, STB output and SO output are always fixed at 'L' level. SI data is inputted by the trailing of CK signal.

4. Serial Timing Pulse Width

Pulse width of each timing signal is shown below.



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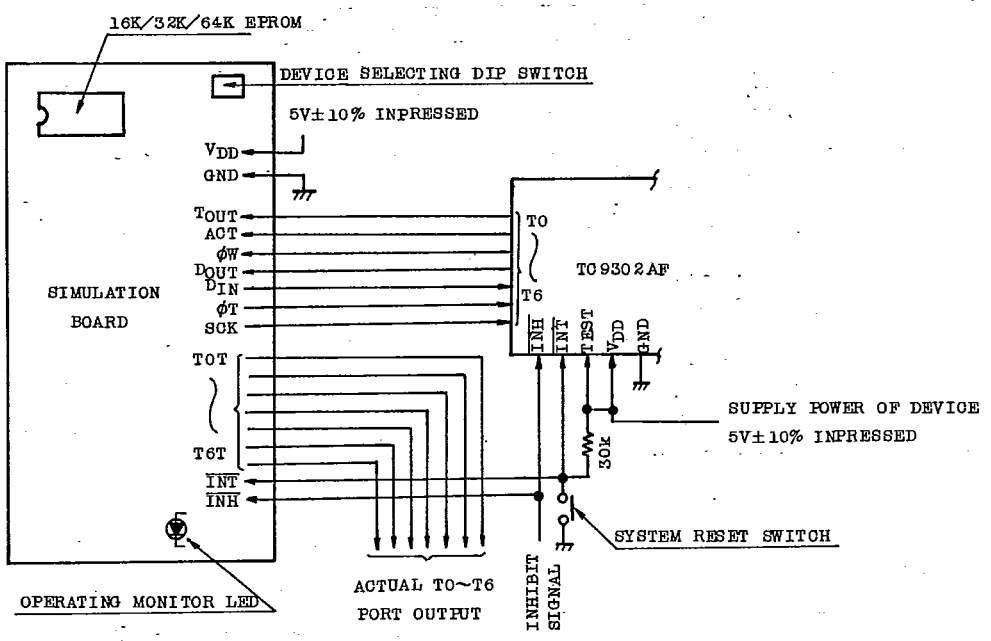
APPLICATION TO EVALUATOR CHIP

When 'H' level is supplied to TEST terminal (Test mode), device operates as evaluator chip, and function evaluation of developing program can be made by utilizing external simulation board and EPROM. In the test mode, the device operates by the program written in EPROM, irrespective of the content of program memory in the device. At this time, key timing output port (T0 ∿ T6) is transferred to the controlling input and output terminal of simulation board, actual T0 ∿ T6 port output is outputted from the simulation board side.

For the system reset in test mode, $\overline{INT}$ input is employed.

Below is shown connection diagram of the device and simmulation board when the unit is used as evaluator chip.



(Note) Select the device TC9302AF by a dip switch on the simulation board.

(Note) Inpress 5V ±10% voltage on the device and simulation board even during back-up mode. In the test mode, it is impossible to reduce the supply voltage of the device to 2V.

(Note) In the case of back-up mode (execution of CKSTP instruction), operating monitor LED on the simulation board turns off.

(Note) Each terminal of the device other than that indicated above can be used