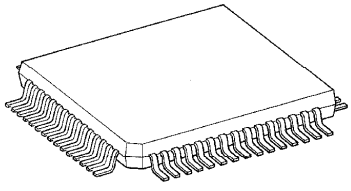
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9308AF

DTS MICRO CONTROLLER CONTAINING PLL·LCD DRIVER (DTS-11)

TC9308AF is a 4bit CMOS microcontroller for digital tuning system capable of making 3V low voltage operation, and containing PLL circuit, LCD driver.
CPU has 4bit parallel addition and substruction (AI / SI instructions, etc.), logical operation (OR and AN instructions, etc.), plural bit judge, comparison instructions (TM, SL instructions, etc.) and time base function.
The package is 60-pin mini-flat type, and has abundant I / O ports and exclusive key-input ports controlled by the powerful input / output instructions (IO, KEY instructions), besides containing PLL circuit.
By combining with the prescaler TD6134AF, it permits the configuration of DTS that receives FM / AM and TV (VHF) bands.



QFP60-P-1414-0.80A

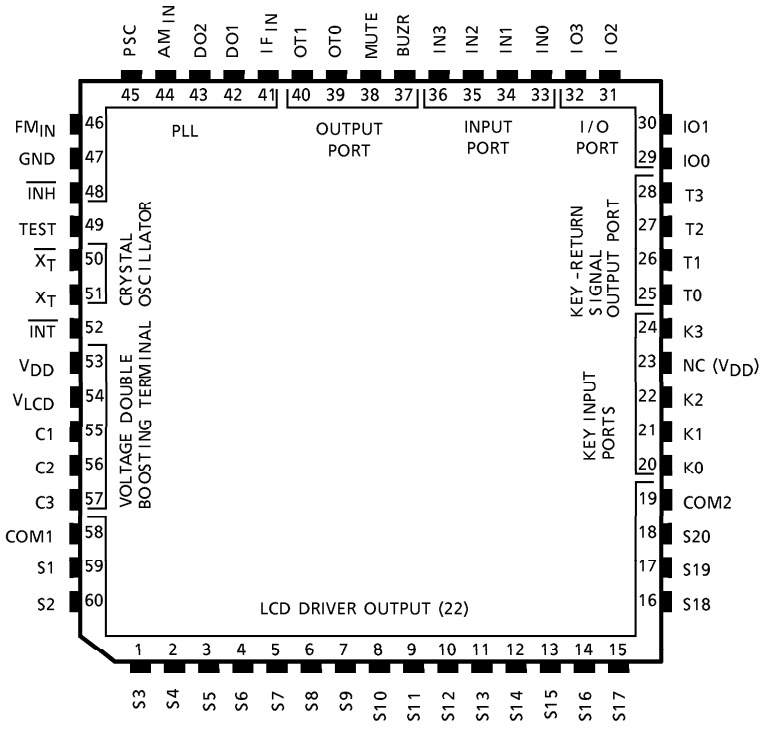
Weight : 0.85g (Typ.)

FEATURES

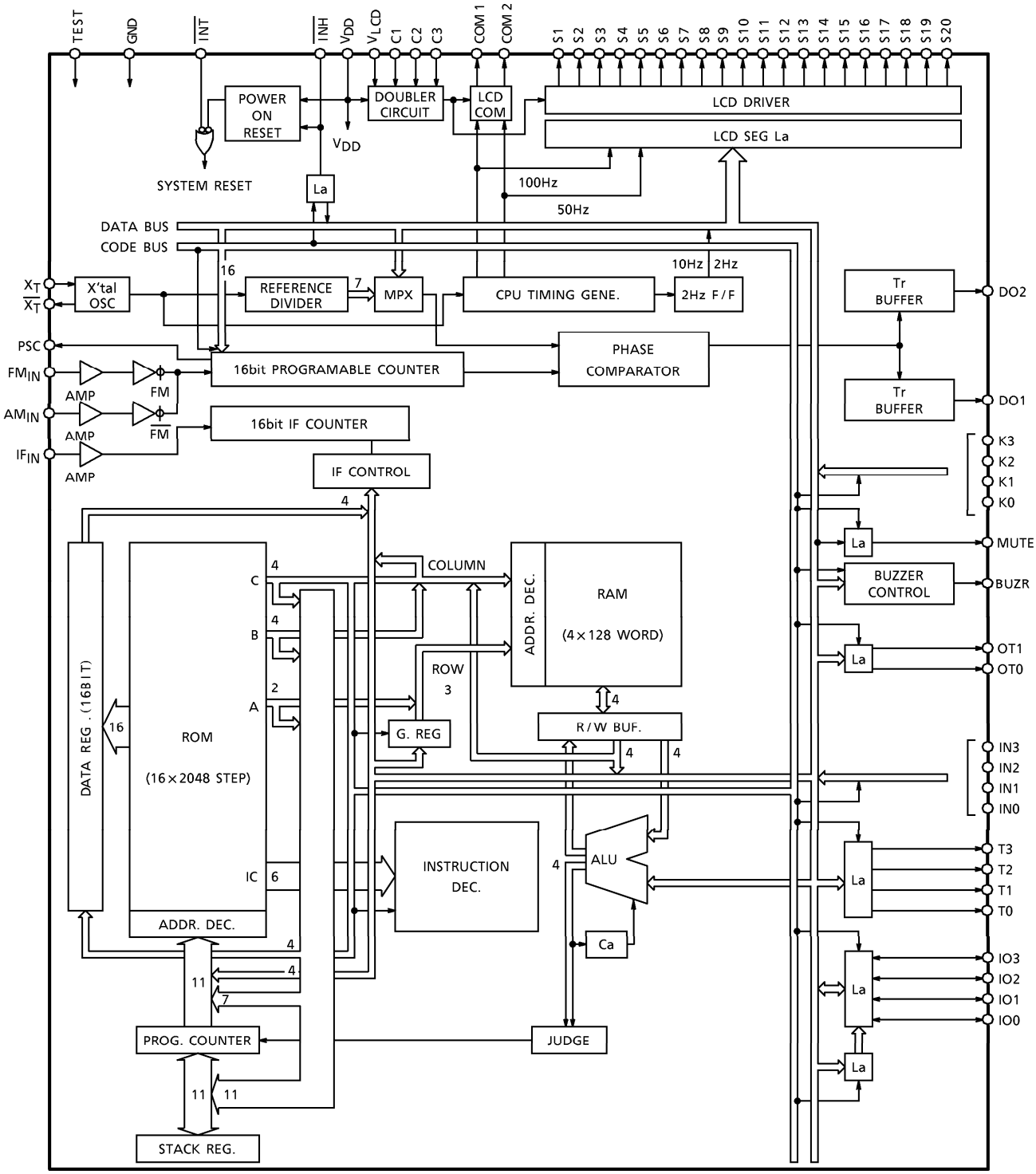
- 4bit micro controller for digital tuning system use
- It is operated with 3V single power supply. (V_{DD} = 1.8~3.6V)
- Back-up of data memory (RAM) and each port are easily made. (by $\overline{INH}$ terminal)
- Built-in LCD driver (1 / 2 duty, 1 / 2 bias driving, driving frequency : 50Hz), and boosting circuit for display
- Program memory (ROM) : 16 bits × 2048 steps
- Data memory (RAM) : 4 bits × 128 words
- Powerful instruction set of 65 kinds (all single word instruction)
- Instruction executing time 80μs (75kHz crystal connection)
- Abundant addition and substraction instructions
  (addition instructions 12 kinds, substraction instructions 12 kinds)
- Powerful compound judge instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN instructions)

- Data transfer in same low address is possible.
- Indirect transfer of register is possible. (MVRD, MVRS, MVGD, MVGS instructions)
- 16 powerful general registers (arranged in RAM)
- Stack level : 1 level
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instruction can be freely made among 2048 steps.
- At the FM or TV band, swallow counter is composed by combining with prescaler TD6134AF, and is able to receive TV VHF band.
- It is possible to freely refer to the content, 16 bits, of optional address within 1024 steps in program memory (ROM). (DAL instruction)
- Independent frequency input terminal at FM and AM (FM_{IN}, AM_{IN}), and two phase-Comparator outputs. (DO1, DO2)
- 7 kinds of reference frequency can be selected with program.
- Powerful input / output instructions. (IO, KEY instructions)
- Exclusive input port (K0~K3) for key input use and abundant 22 exclusive LCD driving terminals.
- Abundant 10 I / O ports (ports for which input and output can be assigned for each bit : 4, exclusive input ports : 4, exclusive output ports : 2)
- 3 kinds of back-up mode (only CPU operating, Crystal oscillation and Clock stop) are possible by instructions.
- 2Hz timer F / F and 10Hz interval pulse output are contained. (Internal port for time base use)
- Locked condition of PLL can be detected.
- Universal-type IF counter is built in.

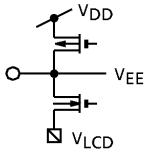
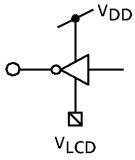
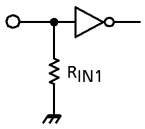
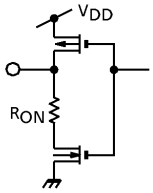
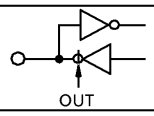
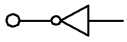
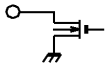
PIN CONNECTION

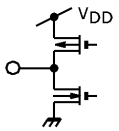
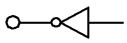
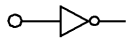
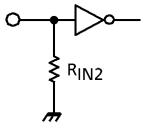


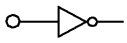
BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	EXPLANATION OF FUNCTION AND OPERATION	REMARKS
58	COM1	LCD Common Output	This is a common signal output terminal to LCD. Indication of maximum 40 segments is possible with matrix made with S1~S20. To this terminal, three value levels of V_{DD}, V_{EE}, V_{LCD} are output with 5ms interval and 50Hz cycle.	
19	COM2			
59, 60 1~18	S1~S20	LCD Segment Output	This is a segment signal output terminal to LCD. Indication of maximum 40 segments is possible with matrix made with COM1 and COM2. The data for these terminals are output by the execution of SEG instruction (COM1 system) and MARK instruction (COM2 system).	
20~22 24	K0~K3	Key Input Port	This is a 4bit input port for key matrix input. 16 (=4×4) key data can be input with matrix made with T0~T3 Key Return Timing Output Port. All these terminals are built in pull-down resistances.	
25~28	T0~T3	Key Return Timing Output Port	This is a 4bit output port for Key Return Timing Output. Usually, it is output the timing signal for key matrix. For making the matrix, it is built in load resistance at N-ch FET side, useless the diode.	
29~32	IO0~IO3	I/O Port	This is a 4bit general purpose I/O port. It is possible to assign input and output for each bit by program.	
33~36	IN0~IN3	Input Port	This is a 4bit general purpose input port. The input data is read into the RAM at 4bit unit.	
37	BUZR	Buzzer Pulse Output Port	This is the beep sound pulse output port. It is output 3 kinds of beep sound pulse signal by program.	
38	MUTE	Muting Output Port	This is a 1bit output port. This is usually used as muting control signal output.	
39, 40	OT0, OT1	Output Port	This is a 2bit general purpose output port. Output form is N-ch FET open-drain structure, output breakdown voltage is 12V.	

PIN No.	SYMBOL	PIN NAME	EXPLANATION OF FUNCTION AND OPERATION	REMARKS
41	IF_{IN}	IF Counter Input Port	This is a IF signal input terminal of 16bit general purpose IF counter. This terminal has built-in amplifiers, and operates with C-connection and small amplitude.	Built-in Input Amplifier
42, 43	DO1, DO2	Phase Comparator Output	This is a Phase comparator output terminal of PLL. DO1 and DO2 are parallel outputs. Therefore, optimum filter constant can be set for each band of FM / AM.	
44	AM_{IN}	AM Programable Counter Input	This is a programmable counter input terminal at 12bit direct frequency-divider mode. Usually the local oscillator signal at AM band is input to this terminal. This terminal has built-in amplifiers, and operates with C-connection and small amplitude.	Built-in Input Amplifier
45	PSC	Prescaler Control Output	This is an output terminal which controls 1 / 15 or 1 / 16 frequency-dividing mode of two modulus prescaler. This output signal controls two frequency-dividing mode of external prescaler as using programmable counter for pulse-swallow counter. 1 / 15 : "L", 1 / 16 : "H"	
46	FM_{IN}	FM Programable Counter Input	This is an input terminal of programmable counter at 16bit swallow-counter mode. This terminal is input the divided frequency output signal of external prescaler, and has built-in input amplifiers and operates with C-connection and small amplitude.	Built-in Input Amplifier
48	$\overline{INH}$	Inhibit Input	This is a signal input terminal for selecting radio mode. "H" : radio ON "L" : radio OFF	
49	TEST	Test Input	This is an input terminal for controlling test mode control. At "H" level, test mode is made, and at "L" level, normal operation is carried out. In the test mode, the device operates as evaluator chip, and program evaluation is made possible on EPROM base through combination with external simulation board. This terminal is built in a pull-down resistance.	

PIN No.	SYMBOL	PIN NAME	EXPLANATION OF FUNCTION AND OPERATION	REMARKS
50	$\overline{X_T}$	Crystal Oscillation Terminal	This is a connecting terminal of crystal resonator. Reference crystal of 75kHz is connected. During the execution of CKSTP instruction, oscillation is automatically stopped.	Built-in Oscillator
51	X_T			
52	$\overline{INT}$	Initializing Input	This is a system reset signal input terminal of the device. During $\overline{INT}$ is at "L" level, reset is applied, and when it becomes "H" level, it is normal operation mode.	
54	V_{LCD}	Voltage Double Boosting Terminal	These are voltage double boosting terminal for driving LCD. Boosting capacitors are connected to these terminals. (Typ. 0.1~3.3μF)	—
55	C1			
56	C2			
57	C3	Reference Voltage Stabilizing Capacitor Connecting Terminal	The stabilizing capacitor of Reference Voltage is connected to this terminal for LCD driving. (Typ. 0.01~0.1μF)	—
53	V_{DD}	Power Supply Terminal	Power supply voltage is applied. V_{DD} = 1.8~3.6V (Typ. 3.0V)	—
47	GND			

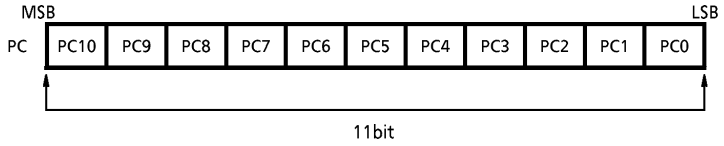
EXPLANATION OF OPERATION

○ CPU

CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, carry F/F and judging circuit.

1. Program counter (PC)

Program counter is a bolck to designate the address of program memory (ROM), and is composed of 11 bits binary up counter. This is cleared by system reset, and the program starts from zero address.
Usually, it's increment is made one by one everytime the one instruction is executed, but when JUMP instruction or CAL instruction is executed, the address designated at operand part of that instruction is loaded.
Further, when the instruction (AIS, SLT, TMT, RNS instructions, etc.) having skip function is executed, two increments of program counter is made if the result is the condition to be skipped, and the succeeding instruction is skipped.



2. Stack register (STACK)

This is a register composed of 1×11 bits during the execution of subroutine call instruction, the value obtained by adding +1 to the content of program counter, namely return address, is housed. The content of stack register is loaded on the program counter by the execution of return instruction. (RN, RNS instructions)
This stack level is 1 level, and nesting is 1 level.

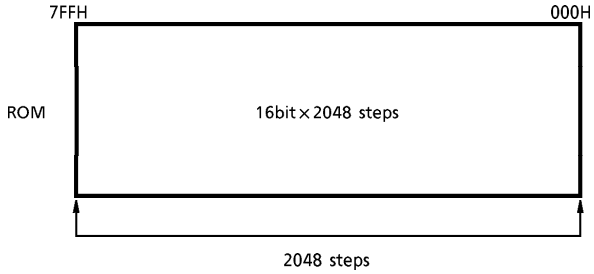
3. ALU

ALU has binary 4 bits parallel addition and subtraction, logical operation, comparison and plural bit judge functions.
This CPU has no accumulator, and all operations directly treat the contents of data memory.

4. Program memory (ROM)

Program memory is composed of 16bit×2048 steps and is the address of 000H~7FFH.
Program memory has no concept of page or field, so JUMP instruction and CAL instruction can be freely used among 2048 steps.
Further, it is possible to use optional address of program memory as data area, and its content, 16 bits, can be loaded to the data register by executing DAL instruction.

(Note) Provide the data area at the address outside the program loop in the program memory.



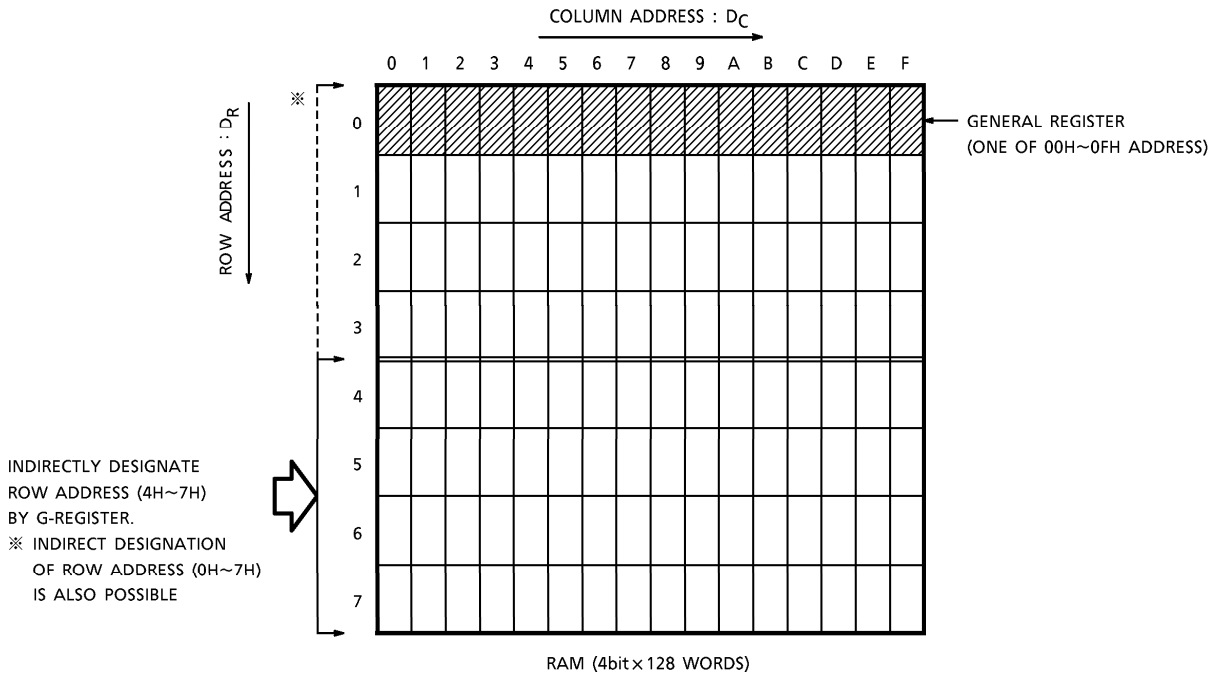
(Note) In DAL instruction, the address of program memory can be designated as the data area becomes 1024 steps of 000H~3FFH.

5. Data memory (RAM)

Data memory is composed of 4bit×128 words and used for storing data.
This 128 words are expressed with row address (3bit) and column address (4 bits).
64 words (row address = 4H~7H) among the data memory are indirect addressing by G-register. For this reason, when carrying out data processing within this territory, it is necessary to designate row address by G-register beforehand Area of 00H~0FH address in data memory is called general register, and can be used only by designating column address (4 bits). These 16 general registers can be used for operation and transfer between data memories. Further, it can also be used as ordinary data memory.

(Note) The column address (4 bits) to designate general register becomes register number of the general register.

(Note) It is also possible to indirectly designate all of row address (=0H~7H) by G-register.



6. G-register (G-REG.)

   G-register is a 3 bits register for addressing row address (D_R = 4H~7H) of 64 words in data memory.
   Content of this register is effective during executing MVGD instruction, MVGS instruction, and is not related with the execution of other instructions.
   This register is treated as one of the port, and its content is set by the execution of IO instruction among input and output instructions.
   (refer to register port item 1 page 37)

7. Data register (DATA REG.)

   This is a register composed of 1×16 bits. In this register, 16 bits data of optional address among the program memory is loaded during executing of DAL instruction. This register is treated as one of the port, and when KEY instruction among input and output instruction is executed, it's content is read in the data memory in 4 bits unit.
   (refer to register port item 2 page 37)

8. Carry F/F (C·F/F)

   This is set when carry or borrow is produced as a result of executing operational instruction, and is reset when it is not produced. Content of carry F/F changes only when addition and subtraction instruction is executed, and does not change during the execution of other instructions.

9. Judging circuit (J)

When a instruction with skip function is executed, this circuit judges it's skip condition. When skip condition is satisfied, this circuit makes two increments of program counter, and skips the succeeding instruction.
It is provided with 31 kinds of instructions having abundant skip function.
(refer to Item 11, explanation list of function and operation of instructions, ※ marked instruction page 11~17)

10. List of instruction set

65 kinds of instruction set are included, all of which consisting of one word instruction. These instructions are expressed with 6 bits instruction code.

HIGHER RANK 2 BITS / LOWER RANK 4 BITS		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	LD r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	ST M, r	SGEI M, I
0010	2	AIN M, I	ADN r, M	MVRD r, M	SEQI M, I
0011	3	SI M, I	SU r, M	MVRS M, r	SNEI M, I
0100	4	SIS M, I	SUS r, M	MVSR M_1, M_2	SLT r, M
0101	5	SIN M, I	SUN r, M	MVIM M, I	SGE r, M
0110	6	CAL $ADDR_1$	ORR r, M	MVGD r, M	SEQ r, M
0111	7		ANDR r, M	MVGS M, r	SNE r, M
1000	8	AIC M, I	AC r, M	PLL M, C	TMTR r, M
1001	9	AICS M, I	ACS r, M	SEG M, C	TMFR r, M
1010	A	AICN M, I	ACN r, M	MARK M, C	TMT M, N
1011	B	SIB M, I	SB r, M	IO M, C	TMF M, N
1100	C	SIBS M, I	SBS r, M	KEY M, C	TMTN M, N
1101	D	SIBN M, I	SBN r, M	WAIT P	TMFN M, N
1110	E	JUMP $ADDR_1$	ORIM M, I	XORIM M, I	DAL $ADDR_2$, r
1111	F		ANIM M, I	XORR r, M	RN, RNS, CKSTP, NOOP

11. Explanation list of function and operation of instructions (Explanation of symbols)

M	:	Data memory address Normally, one of 00H~3FH address of data memory.
r	:	General register One of 00H~0FH address of data memory.
PC	:	Program counter (11 bits)
STACK	:	Stack register (11 bits)
G	:	G-register (3 bits)
DATA	:	Data register (16 bits)
I	:	Immediate data (4 bits)
N	:	Bit position (4 bits)
—	:	All "0"
C	:	Code No. of port (4bit)
C_N	:	Lower rank 3bit of port code No.
R_N	:	General register No. (4bit)
$ADDR_1$	:	Program memory address in page 0 or 1 (10bit)
$ADDR_2$	:	Higher rank 6bit of program memory address in page 0
Ca	:	Carry
b	:	Borrow
PLL	:	Port treated during the execution of PLL instruction
SEG	:	Port treated during the execution of SEG instruction
MARK	:	Port treated during the execution of MARK instruction
IO	:	Port treated during the execution of IO instruction
KEY	:	Port treated during the execution of KEY instruction
( )	:	Register or data memory content
$[\ ]_C$	:	Content of port indicated by code No. C (4bit)
[ ]	:	Content of data memory indicated by the content of register or data memory
$[\ ]_P$	:	Content of program memory (16bit)
IC	:	Instruction code (6bit)
※	:	Instruction having skip function
D_C	:	Data memory column address (4bit)
D_R	:	Data memory row address (2bit)
P	:	Wait condition select bit at WAIT instruction

(Note) Address 000H~3FFH of program memory address : Page 0 area
Address 400H~7FFH of program memory address : Page 1 area

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
ADDITION INSTRUCTION	AI M, I		Add immediate data to memory	M←(M) + I	000000	D_R	D_C	I
	AIS M, I	※	Add immediate data to memory, then skip if carry	M←(M) + I Skip if carry	000001	D_R	D_C	I
	AIN M, I	※	Add immediate data to memory, then skip if not carry	M←(M) + I Skip if not carry	000010	D_R	D_C	I
	AIC M, I		Add immediate data to memory with carry	M←(M) + I + ca	001000	D_R	D_C	I
	AICS M, I	※	Add immediate data to memory with carry, then skip if carry	M←(M) + I + ca Skip if carry	001001	D_R	D_C	I
	AICN M, I	※	Add immediate data to memory with carry, then skip if not carry	M←(M) + I + ca Skip if not carry	001010	D_R	D_C	I
	AD r, M		Add memory to general register	r←(r) + (M)	010000	D_R	D_C	R_N
	ADS r, M	※	Add memory to general register, then skip if carry	r←(r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN r, M	※	Add memory to general register, then skip if not carry	r←(r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC r, M		Add memory to general register with carry	r←(r) + (M) + ca	011000	D_R	D_C	R_N
	ACS r, M	※	Add memory to general register with carry, then skip if carry	r←(r) + (M) + ca Skip if carry	011001	D_R	D_C	R_N
	ACN r, M	※	Add memory to general register with carry, then skip if not carry	r←(r) + (M) + ca Skip if not carry	011010	D_R	D_C	R_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
SUBTRACTION INSTRUCTION	SI M, I		Subtract immediate data from memory	M←(M) – I	000011	D_R	D_C	I
	SIS M, I	※	Subtract immediate data from memory, then skip if borrow	M←(M) – I Skip if borrow	000100	D_R	D_C	I
	SIN M, I	※	Subtract immediate data from memory, then skip if not borrow	M←(M) – I Skip if not borrow	000101	D_R	D_C	I
	SIB M, I		Subtract immediate data from memory with borrow	M←(M) – I – b	001011	D_R	D_C	I
	SIBS M, I	※	Subtract immediate data from memory with borrow, then skip if borrow	M←(M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN M, I	※	Subtract immediate data from memory with borrow, then skip if not borrow	M←(M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU r, M		Subtract memory from general register	r←(r) – (M)	010011	D_R	D_C	R_N
	SUS r, M	※	Subtract memory from general register, then skip if borrow	r←(r) – (M) Skip if borrow	010100	D_R	D_C	R_N
	SUN r, M	※	Subtract memory from general register, then skip if not borrow	r←(r) – (M) Skip if not borrow	010101	D_R	D_C	R_N
	SB r, M		Subtract memory from general register with borrow	r←(r) – (M) – b	011011	D_R	D_C	R_N
	SBS r, M	※	Subtract memory from general register with borrow, then skip if borrow	r←(r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN r, M	※	Subtract memory from general register with borrow, then skip if not borrow	r←(r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
COMPARISON INSTRUCTION	SLTI M, I	※	Skip if memory is less than immediate data	Skip if (M)<I	110000	D_R	D_C	I
	SGEI M, I	※	Skip if memory is greater than or equal to immediate data	Skip if (M)≧I	110001	D_R	D_C	I
	SEQI M, I	※	Skip if memory is equal to immediate data	Skip if (M)=I	110010	D_R	D_C	I
	SNEI M, I	※	Skip if memory is not equal to immediate data	Skip if (M)≠I	110011	D_R	D_C	I
	SLT r, M	※	Skip if general register is less than memory	Skip if (r)<(M)	110100	D_R	D_C	R_N
	SGE r, M	※	Skip if general register is greater than or equal to memory	Skip if (r)≧(M)	110101	D_R	D_C	R_N
	SEQ r, M	※	Skip if general register is equal to memory	Skip if (r)=(M)	110110	D_R	D_C	R_N
	SNE r, M	※	Skip if general register is not equal to memory	Skip if (r)≠(M)	110111	D_R	D_C	R_N
TRANSFER INSTRUCTION	LD r, M		Load memory to general register	r←(M)	100000	D_R	D_C	R_N
	ST M, r		Store general register to memory	M←(r)	100001	D_R	D_C	R_N
	MVRD r, M		Move memory to destination memory referring to general register in the same row	$[D_R, (r)]$←(M)	100010	D_R	D_C	R_N
	MVRS M, r		Move source memory referring to general register to memory in the same row	M←$[D_R, (r)]$	100011	D_R	D_C	R_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)				
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)	
TRANSFER INSTRUCTION	MVSR M1, M2		Move memory to memory in the same row	$(D_R, D_{C1}) \leftarrow (D_R, D_{C2})$	100100	D_R	D_{C1}	D_{C2}	
	MVIM M, I		Move immediate data to memory	$M \leftarrow I$	100101	D_R	D_C	I	
	MVGD r, M		Move memory to destination memory referring to G-register and general register	$[(G), (r)] \leftarrow (M)$	100110	D_R	D_C	R_N	
	MVGS M, r		Move source memory referring to G-register and general register to memory	$M \leftarrow [(G), (r)]$	100111	D_R	D_C	R_N	
INPUT AND OUTPUT INSTRUCTION	PLL M, C		Input PLL port data to memory	$M \leftarrow [PLL]_C$	101000	D_R	D_C	0	C_N
			Output contents of memory to PLL port	$[PLL]_C \leftarrow (M)$		D_R	D_C	1	C_N
	SEG M, C		Input SEG port data to memory	$M \leftarrow [SEG]_C$	101001	D_R	D_C	0	C_N
			Output contents of memory to SEG port	$[SEG]_C \leftarrow (M)$		D_R	D_C	1	C_N
	MARK M, C		Input MARK port data to memory	$M \leftarrow [MARK]_C$	101010	D_R	D_C	0	C_N
			Output contents of memory to MARK port	$[MARK]_C \leftarrow (M)$		D_R	D_C	1	C_N
	IO M, C		Input IO port data to memory	$M \leftarrow [IO]_C$	101011	D_R	D_C	0	C_N
			Output contents of memory to IO port	$[IO]_C \leftarrow (M)$		D_R	D_C	1	C_N
	KEY M, C		Input KEY port data to memory	$M \leftarrow [KEY]_C$	101100	D_R	D_C	0	C_N
			Output contents of memory to KEY port	$[KEY]_C \leftarrow (M)$		D_R	D_C	1	C_N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
LOGICAL OPERATION INSTRUCTION	ORR r, M		Logical OR of general register and memory	r←(r)∨(M)	010110	D_R	D_C	R_N
	ANDR r, M		Logical AND of general register and memory	r←(r)∧(M)	010111	D_R	D_C	R_N
	ORIM M, I		Logical OR of memory and immediate data	M←(M)∨I	011110	D_R	D_C	I
	ANIM M, I		Logical AND of memory and immediate data	M←(M)∧I	011111	D_R	D_C	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M←(M)⊕I	101110	D_R	D_C	I
	XORR r, M		Logical exclusive OR of general register and memory	r←(r)⊕(M)	101111	D_R	D_C	I
BIT JUDGE INSTRUCTION	TMTR r, M	※	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	111000	D_R	D_C	R_N
	TMFR r, M	※	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	111001	D_R	D_C	R_N
	TMT M, N	※	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	111010	D_R	D_C	N
	TMF M, N	※	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	111011	D_R	D_C	N
	TMTN M, N	※	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	111100	D_R	D_C	N
	TMFN M, N	※	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	111101	D_R	D_C	N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16 bit)			
					IC (6bit)	A (2bit)	B (4bit)	C (4bit)
SUBROUTINE INSTRUCTION	CALL ADDR$_1$		Call subroutine in page 0	STACK←(PC) + 1 and PC←ADDR$_1$ in page 0 or 1	000110	ADDR$_1$ (10 bit)		
			Call subroutine in page 1		000111			
	RN		Return to main routine	PC←(STACK)	111111	00	—	—
	RNS	※	Return to main routine and skip unconditionally	PC←(STACK) and skip	111111	01	—	—
JUMP INST.	JUMP ADDR$_1$		Jump to the address specified in page 0	PC←ADDR$_1$ in page 0 or 1	001110	ADDR$_1$ (10 bit)		
			Jump to the address specified in page 1		001111			
OTHER INSTRUCTION	WAIT P		At P = "0"H, the condition is CPU waiting (Soft wait mode)	Wait at condition P	101101	P	—	—
			At P = "1"H, except for clock generator, all function is waiting (Hard wait mode)				—	—
	DAL ADDR$_2$, r		Load program memory in page 0 to DATA register	DATA←[ADDR$_2$ + (r)]$_P$ in page 0	111110	ADDR$_2$ (6bit)		R_N
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH}$ = "0"	111111	10	—	—
	NOOP		No operation	—	111111	11	—	—

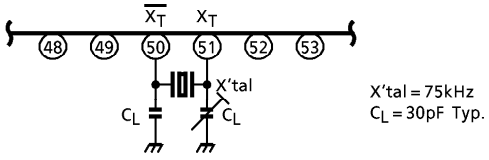
(Note 1) During the execution of input and output instruction, control of input / output instruction is automatically carried out at the most significant bit in Code No. (C) of port.
- MSB = "1" of Code No. (C) : Output instruction
- MSB = "0" of Code No. (C) : Input instruction

(Note 2) In the TC9308AF, the input port treated by the execution of SEG, MARK instruction does not exist, so these input instruction can not be used.

(Note 3) Among 10 bits of the program memory address assigned by DAL instruction, the lower rank of 4 bits become indirect addressing based on the content of general register.
DAL instruction executing time is 160μs.

○ Connection of crystal resonator

Connect 75kHz crystal resonator with the crystal oscillator terminals (XT, $\overline{XT}$ terminal) of the device as shown below. This oscillation signal is supplied to clock generator and reference frequency divider, and produced each timing signal of CPU and reference frequency signal. Adjust the crystal oscillation frequency while monitoring LCD segment output terminal.



(Note) Use crystal resonator of low CI value and satisfactory starting characteristics.

○ System reset

System reset is applied to the device when "L" level is given to $\overline{INT}$ terminal, or when the voltage, 0V→1.8V~3.6V is supplied to V_{DD} terminal (power on reset).
After the lapse of 100ms stand-by time succeeding to the system reset, program starts from zero address.
As power on reset function is employed usually, $\overline{INT}$ terminal is fixed at "H" level.

(Note 1) During the system reset time and the succeeding stand-by time, LCD common output and segment output are fixed at "L" level.

(Note 2) After system reset, all of I/O ports are set at input mode, but initialization of output port and internal port (G-register, etc.) is not carried out. Especially, at the initial power on stage, content of these ports is indefinite, and therefore it is necessary to make initialization with program according to your use.

○ Back up mode

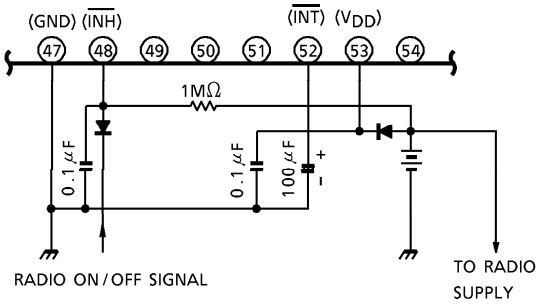
If CKSTP instruction or WAIT instruction is executed when $\overline{INH}$ terminal is at "L" level, it can select for the three kinds of back up mode.

1. Clock stop mode

If CKSTP instruction is executed when $\overline{INH}$ terminal is at "L" level, clock generator and CPU internal of the device stop operation completely, and memory back up state can be realized at low current consumption (1μA MAX. at V_{DD} = 3V).
At this time, LCD display driver terminals and output ports are all fixed at "L" level or off condition. During this clock stop mode, supply voltage can be reduced down to 1.2V and used for exchange of battery.
So this mode is available when the battery is changed in the radio set.
In clock stop mode, program stops at the execution address of CKSTP instruction.
The clock stop mode is released at $\overline{INH}$ = "H" level or changing the input condition of I/O port (IO0~IO3) set at input mode, and the next address is executed after the lapse of stand-by time of 100ms.

(Note 1) In the clock stop mode, the condition of output terminal is all fixed at "L" level or off but output port holds on the data just before clock stop mode.

(Note 2) When CKSTP instruction is executed during $\overline{INH}$ = "H" level, the same operation as NOOP instruction is made (Clock stop mode is not entered).



EXAMPLE OF THE MEMORY BACK UP CIRCUIT USING CAPACITOR AT CLOCK STOP MODE

2. Waiting mode

If WAIT instruction is executed when $\overline{INH}$ terminal is at "L" level, it can select the hardware waiting mode or the software waiting mode.

1) Software waiting mode

If WAIT instruction is executed at designated operand port [P = 0H], only CPU internal of the device stop operation, and software waiting mode can be realized at low current consumption. Since the other part of clock generator and display circuit operate normally, at the time of using the program of clock function, the software waiting mode is effective to realize at low current consumption during the clock operation.

2) Hardware waiting mode

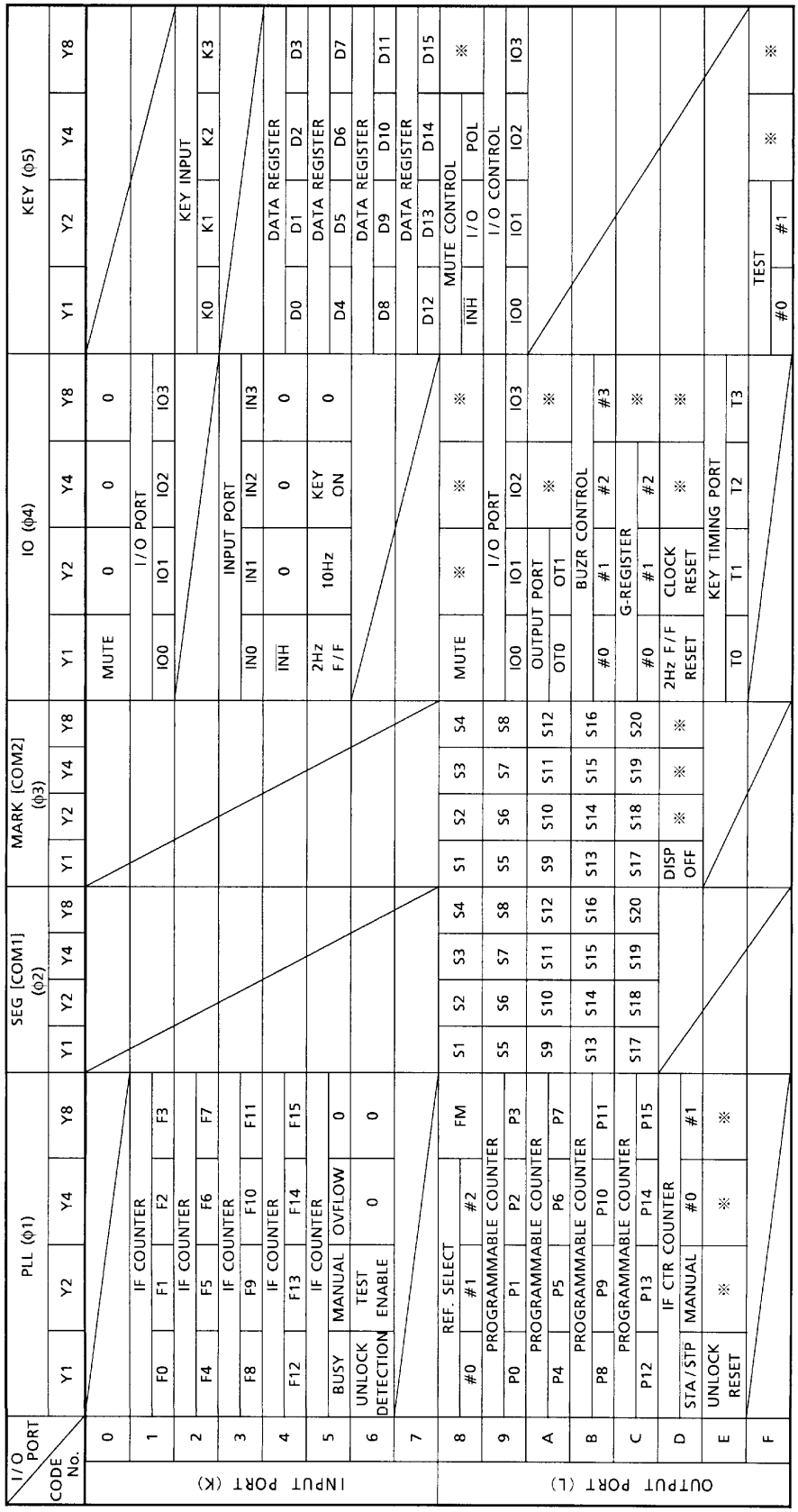
If WAIT instruction is executed at designated operand part [P = 1H], all the function without crystal oscillator are stopped and hardware waiting mode can be realized at lower current consumption than software waiting mode (under 100μA at V_{DD} = 3.0V). At this time, CPU and display circuit stop operation, output terminal for LCD display is fixed at "L" level automatically.
In these waiting mode, program stops at the execution address of WAIT instruction, and waiting is released in following condition, so next address is executed.

3) Released condition of waiting mode

- Changing to $\overline{INH}$ = "H" level
- Key input terminal (K0~K3) is set at "H" level.
- 2Hz timer F/F is set at "1".
- Changing the input condition of I/O port (IO0~IO3) set at input mode
- MUTE port is set at "1".

(Note) In waiting mode, each of output terminal is held on the condition just before waiting mode.

I/O MAP



TC9308AF-21

○ I/O map

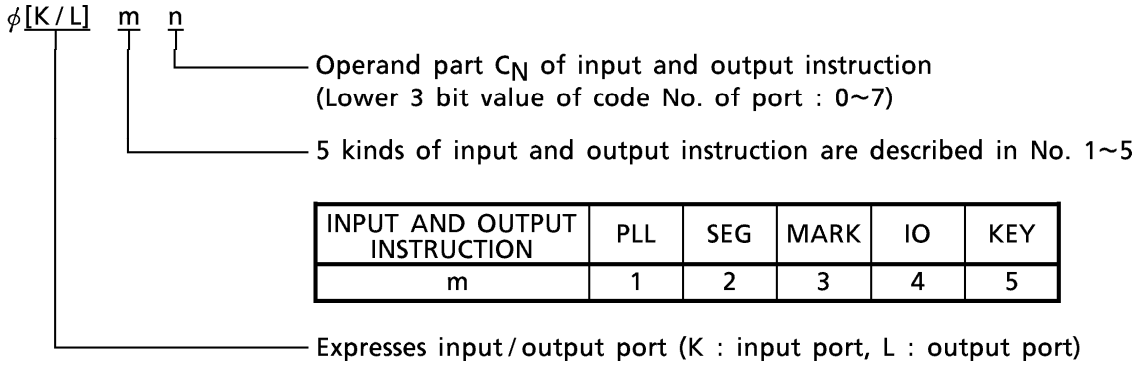
All ports in the device are expressed by matrix of five input and output instruction (PLL instruction, SEG instruction, MARK instruction, IO instruction, KEY instruction) and 4 bits of code No.C. Assignment of these ports is indicated previously as I/O map. In the I/O map, port names treated in the execution of each input and output instruction are assigned horizontally, while code No. of port are assigned vertically. G-register and data register are also treated as port. Basically, the data is treated at each port as 4 bits unit, and code No. (C) = 0H~7H are assigned to input port, while code No. (C) = 8H~FH are assigned to output port.

(Note 1) The port indicated with oblique line on I/O map is a port not existing in the device. In the execution of output instruction, when data is output to the non-existing output port, no effect is given to the content of other port or data memory. When non-existing input port is designated during the execution of input instruction, the content read into the data memory becomes indefinite.

(Note 2) Among the output ports on I/O map, ※ marked port is unused port. The data outputted here becomes "don't care".

(Note 3) Regarding the content of port expressed in 4 bits, Y1 corresponds to the least significant of the data of data memory, and Y8 to the most significant bit. Data of each port is all treated with positive logic.

(Note 4) Each port assigned by five input and output instruction and code No. C is coded as follows :



INPUT AND OUTPUT INSTRUCTION	PLL	SEG	MARK	IO	KEY
m	1	2	3	4	5

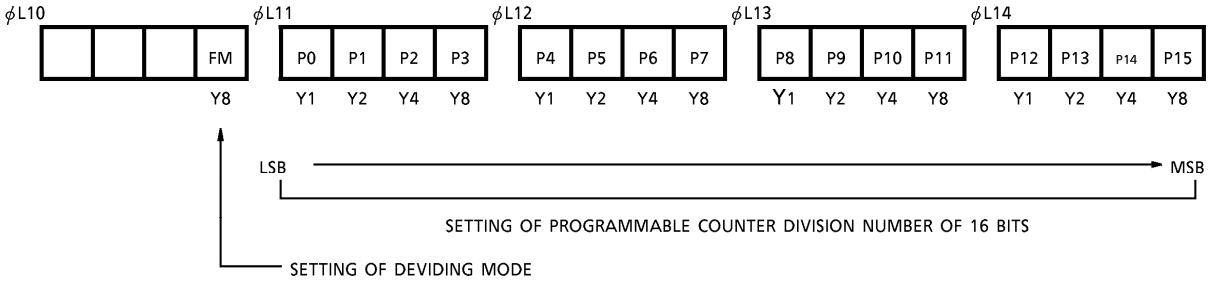
○ Programmable counter

Programmable counter block is composed of external two modulus prescaler TD6134AF, 4 bits + 12 bits programmable binary counter, and PLL output ports to control them.

1. PLL output port (ϕL10~ϕL14)

The exclusive PLL port is used to control the division number and the dividing mode and made access by PLL output instruction designated operand part [C_N = 0~4].

1) Structure of PLL port



2) Setting of dividing mode

Pulse swallow mode or direct dividing mode are selected by FM port. In AM band, it selects the direct dividing mode. In FM or VHF band, it selects pulse swallow mode combined with external two modulus prescaler, TD6134AF.

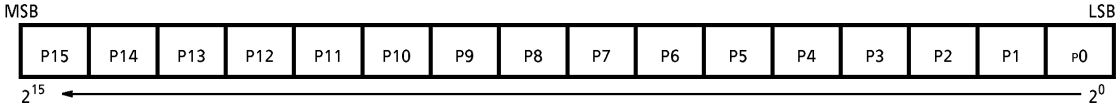
FM	DIVIDING MODE	EXAMPLE OF RECEIVING BAND	OPERATING FREQUENCY RANGE	INPUT TERMINAL	DIVISION NUMBER	PRESCALER
0	Direct Dividing Mode	MW / LW	0.5~2.5MHz	AM_{IN}	n	—
1	1/4×(1/15 or 1/16) Pulse swallow Mode	FM	(Note 1) 50~150MHz	FM_{IN}	(Note 2) 4·n	TD6134AF
	1/8×(1/15 or 1/16) Pulse swallow Mode	VHF	(Note 1) 50~250MHz	FM_{IN}	8·n	

(Note 1) This shows the input frequency range to TD6134AF.
(Note 2) "n" shows the programmed division number.

3) Setting of frequency division number

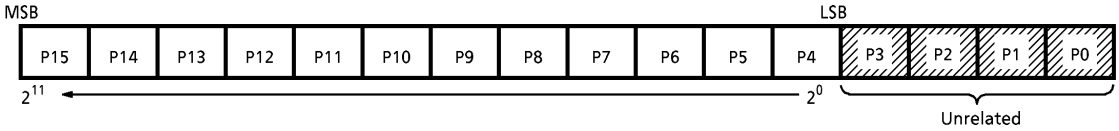
Division number of programmable counter is set on P0~P15 ports with binary.

- Pulse-swallow mode (16bit)



※ Frequency division number setting range (pulse swallow mode)
n = 210H~FFFFH (528~65535)

- Direct dividing mode (12bit)



※ Frequency division number setting range (Direct dividing mode)
n = 10H~FFFH (16~4095)

(Note 1) As the programmable counter is not provided with dividing offset, the programmabled number becomes the actual frequency division number. However, in the case of FM band, the actual frequency division number becomes four times of programmed value, and in VHF band, the actual frequency division number becomes eight times of programmed value in combination with prescaler TD6134AF.

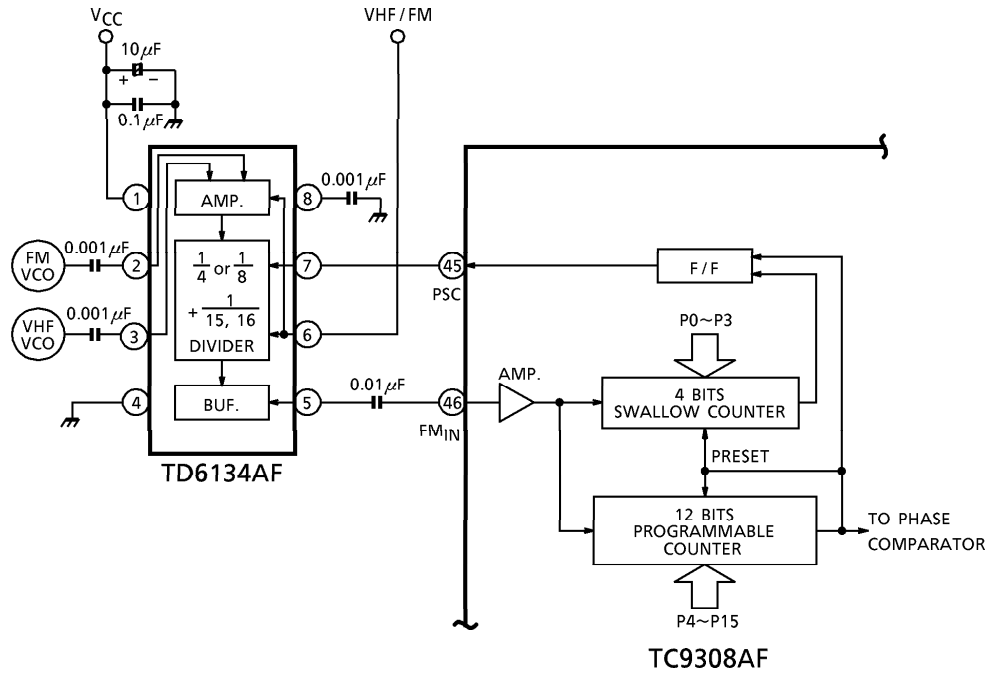
(Note 2) In case of direct dividing mode, P0~P3 port (ϕL11) data becomes unrelated and P4 port becomes LSB.

(Note 3) Frequency division number is entirely renewed at the time of data setting of MSB port (ϕL14).
So this prevents wrong influence from giving to the lock up time.
For this reason, the data of MSB port (ϕL14) must be set at the end of division number. Even when the data setting is considered unnecessary (when the data is same as the previous one), the data setting of MSB port (ϕL41) must be executed.

2. Circuit construction of external prescaler and programmable counter

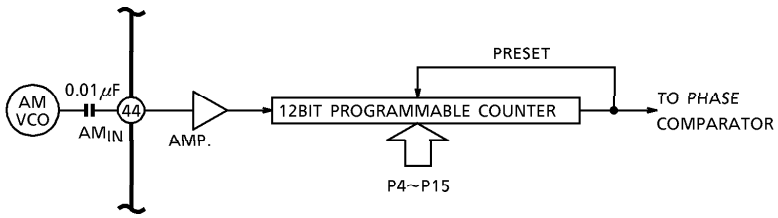
1) Circuit construction of pulse swallow dividing mode

The circuit is composed of (1/4 or 1/8×1/15, 1/16) 2-modulous prescaler TD6134AF and swallow counter of 4 bits and binary programmable counter of 12 bits. In the case of FM band, it selects 1/4 divider to the front stage of 2-modulous prescaler, and in VHF band, it selects 1/8 divider to the front stage of 2-modulous prescaler.
The block diagram including prescaler is shown as follows.



2) Circuit construction of direct dividing mode

In this case, it is unnecessary to use the external prescaler, 12 bits programmable counter is only used.



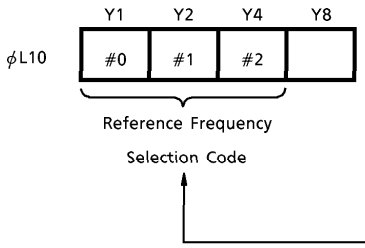
(Note) Both FM_{IN} and AM_{IN} have built-in amplifiers, and the small amplitude operation is possible through the capacitor coupling.

○ Reference frequency divider

This block divides oscillating frequency of external 75kHz crystal, and produces seven kinds of PLL reference signal, 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 12.5kHz, 25kHz. Selection of reference signal is carried out with the data of REF select port.
The selected signal is supplied to the phase comparator as the reference frequency.

1. REF select port (ϕL10)

This is an internal port to select seven kinds of reference frequency signal.
Normally, this port is made access by PLL instruction designated the operand part [$C_N = 0$] (ϕL10).

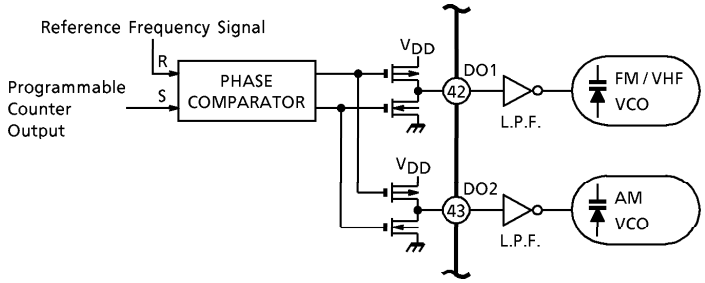


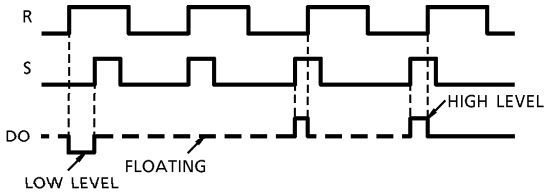
REF. Output Code Table

#2	#1	#0	\	REFERENCE FREQUENCY
0	0	0	0	1kHz
0	0	1	1	3kHz
0	1	0	2	3.125kHz
0	1	1	3	5kHz
1	0	0	4	6.25kHz
1	0	1	5	12.5kHz
1	1	0	6	25kHz
1	1	1	7	REF. output is stopped

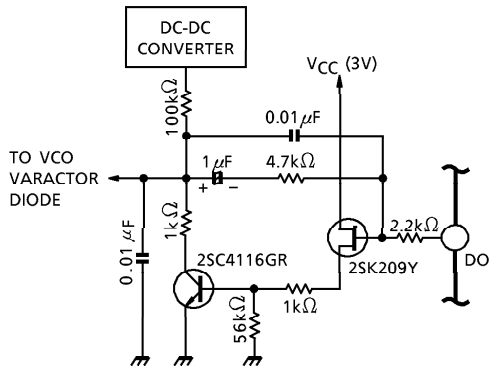
○ Phase comparator

The phase comparator outputs the error amount comparing the phase difference between the reference frequency signal supplied from the reference frequency divider and the programmable counter dividing output. VCO is controlled through low-pass filter so that the frequencies and the phase-difference of these two signals may coincide.
Since two tri-state buffer DO1 and DO2 terminals are parallel output from the phase comparator, the filter constant can be optimumly designed for each band of FM / VHF and AM.





DO Output Timing Chart

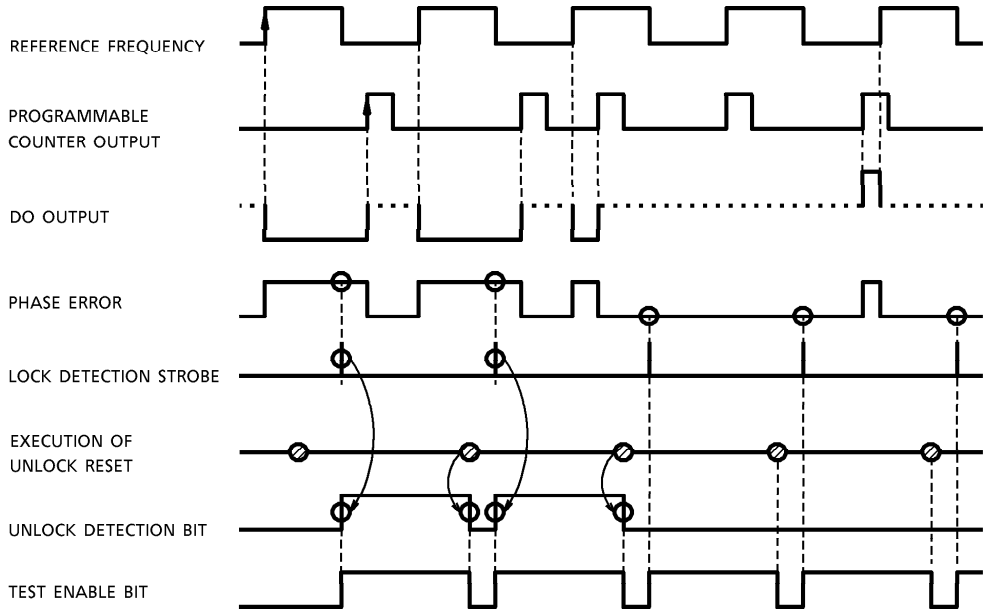


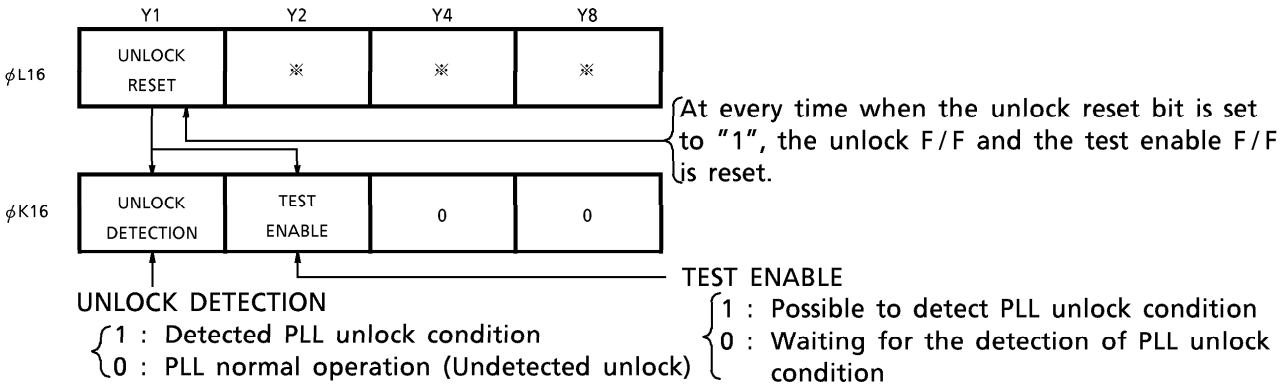
Example of Active LOW-PASS Filter Circuit (for reference)

DO output timing chart and example of active low-pass filter circuit structured by darlington connection of FET and transistor are shown in the above figures.
The filter circuit shown in the above figure is an example for reference, and the actual circuit should be investigated and designed conforming to the system band construction and the required characteristics.

○ Unlock detection bit (ϕLK16)

This is the bit for detecting the locked state of PLL system. When PLL system is unlocked state, namely, in the state in which the reference signal and the dividing frequency of programmable counter do not coincide, the pulse is output from the phase comparator to the unlock F/F with the cycle of the reference frequency.
By this pulse, the unlock F/F is set. At every time when the unlock-reset bit is set to "1" by PLL output instruction designated the operand part [$C_N = 6$], the unlock F/F is reset (ϕL16).
After the unlock F/F is reset, the locked condition can be detected by access the unlock detection bit with PLL input instruction (ϕK16). Since the pulse is input with the cycle of the reference frequency, after the unlock F/F is reset, it is necessary to make access the unlock detection bit after the time exceeding the cycle of the reference frequency. If the time is shorter than the cycle, the correct locked condition can not be detected.
So the test enable F/F is prepared. Every time when the unlock reset bit is set to "1", the test enable F/F is reset and set to "1" with the unlock detection timing. In short, it is able to detect the unlock condition correctly at "1" state of the test enable bit (ϕK16).



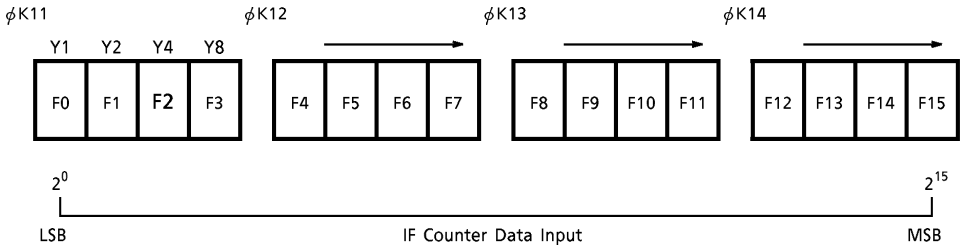


○ General IF counter

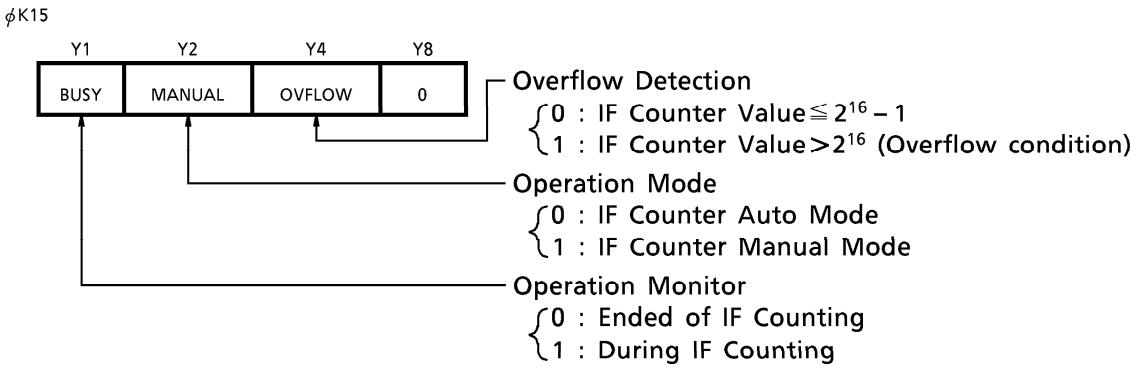
16 bits general IF counter is able to detect the auto-stop signal with counting intermediate frequency (IF) of FM or AM band at auto-tuning mode. The general IF counter is available for auto tuning function of IF counting type easily in combination with TA8132F, a AM / FM IF + MPX IC corresponding to DTS. IF counter block is composed of 16 bits binary counter and the port for IF counter control.

1. IF counter data port (ϕK11~ϕK15)

This is the data input port for input the counted data of IF counter and operating condition. The data is read into data memory by PLL input instruction designated the operand part [C_N = 1~5].



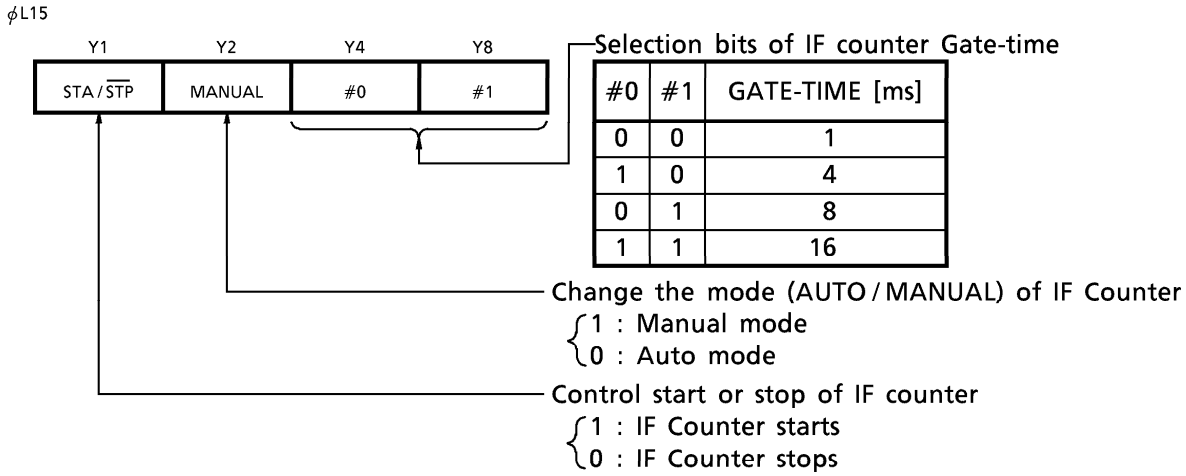
The counted data of IF counter is inputted with binary from the input port, F0~F15.



This is the input port for detecting operation condition of IF counter (ϕK15).
In case of using IF counter, the counted data (F0~F15) should be calculated after confirming "0" of BUSY bit (end of IF counting) and OVFLOW bit (not overflow condition).

2. IF counter control port (ϕL15)

This is the data output port controlled for IF counter operation. This port is made access by PLL output instruction designated the operand part [$C_N = 5$].

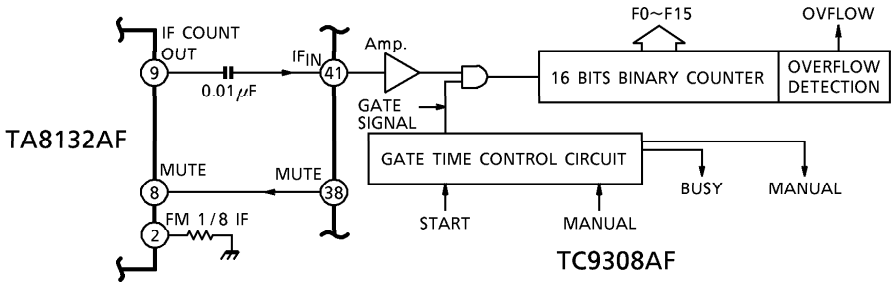


At the auto mode (MANUAL bit is set to "0"), the STA / $\overline{STP}$ bit is set to "1" every time, IF counter starts. IF counter counts during the gate time selected by #0, #1 bits, and it ends automatically.
At manual mode, when the STA / $\overline{STP}$ bit is set to "1", IF counter counts continuously until the STA / $\overline{STP}$ bit is set to "0".

(Note) At $\overline{INH}$ = "0", IF counter is reset by compulsorily.

3. Circuit construction of IF counter

IF counter is composed of input Amp., gate-time control circuit, 16 bits binary counter.



At AM band AM IF signal is input to IF_{IN} (TC9308AF Pin 41) from TA8132AF directly, at FM / VHF band 1 / 8 divided output of FM / VHF IF signal is input to IF_{IN}.

(Note) IF_{IN} terminal has built-in amplifier, and the small amplitude operation is possible through the capacitor coupling.

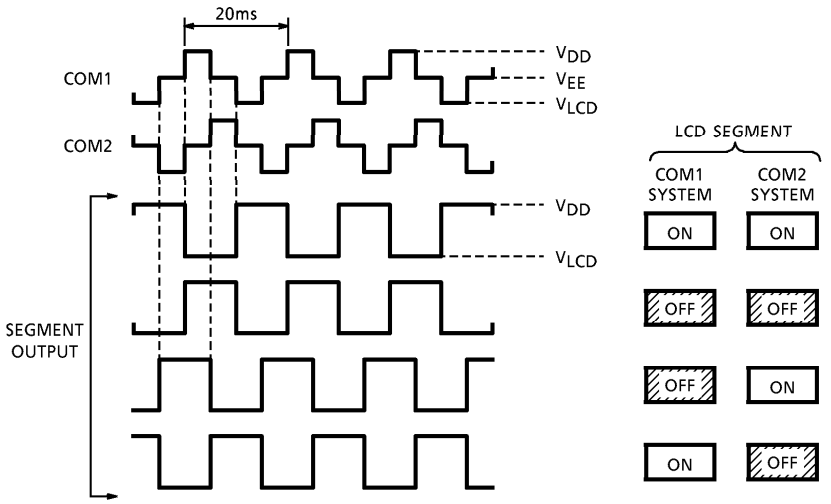
(Note) If it is used without TA8132AF, 1 / 8 divided IF signal should be input to IF_{IN} (TC9308AF Pin 41) at FM / VHF band.
At AM band, IF signal is input directly.

○ LCD driver

The TC9308AF contains LCD driver of 1/2 duty and 1/2 bias driving (frame frequency = 100Hz). Two common terminals (COM1, COM2) output three potentials of voltage, V_{DD}, V_{EE}, V_{LCD} level respectively with 1/4 phase difference.
40 segments can be displayed by the combination of these common outputs and 20 segment outputs (S1~S20). That is to say, both COM1 system segment and COM2 system segment can be displayed by one segment output, what is called dynamic display method.
LCD driver does not contain segment decoder, so 40 segments can be freely used by program for 7-segment display or mark segment display.
COM1 system segment output is controlled by execution of SEG instruction and COM2 system segment output is by execution of MARK instruction.

1. Timing chart of LCD driver

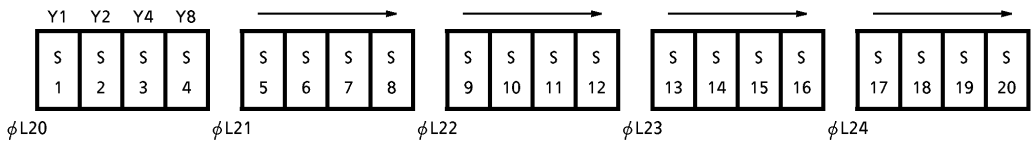
Below are shown the timing chart of COM1, COM2 output wave form and four kinds of segment output wave form.



(Note) During system reset and back up mode (CKSTP instruction executing), common output and segment output are all fixed at "L" lavel automatically.

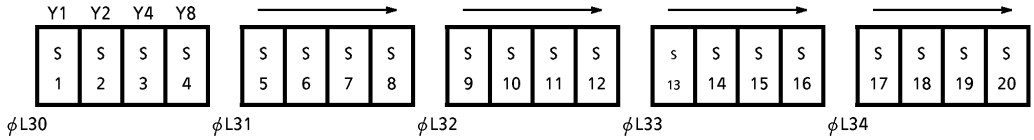
2. COM1 system segment port (ϕL20~ϕL24)

This is a port group to output 20 segment data of COM1 system. It is made access by SEG output instruction. Segment data is treated with 4 bits unit, and COM1 system segment turns "ON" when data "1" is output, while COM1 system segment turns "OFF" when data "0" is output.



3. COM2 system segment port (ϕL30~ϕ34)

This is a port group to output 20 segment data of COM2 system. It is made access by MARK output instruction. Segment data is treated with 4 bits unit, and COM2 system turns "ON" when data "1" is output, while COM2 system segment turns "OFF" when data "0" is output.

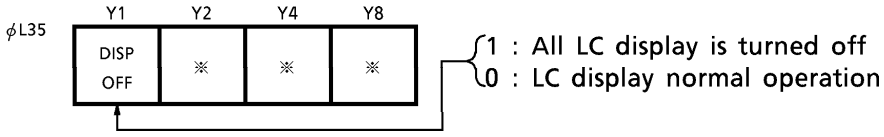


- DISP OFF bit (ϕL35)

This bit controls turning on or off of LC display. When data "1" is set to this bit, common outputs and segment outputs are all fixed at "L" level, all display becomes turned off. When data "0" is set to this bit, display becomes normal action. And this bit is reset to "0" after system reset.

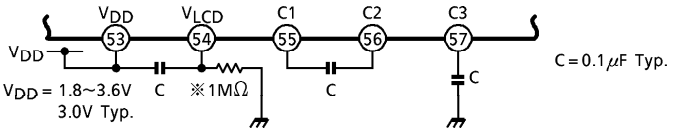
(Note) The name of each port of COM1 system and COM2 system corresponds to the name of segment output terminal, respectively. And as the content of each port don't accept DISP OFF bit's influence, even display off made by DISP OFF bit, it is able to output the data to each segment port normally.

(Note) Decoding of segment can be made by providing the segment decode pattern in the program memory and reading it into the data memory by using DAL instruction. Therefore LCD driver doesn't have built-in segment decoder especially. As DAL instruction refers to the data in the program memory with 16 bits unit, assignment of segment port appropriated to the made 7-segment display is continuously performed with 8 bits unit (7-segment + 1 mark) for example port S1~S4, port S5~S8 both COM1 system and COM2 system in common.



4. Voltage boosting circuit for LC display

TC9308AF has built-in voltage boosting circuit for LC display, it is able to stabilize LC display driving at the low voltage operation. This circuit is composed with 1.5V reference voltage circuit (V_{EE}) and voltage double boosting circuit (V_{LCD}), be connected the boosting capacitor as follows.



※ Be connected the register for improving the motive characteristics of voltage boosting circuit.

○ Input and output port

1. I/O port IO0~IO3 (ϕKL41)

I/O port is 4 bits CMOS type, and is capable of making input and output setting with each bit.
Input and output setting of I/O port is made by the content of I/O control internal port. Setting to input port can be made by setting "0" to the bit of I/O control port corresponding to I/O port, while setting to output port can be made by setting "1" in the same.
In case of input port setting, the present data input I/O port is read into the data memory by the execution of IO input instruction designated the operand part [$C_N = 1$] (ϕK41). At this time, input data is set to output latch of I/O port (ϕL41) in the same.
In case of output port setting, output condition of I/O port is controlled execution of IO output instruction designated the operand part [$C_N = 1$]. And the present output data of I/O port is read into the data memory by the execution of IO input instruction (ϕK41).

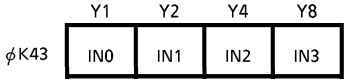
(Note) I/O control port is made access by KEY instruction designated the operand part [$C_N = 1$]. After system reset, the content of this port is all reset to "0", and I/O port is all set up input mode.

(Note) During the clock stop mode (executing CKSTP instruction), output condition of I/O port set at output mode is all fixed at "L" level automatically, but each output latch holds on the data just before the clock stop mode.

(Note) At the time of changing input condition of I/O port set at input mode, it cancels the execution of WAIT and CKSTP instructions and makes the operation restart. In case of setting "1" to I/O-bit of MUTE control port, MUTE port is made to set to "1" compulsorily by the same condition.

2. General input port IN0~IN3 (ϕK43)

IN0~IN3 is input port of 4 bits, CMOS type. By the execution of IO input instruction designated the operand part [$C_N = 3$], input data is read into the data memory. The data is input with positive logic.



3. General output port OT0, OT1 (ϕL42)

OT0 and OT1 are output port of 2 bits, N-ch FET open-drain structure. It is made access by the execution of IO output instruction designated the operand part [$C_N = 2$] (ϕL42). When this port is set to "1", the N-ch transistor turns on, so output becomes "L" level. When this port is set to "0", the N-ch transistor turns off, output becomes high impedance. To make the output "H" level, be connected pull-up resistor. Then output can drive the voltage of 0~12V.

(Note) During the clock stop mode (executing CKSTP instruction), OT0, OT1 output is off condition automatically, but the content of port is held on the previous data.

	Y1	Y2	Y4	Y8
ϕL42	OT0	OT1	※	※

4. Key timing output port T0~T3 (ϕL46)

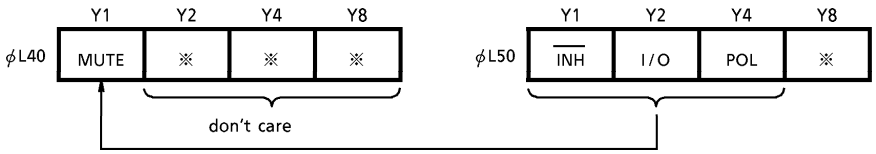
T0~T3 is exclusive output port of 4 bits, CMOS type. Normally, it is used as output of key return timing signal for key matrix. So, the resistor is built-in at Nch transistor side and sink current is decreased.
Therefore, of using push key, the diode can be omitted on the key matrix. Output port is made access by IO output instruction designated the operand part [$C_N = 6$] (ϕL46). In case of using for normal output port, take care to make the external circuit because of output impedance of "L" level increased.

(Note) During the clock stop mode (executing CKSTP instruction), T0~T3 output is fixed at "L" level automatically, but the content of port is held on the previous data.

	Y1	Y2	Y4	Y8
ϕL46	T0	T1	T2	T3

5. MUTE port (ϕKL40)

This is a 1bit CMOS type exclusive output for muting control. Normally, it is made access by IO output instruction designated operand part [$C_N = 0$] (ϕL40).
Further, by the execution of IO input instruction designated operand part [$C_N = 0$], content of present output data is read into data memory (ϕK40).
And according to the data of MUTE control port (ϕL50), MUTE port is controlled.



- $\overline{INH}$ Bit

  In case of setting "1" to this bit, MUTE port is set to "1" compulsorily by changing of $\overline{INH}$ input level ("L"→"H" or "H"→"L").

- I/O Bit

  In case of setting "1" to this bit, MUTE port is set to "L" compulsorily by input level changing of I/O port set at input mode.

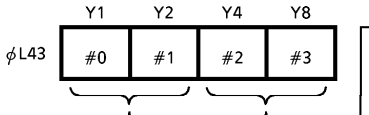
- POL Bit

  The bit controls output polarity of MUTE port. In case of setting "0" to this bit, the data of MUTE port is output with positive logic. In case of setting "1" to the bit, the data of MUTE port is output with negative logic.

(Note) After system reset, the content of $\overline{INH}$, I/O, POL each bit is reset to "0".

○ Buzzer port

Buzzer output is available as beep sound for confirmation of key operation, and as alarm sound. It uses as 1bit general output port. The buzzer output condition is controlled by buzzer control port (ϕL43) as follows. Buzzer control port is made access by IO output instruction designated the operand part [$C_N = 3$].



Selection Bits of Buzzer Port Output Mode

#2	#3	BUZZER OUTPUT MODE
0	0	Single Output (Mode A)
1	0	Continuous Output (Mode B)
0	1	Continuous Output for 100ms Period (At intervals of 50ms) (Mode C)
1	1	Continuous Output for 100ms Period and At intervals of 500ms (Mode D)

Selection Bits of Buzzer Frequency

#0	#1	BUZZER FREQUENCY [kHz]
0	0	Don't use
1	0	1
0	1	1.5
1	1	3

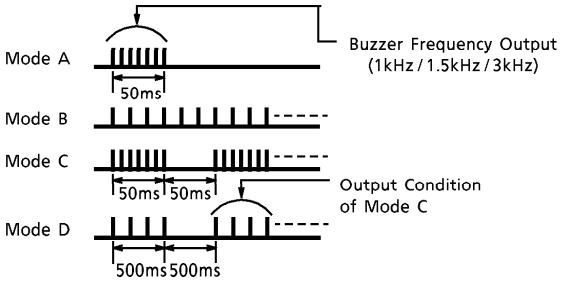
(Note) In case of using buzzer port as general output port, the following data is set to buzzer control port.

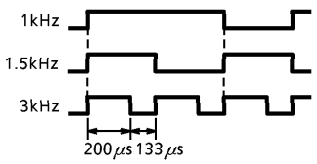
#0	#1	#2	#3	OUTPUT CONDITION OF BUZZER PORT
0	0	0	0	L
0	0	1	0	H

(Note) In case of setting all "0" to the buzzer control port and of executing CKSTP or WAIT (at P = 1H) instruction, buzzer output is reset.

(Note) In case of using as general output port, output is fixed at "L" level by executing CKSTP instruction, but the content of this port is held on.

Below are shown the timing chart of buzzer signal output and buzzer frequency wave form.





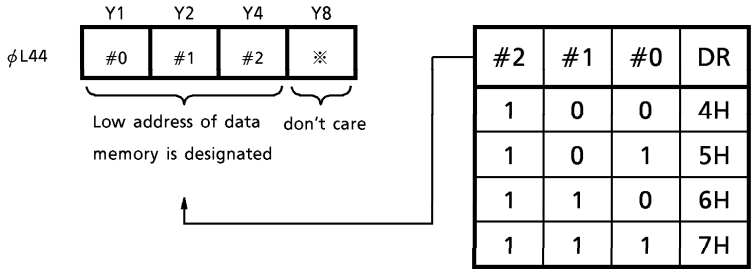
○ Register port

G-register and data register stated in the explanation of CPU are also treated as one of internal ports.

1. G-register (ϕL44)

This is a register to make addressing of low address (D_R = 4H~7H) of data memory during the execution of MVGD instruction and MVGS instruction. This register is made access by IO output instruction designated the operand part [C_N = 4].

(Note) Content of this register is effective only during the execution of MVGD instruction and MVGS instruction, and gives no effect during the execution of other instructions.

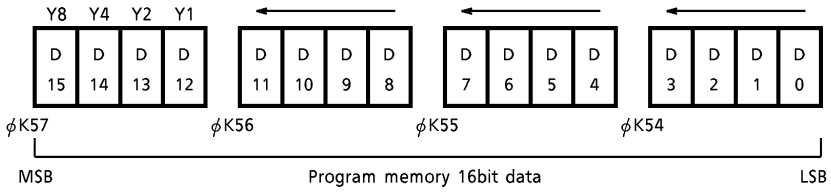


#2	#1	#0	DR
1	0	0	4H
1	0	1	5H
1	1	0	6H
1	1	1	7H

(NOTE) It is possible to indirectly designate all low address of data memory by setting data 0H~7H on G-register. (D_R = 0H~7H)

2. Data register (ϕK54~ϕK57)

This is 16bit register on which the data of program memory is loaded by the execution of DAL instruction. Content of this register is read into the data memory in 4bit unit by the execution of KEY input instruction designated the operand part [C_N = 4~7].
This register is available for the decoding of LCD segment, or for the taking of band edge data of radio and coefficient data during binary to BCD conversion.

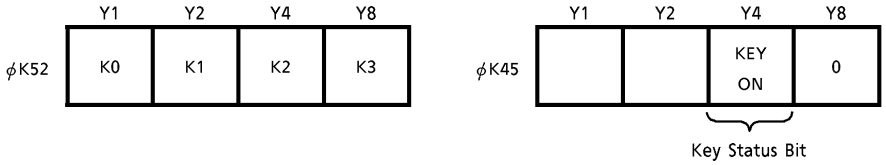


○ Key input

Exclusive 4 bits key input terminal for key matrix data input is provided. Four terminals contain pulldown resistors.

1. Key input port (ϕK52)

   This is exclusive key input port of 4 bits, the data of key input terminal is read into the data memory by the execution of KEY input instruction designated part [$C_N = 2$].



2. Key status bit (ϕK45)

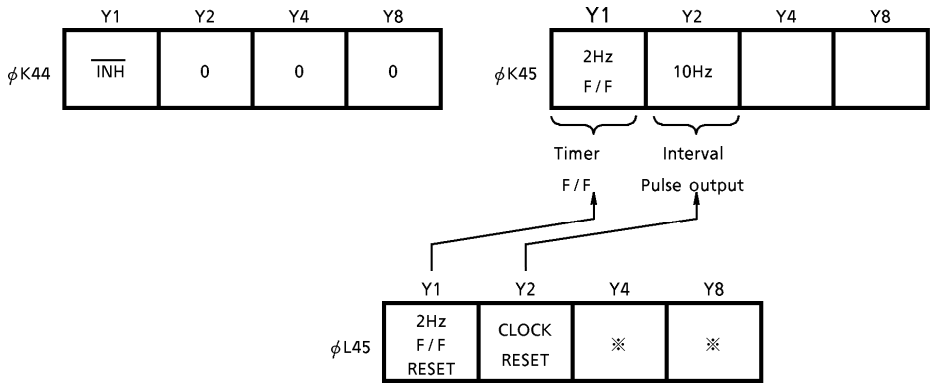
   Key status bit (KEY ON) is provided for purpose of knowing the outline of present key input status. Content of this bit is read into data memory by execution of IO instruction designated operand part [$C_N = 5$].

   - KEY ON bit

     Logical OR of four input data of K0~K3 terminals is output. This is available for judging existance of key input. When KEY ON bit is "1" (In case of inputting "H" level to key input terminal K0~K3), it releases execution of WAIT instruction, the operation is removed.

○ Internal control port

Internal control port is used for reading into data memory the inside condition of device which must be known in the execution of program, or for resetting the inside condition of device.



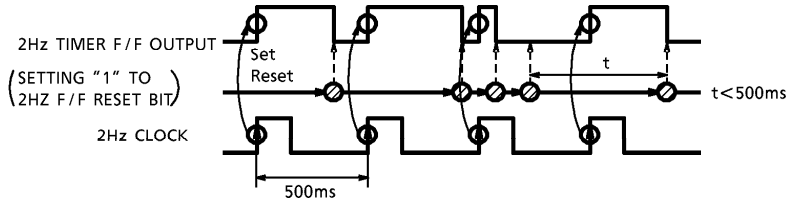
1. $\overline{INH}$ input port (ϕK44)

   This is an input port for inputting the data of $\overline{INH}$ input terminal. Content of this port is read into the data memory by IO instruction designated the operand part [$C_N = 4$]. Data "1" and "0" represent radio "ON" mode and "OFF" mode, respectively.
   At radio off mode, it stops operating of PLL and IF counter block. When $\overline{INH}$ bit of MUTE control port is "1", MUTE port is set to "1" compulsorily by changing the data of $\overline{INH}$ input port. At $\overline{INH}$ input port is "1", it releases execution of CKSTP instruction and the operation is removed. By changing the condition of $\overline{INH}$ input port, execution of WAIT instruction is released.

2. 2Hz timer F/F (ϕK45)

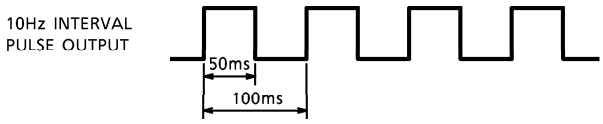
   2Hz timer F/F is set by 2Hz (500ms) signal. With the execution of IO output instruction designated the operand part [$C_N = 5$] this timer is reset by setting data "1" to 2Hz F/F RESET bit. This F/F output is read into the data memory by execution of IO input instruction designated the operand part [$C_N = 5$].
   As 2Hz timer F/F is automatically set every 500ms, it is usually available for counting of clock.
   Since 2Hz timer F/F is reset only by 2Hz F/F RESET bit, count error takes place unless data "1" is set to 2Hz F/F RESET bit within 500ms period, and correct times is not obtainable.

(Note) Condition of 2Hz timer F/F output becomes "0" at power on reset or after execution of CKSTP instruction.



3. 10Hz interval pulse (ϕK45)

10Hz interval pulse is output to 10Hz bit with 100ms period, duty 50% pulse. This is read into the data memory by the execution of IO input instruction designated the operand part [C_N = 5]. This output has no flip flop and is available for mute time counting etc.



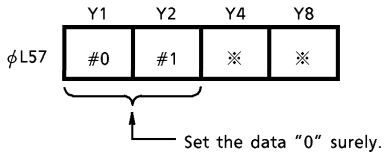
4. Other control bit (ϕL45)

- CLOCK RESET bit

  Every time data "1" is set to this bit, clock of under 50Hz is reset (10Hz interval pulse is also reset). This bit is used for adjusting time of clock.
  Accuracy of clock at this time is −0, +0.02 second.

5. TEST port (ϕL57)

This is an internal port for testing function of device. It is made access by KEY output instruction designated the operand part [C_N = 7]. Never fail to set data "0" in ordinary program.

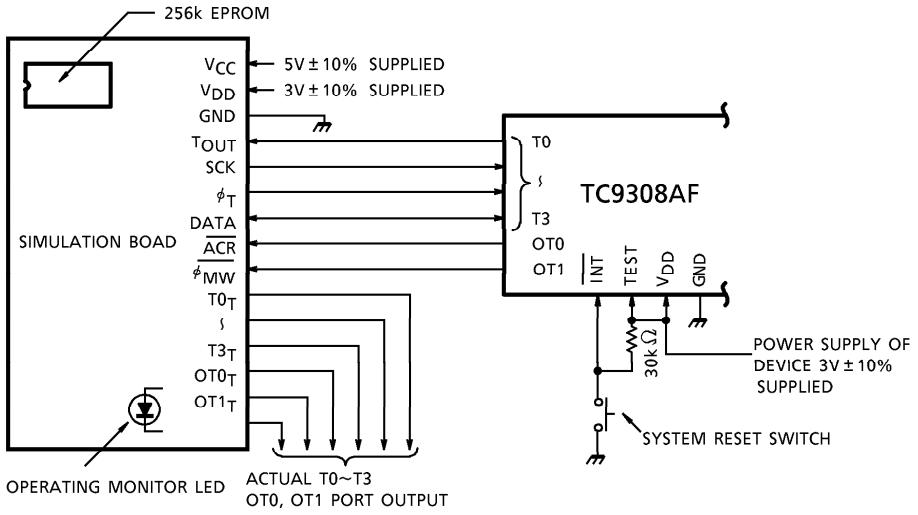


○ Application to evaluator chip

When "H" level is supplied to TEST terminal (Test mode), device operates as evaluator chip, and functional evaluation of developing program can be made by utilizing external simulation board and EPROM. In the test mode, the device operates with the program written in EPROM, irrespective of the content of program memory in the device.

As key timing output port (T0~T3) and output port (OT0, OT1) are transferred to the input and output terminal for control of simulation board at this time, actual T0~T3 and OT0, OT1 port signal are output from the simulation board side.

Below is shown connection diagram of the device and simulation board in case that it is used as evaluator chip.



(Note) Supply 3V±10% voltage to the device and 5V±10% voltage to the simulation board even during back-up mode.

(Note) Each terminal of the device except that shown above can be used normally.

(Note) In case of back-up mode (execution of CKSTP instruction), operating monitor LED on the simulation board turns off.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3~4.0	V
Input Voltage	V_{IN}	− 0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	100	mW
Operating Temperature	T_{opr}	− 10~60	°C
Storage Temperature	T_{stg}	− 55~125	°C
Open Drain Output Breakdown Voltage	V_{BDS}	12	V

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 3.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage Range	V_{DD}	—	※	1.8	3.0	3.6	V
Memory Holding Voltage Range	V_{HD}	—	Crystal oscillation stops (Excuting CKSTP instruction)※	1.2	~	3.6	
Operating Power Supply Current	I_{DD1}	—	Normal operation, output No-load	—	0.7	2.0	mA
	I_{DD2}	—	At only CPU operation (Radio off, lighting display)	—	75	150	μA
	I_{DD3}	—	At stand-by mode (Radio off, only crystal oscillation)	—	50	100	
Memory Holding Power Supply Current	I_{HD}	—	Crystal oscillation stop (Excuting CKSTP instruction)	—	0.1	1.0	
Crystal Oscillation Frequency	f_{XT}	—	※	—	75	—	kHz
Crystal Oscillation Starting Time	t_{ST}	—	Crystal oscillation = 75kHz	—	—	1.0	s

VOLTAGE DOUBLE BOOSTING CIRCUIT

Voltage Double Reference Voltage	V_{EE}	—	V_{DD} reference	1.2	1.5	1.8	V
Voltage Double Boosting Voltage	V_{LCD}	—	V_{DD} reference	2.4	3.0	3.6	

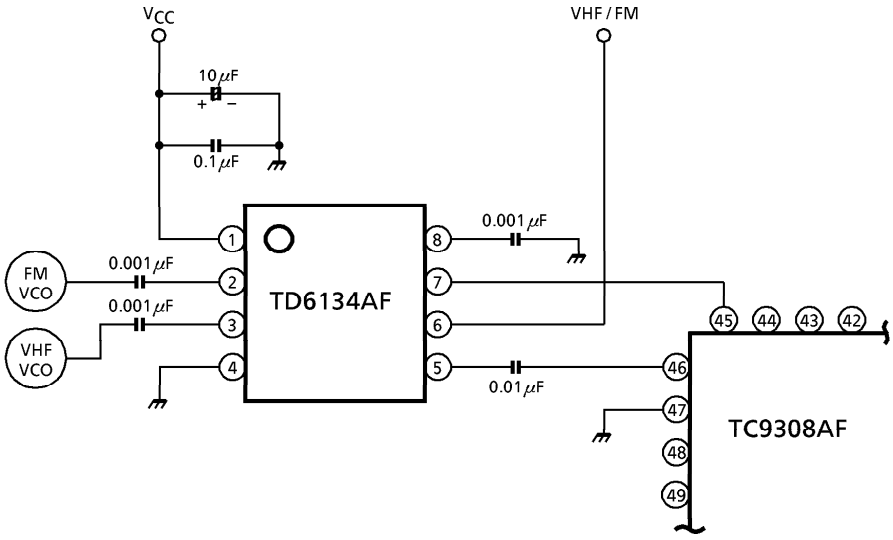
※ Marked items are guaranteed by all conditions of V_{DD} = 1.8~3.6V, Ta = − 10~60°C

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PROGRAMMABLE COUNTER, IF COUNTER							
Operating Frequency Range	f_{IN1}	—	V_{IN} = 0.3V_{p-p} (FM_{IN}, AM_{IN}) ※	0.5	~	25	MHz
	f_{IN2}	—	V_{IN} = 0.3V_{p-p} (IF_{IN}) ※	0.35	~	20	
Operating Input Amplitude Range	V_{IN1}	—	f_{IN} = 0.5~2.5MHz (FM_{IN}, AM_{IN}) ※	0.3	~	V_{DD} – 0.3	V_{p-p}
	V_{IN2}	—	f_{IN} = 0.35~2.0MHz (IF_{IN}) ※	0.3	~	V_{DD} – 0.3	
FM_{IN}-PSC Propagation Delay Time	t_{pd}	—	V_{IN} = 0.3V_{p-p} C_L = 15pF (FM_{IN}) ※	—	—	400	ns
PSC Maximum Load Capacity	C_L	—	(PSC) ※	—	—	15	pF
LCD COMMON OUTPUT							
Output Current	"H" Level	I_{OH1}	—	V_{LCD} = 0V, V_{OH} = 2.7V (COM1, 2)	– 100	– 200	—	μA
	"L" Level	I_{OL1}	—	V_{LCD} = 0V, V_{OL} = 0.3V (COM1, 2)	100	200	—	
LCD SEGMENT OUTPUT							
Output Current	"H" Level	I_{OH2}	—	V_{LCD} = 0V, V_{OH} = 2.7V (S1~S20)	– 50	– 100	—	μA
	"L" Level	I_{OL2}	—	V_{LCD} = 0V, V_{OL} = 0.3V (S1~S20)	50	100	—	
KEY RETURN OUTPUT PORT							
Output Current	"H" Level	I_{OH3}	—	V_{OH} = 2.7V (T0~T3)	– 0.5	– 1.0	—	mA
N-ch FET Side Load Resistance		R_{ON}	—	V_{OL} = 3.0V (T0~T3)	37	70	140	kΩ
MUTE, BUZR, PSC OUTPUT							
Output Current	"H" Level	I_{OH4}	—	V_{OH} = 2.7V	– 300	– 600	—	μA
	"L" Level	I_{OL4}	—	V_{OL} = 0.3V	300	600	—	
GENERAL PURPOSE OUTPUT PORT							
Output Current	"L" Level	I_{OL4}	—	V_{OL} = 0.3V (OT0, OT1)	300	600	—	μA
Output Off-Leakage Current		I_{LDS}	—	V_{DS} = 12V (OT0, OT1)	—	—	1.0	

※ Marked items are guaranteed by all conditions of V_{DD} = 1.8~3.6V, Ta = – 10~60°C

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DO1, 2 OUTPUT								
Output Current	"H" Level	I_{OH4}	—	V_{OH} = 2.7V	− 300	− 600	—	μA
	"L" Level	I_{OL4}	—	V_{OL} = 0.3V	300	600	—	
Output Off-Leakage Current		I_{TL}	—	V_{TLH} = 3.0V, V_{TLL} = 0V	—	—	± 100	nA
GENERAL PURPOSE I/O PORT								
Output Current	"H" Level	I_{OH4}	—	V_{OH} = 2.7V (IO0~IO3)	− 300	− 600	—	μA
	"L" Level	I_{OL4}	—	V_{OL} = 0.3V (IO0~IO3)	300	600	—	
Input Leakage Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V	—	—	± 1.0	
Input Voltage	"H" Level	V_{IH1}	—	(IO0~IO3)	2.4	~	3.0	V
	"L" Level	V_{IL1}	—	(IO0~IO3)	0	~	0.6	
$\overline{INT}$ INPUT, GENERAL PURPOSE INPUT PORT								
Input Leakage Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	($\overline{INT}$, IN0~IN3)	2.4	~	3.0	V
	"L" Level	V_{IL2}	—	($\overline{INT}$, IN0~IN3)	0	~	0.6	
KEY INPUT PORT								
Input Pull-down Resistance		R_{IN1}	—	(K0~K3)	80	140	280	kΩ
Input Voltage	"H" Level	V_{IH3}	—	(K0~K3)	2.1	~	3.0	V
	"L" Level	V_{IL3}	—	(K0~K3)	0	~	0.6	
$\overline{INH}$ INPUT PORT								
Input Leakage Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH4}	—	—	2.6	~	3.0	V
	"L" Level	V_{IL4}	—	—	0	~	1.2	
OTHERS								
Input Pull-down Resistance		R_{IN2}	—	(TEST)	25	45	90	kΩ
X_T Input Feedback Resistance		R_{fXT}	—	(X_T-$\overline{X_T}$)	2.5	10	15	MΩ
$\overline{X_T}$ Output Resistance		R_{OUT}	—	($\overline{X_T}$)	50	100	200	kΩ

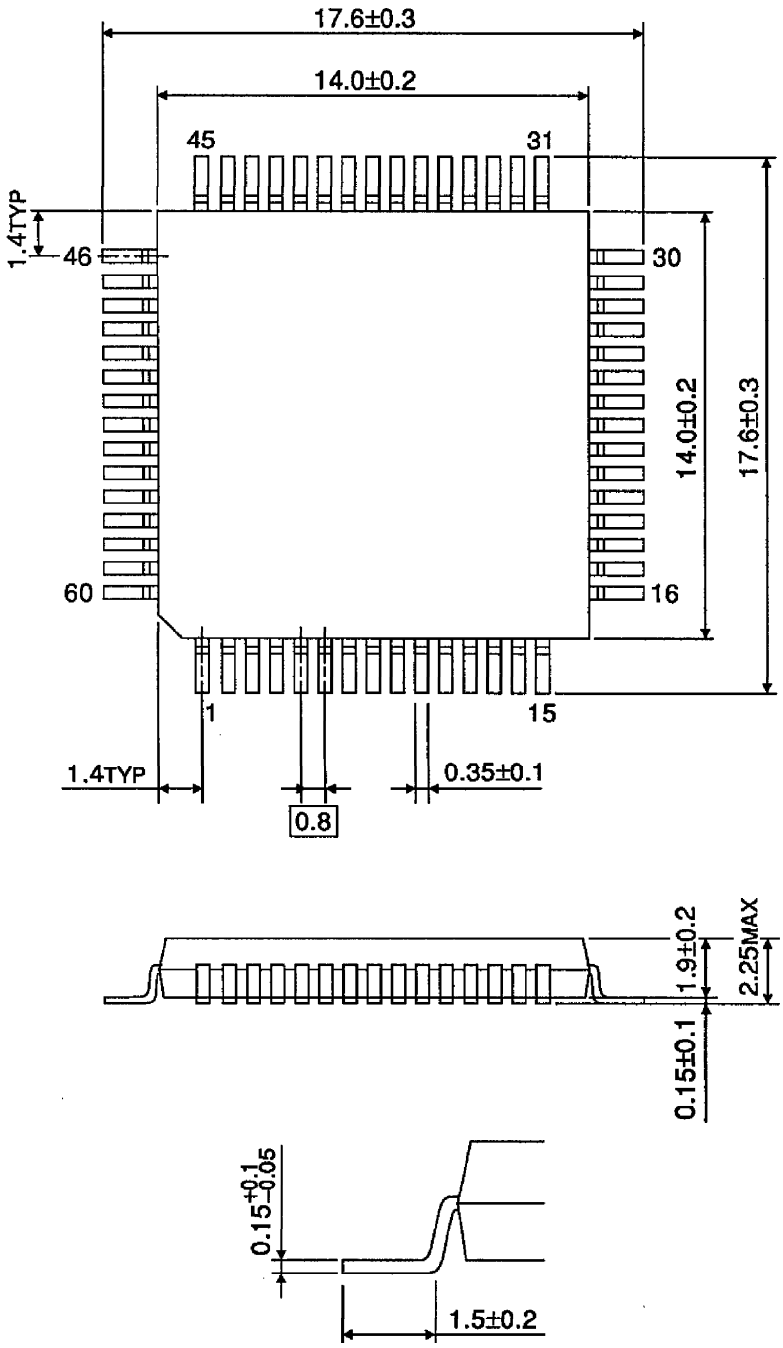
EXAMPLE FOR CONNECT WITH PRESCALER TD6134AF



OUTLINE DRAWING

QFP60-P-1414-0.80A

Unit : mm



Weight : 0.85g (Typ.)