TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

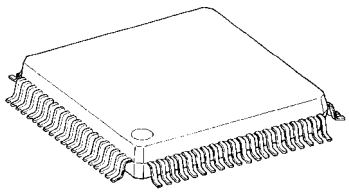
TC9317F

DTS Microcontroller (DTS-21)

The TC9317F is a 4 bit CMOS microcontroller for digital tuning systems. It is capable of functioning at a low voltage of 3 V and features a built-in PLL and LCD drivers.

The CPU has 4 bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AND), composite judging and compare instructions (e.g., TM, SL), and time-base functions.

The package is an pin 80, 0.5-mm-pitch quad flat pack package. In addition to various input/output ports and a dedicated key-input port, which are controlled by powerful input/output instructions (IN 1 to 3, OUT 1 to 3), there are many dedicated LCD pins, a PWM output port, a buzzer port, a 6 bit A/D converter, a serial interface, an IF counter, and other pins. A digital tuning system (DTS) is formed in conjunction with prescalers TD6134AF, TD7101F, or TD7103F.



LQFP80-P-1212-0.50A

Weight: 0.45 g (typ.)

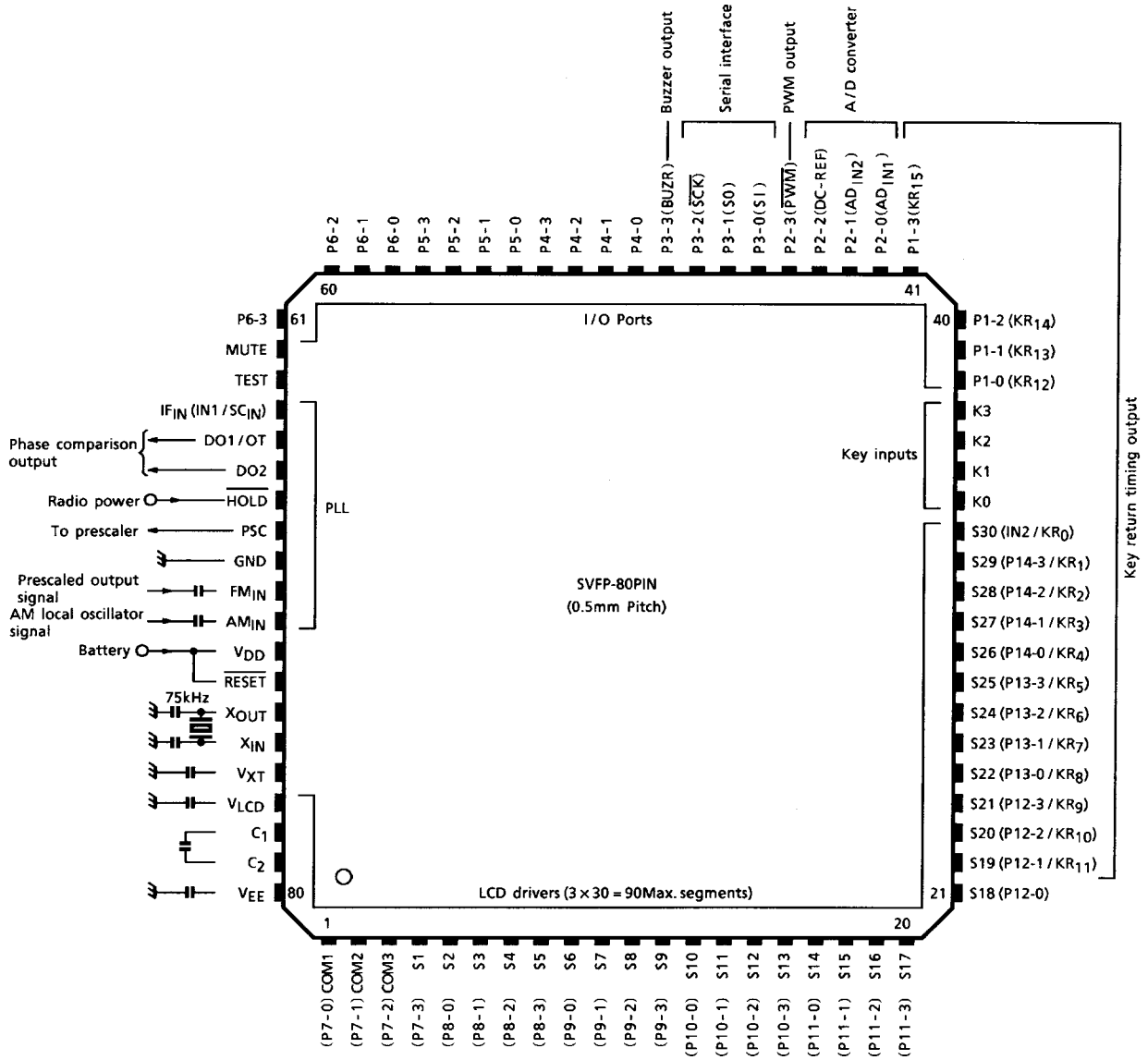
Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.

Features

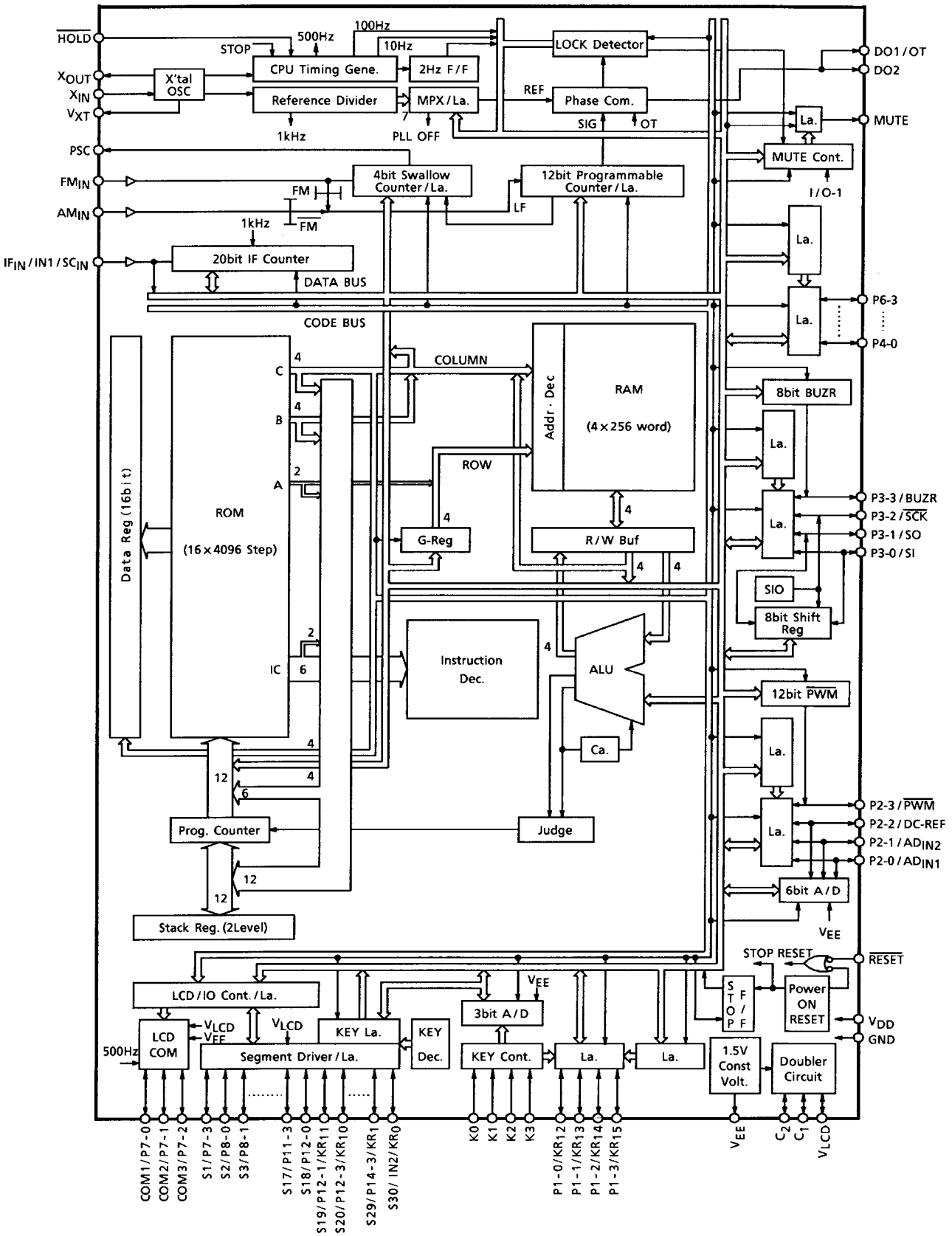
- 4 bit microcontroller for digital tuning systems.
- Operating voltage V_{DD} = 1.8 to 3.6 V, with low current consumption because of CMOS circuitry (with only CPU operating, when V_{DD} = 3 V, I_{DD} = 100 μA max)
- Features built-in 1/3-duty, 1/2-bias LCD drivers and a built-in 3 V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM): 16 bit × 4096 steps
- Data memory (RAM): 4 bit × 256 words
- 62-instruction set (all one-word instructions)
- Instruction execution time: 40 μs (with 75 kHz crystal) (MVGS, DAL instructions: 80 μs)
- Many addition and subtraction instructions (12 types addition, 12 types subtraction)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row.
- Register indirect transfer available (MVGD, MVGS).
- 16 powerful general registers (located in RAM)
- Stack levels: 2
- JUMP or CAL instruction can be used anywhere in the 4096 steps of program memory (ROM) as there are no pages or fields.
- 16 bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Features independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparison outputs for FM and AM.
- In FM or TV mode, a swallow counter is formed with prescalers TD6134AF, TD7101F or TD7103F, and signals of up to 250 MHz can be received.
- Seven reference frequencies can be selected by program.
- Powerful input/output instructions (IN 1 to 3, OUT 1 to 3)
- Dedicated input ports (K_0 to K_3) for key input. 33 LCD drive pins (90 segments maximum) available.
- 25 I/O ports: 24 with input/output programmable in 1 bit units, and one output-only port. The three IF_{IN1}, IF_{IN2}, and DO1 pins can be switched by instruction to IN1 (input-only) or OT (output-only). All LCD output pins can be switched in 1 bit units to I/O ports. (the S30 pin switches to an IN port).

- Three back-up modes available by instruction: Only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2 Hz timer F/F and a built-in 10/100 Hz interval pulse output (internal port for time base).
- Allows PLL lock status detection.
- 12 of the LCD segment outputs (S19t to S30) can also operate as key return timing outputs (KR0 to KR11). The I/O ports are not dedicated key return timing outputs but can have other uses as well.
- Built-in 20 bit, general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8 bit buzzer output circuit can produce 254 different tone signals.
- Built-in 12 bit PWM circuit can be used as a simple DA converter.
- Features a built-in 2-channel, 6 bit AD converter.
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5 V.

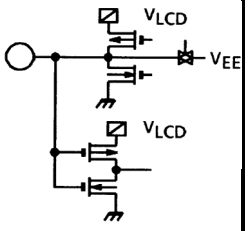
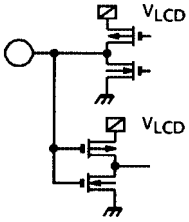
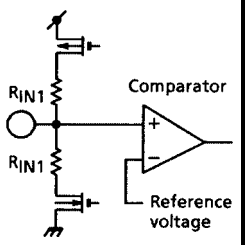
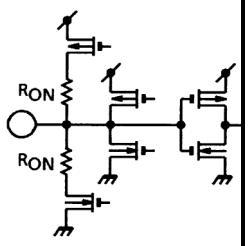
Pin Assignment (top view)

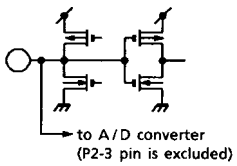
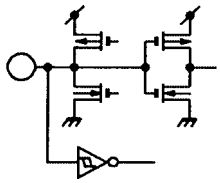
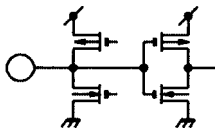
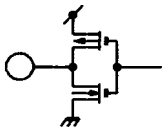
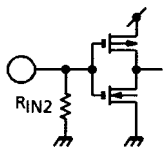


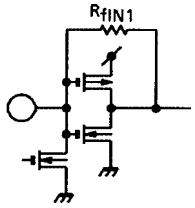
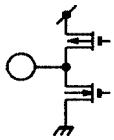
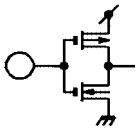
Block Diagram

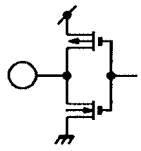
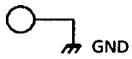
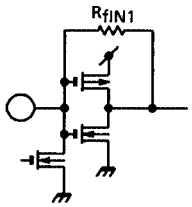
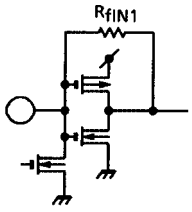
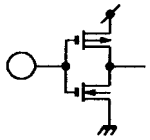


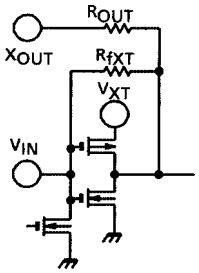
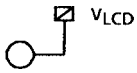
Pin Function

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	COM1/P7-0	LCD common output/input-output ports	Output common signals to the LCD panel. Through a matrix with pins S1 to S30, a maximum of 90 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 83 Hz every 2 ms. V_{EE} is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". These pins can also be programmed as I/O ports.	
2	COM2/P7-1			
3	COM3/P7-2			
4~21	S1/P7-3~ S18/P12-0	LCD segment output/input-output ports	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 90 segments. These pins can also be programmed as I/O ports. (port S30, however, can only be programmed as an input pin). The signals for the key matrix and the segment signals from pins S19/KR11 to S30/KR0 are output on a time division basis. $4 \times 12 = 48$ key matrix can be created in conjunction with key input ports K_0 to K_3.	
22~33	S19/P12-1 /KR11~ S30/IN2/KR0	LCD segment output/input-output ports (IN port)/Key return timing output		
34~37	K0~K3	Key input ports	4 bit input ports for key matrix input. When the key return timing outputs (KR0 to KR11) of the LCD segment pins are combined in a matrix with the key return timing outputs (KR12 to KR15) I/O port 1 (P1-0 to P1-3) pins, data from a maximum of $4 \times 16 = 64$ keys can be input. An A/D comparator with a programmable 3 bit threshold level is used as the input circuit. Input is selectable between pull-down, pull-up, or high impedance, making it possible to construct different types of key matrices. These key input ports may also be used as a sequential compare method 4-channel, 3 bit A/D converter. The WAIT mode is released when high level is applied to key input ports set to pull-down.	
38~41	P1-0/KR12~ P1-3/KR15	Input/output port 1/Key return timing output port	The input and output of these 4 bit I/O ports can be programmed in 1 bit units. Can be programmed to output key matrix timing signals. To form the key matrix, load resistance has been built into both the N-channel and P-channel sides. A key matrix combined with the LCD segment output can be formed, as well as a push-key matrix that does not need a key matrix diode. By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1".	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
42~45	P2-0/AD_{IN1} P2-1/AD_{IN2} P2-2 /DC-REF P2 - 3/$\overline{PWM}$	I/O port 2/A/D analog voltage input /A/D analog voltage input /Reference voltage input /PWM output	4 bit I/O ports. Input and output may be programmed in 1 bit units. Pins P2-0 through P2-2 can also be used for analog input to the built-in 6 bit, 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280 μs. The necessary pin can be programmed to A/D analog input in 1 bit units, and P2-2 can be set to the reference voltage input. Internal power supply (V_{DD}) or constant voltage (V_{EE}) can be used as the reference voltage. In addition, constant voltage (V_{EE}) can be input to the A/D analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance. Pin P2-3 can also take over the output of the built-in 12 bit PWM. The PWM output is a continuous 73.26 Hz pulse, whose duty is converted in 256 steps (8 bit). In addition, a further 4 bit are output every 16 PWM pulse cycles (218.5 ms). The A/D converter, PWM output, and their control are all executed by program.	
46~49	P3-0/SI P3-1/SO P3 - 2/$\overline{SCK}$ P3-3/BUZR	I/O port 3 /Serial data input /Serial data output /Serial clock input-output /Buzzer output	4 bit I/O ports, whose input/output can be programmed in 1 bit units. Pins P3-0 through P3-2 also function as input/output pins for the serial interface circuit (SIO). The SIO serially inputs 4 bit or 8 bit data from the SI pin at the $\overline{SCK}$ pin's clock edge, and serially outputs data from the SO pin. For the serial operation clock ($\overline{SCK}$) there is an internal/external option, and a rising/falling shift option. Moreover, because the SO pin can be switched to serial input (SI), LSI control and communication between controllers is simple. All SIO input pins use built-in Schmitt circuits. The P3-3 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75 kHz and 147 Hz, and at a duty of 50%. The SIO, the buzzer output, and all associated controls can be programmed.	
50~61	P4-0~P6-3	I/O port 4~I/O port 6	The input and output of these 16 bit I/O ports can be programmed in 1bit units.	
62	MUTE	Muting output port	1 bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed; PPL phase difference can also be output using this pin.	
63	TEST	TEST mode control input	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (a pull-down resistor is built in).	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
64	IF_{IN}/IN1 /SC_{IN}	IF signal input/Input port /Frequency measuring input	IF counter's IF signal input pin for counting the IF signals of the FM and AM bands and detecting the automatic stop position. The input frequency is between 0.35 to 12 MHz (0.2 V_{p-p}-min). A built-in input amp and C coupling allow operation at low-level input. The IF counter is a 20 bit counter with optional gate times of 1, 4, 16, and 64 ms. 20 bits of data can be readily stored in memory. The IF counter can also be used as a timer when not being used as an IF counter. This input pin can be programmed for use as an input port (IN port). It can also be used to measure the frequency with the IF counter (SC_{IN}). CMOS input is used when the pin is set as an IN port. Note: When the pin is set for SCIN, use DC coupling and input a square wave.	
65 66	DO1/OT DO2	Phase comparison output /Output port Phase comparison output	PLL's phase comparison tri-state output pins. When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus, the pins can be used to improve lock-up time or used as output ports.	
67	$\overline{HOLD}$	HOLD mode control input	Input pin for request/release HOLD mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{HOLD}$ pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{HOLD}$ pin. Memory back-up is released when the $\overline{HOLD}$ pin goes high in MODE-0, or when the level of the $\overline{HOLD}$ pin level in MODE-1. When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{HOLD}$ pin input releases the mode. In memory back-up mode, current consumption is low (below 1 μA), and all the output pins (e.g., display output, output ports) are automatically set to low level.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
68	PSC	Prescaler control output	Output pin that controls the switching of two modulus prescaler ratios between 1/15 and 1/16. When the programmable counter is used in pulse swallow frequency division mode, this output pin controls the external prescaler ratio. High: 1/16, Low: 1/15	
72	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 1.8 to 3.6 V (3.0 V typ.) is applied. In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0 V. If voltage falls below 1.5 V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5 V, the CPU restarts. STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8 V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (power on reset) Note: To operate the power on reset, the power supply should start up in 10 to 100 ms.	
69	GND			
70	FM_{IN}	FM programmable counter input	Programmable counter input pin for the 16 bit pulse swallow frequency division method. This pin inputs the external prescaler output signals. A built-in input amp and C coupling allow operation at low-level input. Note: When in the PLL OFF mode or when set to AMIN input, the input is pulled down.	
71	AM_{IN}	AM local oscillator signal input	Programmable counter input pin when using the 12 bit direct dividing method. Normally, the pin inputs AM band local oscillation signals. Built-in input amp operates with low-level input using a C coupling. Note: When in PLL OFF mode or when set to FMIN input, the input is pulled down.	
73	$\overline{RESET}$	Reset input	Input pin for system reset signals. Reset takes place while at low level; at high level, the program starts from address "0". Normally, if more than 1.8 V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
74	X_{OUT}	Crystal oscillator pins	Crystal oscillator pins A reference 75 kHz crystal oscillator is connected to the X_{IN} and X_{OUT} pins. The oscillator stops oscillating during CKSTP instruction execution. The V_{XT} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.1 μF typ.) is connected.	
75	X_{IN}			
76	V_{XT}			
77	V_{LCD}	Voltage doubler boosting pin	Voltage doubler boosting pin for driving the LCD. A capacitor (0.1 to 3.3 μF typ.) is connected to boost the voltage. The V_{LCD} pin outputs voltage (3.0 V), which has been doubled from the constant voltage (V_{EE}: 1.5 V) using the capacitors connected between C_1 and C_2. That potential is supplied to the LCD drivers. If the internal V_{LCD} OFF bit is set to "1" by program, an external power supply can be input through the VLCD pin to drive the LCD. At this time, the $V_{LCD}/2$ potential, whose V_{LCD} voltage is divided using registers, is output from the C_2 pin.	
78	C_1			
79	C_2			
80	V_{EE}	Constant voltage supply pin	1.5 V constant voltage supply pin for driving the LCD. A stabilizing capacitor (0.47 μF typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.	—

Note 1: When the device is reset (voltage higher than 1.8 V, or when $\overline{\text{RESET}}$ = low → high) I/O ports are set to input, the pins for LCD output and I/O ports are set to LCD output, the pins for I/O ports and additional functions (e.g., SIO, A/D converter) are set to I/O port input pins, while the IF_{IN}/IN1/SC_{IN} pins become IF input pins.

Note 2: When in PLL OFF mode (when the four bits in the internal reference ports all show "1"), the IF_{IN}/SC_{IN} and FM_{IN}/AM_{IN} pins are pulled down, and DO1 and DO2 are at high impedance.

Note 3: When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports and the LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{XT}) are all off.

Note 4: When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

Note 5: If the pins for LCD output and I/O ports are set to I/O ports, because the V_{LCD} potential is used as the power supply for their input and output, attention must be paid to the input potential when the ports are set to input, and to the high-level output current when set to output.

Description of Operation

CPU

The CPU consists of: program counter, stack register, ALU, program memory, data memory, G-register, data register, carry F/F and judge circuit.

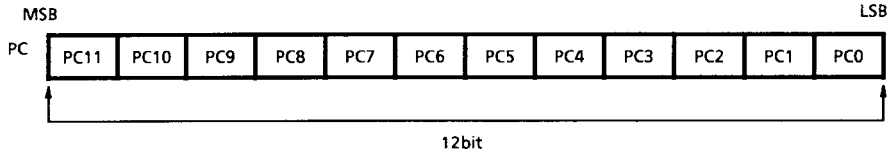
1. Program Counter (PC)

This counter consists of a 12 bit binary up-counter and is for addressing program memory (ROM). It is cleared by system reset and a program starts from address 0.

Normally, when one instruction is executed, it is incremented by one.

However, when JUMP or CAL instruction is executed, the address designated in the operand of the instruction will be loaded.

When an instruction having the skip function (AIS, SLTI, TMT, RNS instruction, etc.) is executed and, if the result is a condition to be skipped it is incremented by two and skips next instruction.



2. Stack Register (STACK)

It is a register consisting of 2 × 12 bits.

When subroutine call instruction is executed, a value of the contents of program counter + 1, that is, return address is stored in this register.

The contents of this register is loaded into program counter when return instruction (RN, RNS instruction) is executed.

This stack level is 2 levels and the nesting also is 2 levels.

3. ALU

It has the following functions: binary 4 bit parallel add-subtraction, logical operation, comparison, multiple bit judge.

The contents of data memory are directly treated in every operation because this CPU has no accumulator.

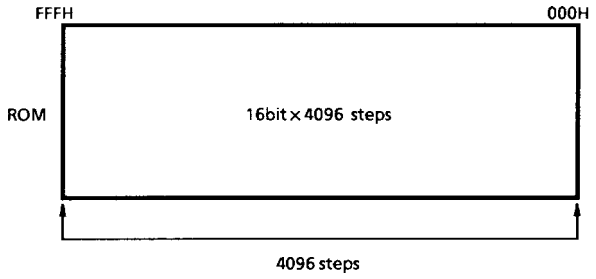
4. Program Memory (ROM)

It consists of 16 bits × 4096 steps and stores programs. The usable address range is 4096 steps from address 000H to FFFH.

There is no concept of page and field in program memory, JUMP and CAL instructions are freely usable in 4096 steps. Any address in program memory can be used as data area. When DAL instruction is executed, the contents of 16 bits are loaded into data register.

Note 6: Set the data area in program memory to an address outside the program loop.

Note 7: When DAL instruction is executed, the address of program memory designat able as data area is within 1024 steps from 000H to 3FFH.



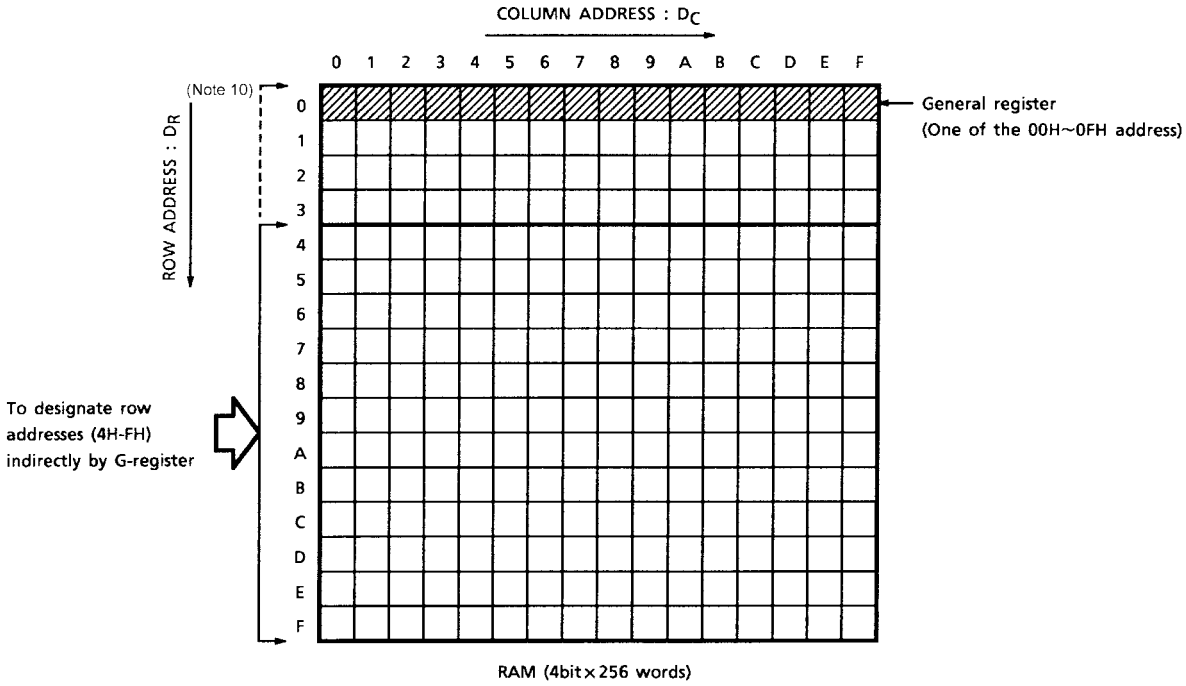
5. Data Memory (RAM)

It consists of 4 bit × 256 words and is used for data storage. These 256 words are expressed by the row address (4 bits) and column address (4 bits). 192-words in data memory (row address = 4H to FH address) are indirectly addressed by G-register. For this reason, when processing data within this area, it is necessary to process after the row address is designated by G-register in advance.

The address 00H to 0FH in data memory is called general register. This is also usable for designating only the column address (4 bits). These 16 general registers are used for operation and transfer with the data memory and are also usable as ordinary data memories.

Note 8: The column address (4 bits) designating general register become the register number of general register.

Note 9: It is possible to designate all row addresses (0H to FH address) indirectly by G-register.



Note 10: Designating row address = 0H-FH indirectly is possible.

6. G-Register (G-REG)

It is a 4 bit register for addressing row addresses (DR = 4H to FH address) of 192 words of data memory. The contents of this register are valid when MVGD/MVGS instruction is executed and have nothing to do when other instructions are executed. This register is used as one port and the contents are set when OUT1 instruction of I/O instructions is executed. (refer to register port, item 1.)

7. Data Register (DATA REG)

It is a register consisting of 1 × 16 bit. When DAL instruction is executed, the 16 bit data of any address between 000H to 3FFH in program memory is loaded. This register is treated as one of port and when IN1 instruction of I/O instructions is executed, it's contents are loaded into data memory by 4 bits unit. (refer to register port, item 2.)

8. Carry F/F (CF/F)

This is set if carry or borrow is generated as a result of execution of the calculation instruction and reset if neither is generated.

The contents of carry F/F changes only when addition/subtraction instruction is executed and remain unchanged when other instructions are executed.

9. Judge Circuit (J)

When an instruction with the skip function is executed, it judges the skip condition. When the skip condition is satisfied, the program counter is incremented by two and the subsequent instruction is skipped.

There are 29 instructions having the skip function. (refer to item 11, instruction function, table of operational instruction marked "*".)

10. Table of Instruction Set

Total 62 kinds of instruction sets are available, and instructions are all one word.
These instructions are expressed in a 6bit instruction code.

High Order 2 Bit / Low Order 4 Bit		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	TMTR r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	TMFR r, M	SGEI M, I
0010	2	AIN M, I	ADN r, M	SEQ r, M	SEQI M, I
0011	3	AIC M, I	AC r, M	SNE r, M	SNEI M, I
0100	4	AICS M, I	ACS r, M	LD r, M	TMTN M, N
0101	5	AICN M, I	ACN r, M	ST M, r	TMT M, N
0110	6	ORIM M, I	ORR r, M	MVGD r, M	TMFN M, N
0111	7	ANIM M, I	ANDR r, M	MVGS M, r	TMF M, N
1000	8	SI M, I	SU r, M	CALL $ADDR_1$	IN1 M, C
1001	9	SIS M, I	SUS r, M		IN2 M, C
1010	A	SIN M, I	SUN r, M		IN3 M, C
1011	B	SIB M, I	SB r, M		OUT1 C, M
1100	C	SIBS M, I	SBS r, M	JUMP $ADDR_1$	OUT2 C, M
1101	D	SIBN M, I	SBN r, M		OUT3 C, M
1110	E	XORI M, I	XORR r, M		DAL $ADDR_2$, r
1111	F	MVIM M, I	MVSR M_1, M_2		RN, RNS, WAIT CKSTP, NOOP

11. Table of Functions and Operation of Instruction

(explanation of symbols in the table)

M: Data memory address
Generally one of data memory addresses 00H to 3FH
r: General register
One of data memory addresses 00H to 0FH
PC: Program counter (12 bit)
STACK: Stack register (12 bit)
G: G-register (4 bit)
DATA: Data register (16 bit)
I: Immediate data (4 bit)
N: Bit position (4 bit)
—: ALL "0"
C: Port code No. (4 bit)
C_N: Port code No. (4 bit)
R_N: General register No. (4 bit)
$ADDR_1$: Program memory address (12 bit)
$ADDR_2$: High order 6 bit of program memory address in page 0
Ca: Carry
b: Borrow
IN1 to IN3: Port treated by execution of IN1 to IN3 instruction
OUT1 to OUT3: Port treated by execution of OUT1 to OUT3 instruction
( ): Contents of register or data memory
[ ] $_C$: Contents of port indicated by Code No. C
[ ]: Contents of data memory shown by the contents of register or data memory
[ ] $_P$: Contents of program memory (16 bit)
IC: Instruction code (6 bit)
*: Instruction with skip function
D_C: Data memory column address (4 bit)
D_R: Data memory row address (2 bit)

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC 6 bit	A 2 bit	B 4 bit	C 4 bit
Addition instruction	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	D_R	D_C	I
	AIS	M, I	*	Add immediate data to memory, then skip if carry	M ← (M) + I Skip if carry	000001	D_R	D_C	I
	AIN	M, I	*	Add immediate data to memory, then skip if not carry	M ← (M) + I Skip if not carry	000010	D_R	D_C	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000011	D_R	D_C	I
	AICS	M, I	*	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + ca Skip if carry	000100	D_R	D_C	I
	AICN	M, I	*	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + ca Skip if not carry	000101	D_R	D_C	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	010000	D_R	D_C	R_N
	ADS	r, M	*	Add memory to general register, then skip if carry	r ← (r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN	r, M	*	Add memory to general register, then skip if not carry	r ← (r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	010011	D_R	D_C	R_N
	ACS	r, M	*	Add memory to general register with carry, then skip if carry	r ← (r) + (M) + ca Skip if carry	010100	D_R	D_C	R_N
	ACN	r, M	*	Add memory to general register with carry, then skip if not carry	r ← (r) + (M) + ca Skip if not carry	010101	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC 6 bit	A 2 bit	B 4 bit	C 4 bit
Subtraction instruction	SI	M, I		Subtract immediate data from memory	M ← (M) – I	001000	D_R	D_C	I
	SIS	M, I	*	Subtract immediate data from memory, then skip if borrow	M ← (M) – I Skip if borrow	001001	D_R	DC	I
	SIN	M, I	*	Subtract immediate data from memory, then skip if not borrow	M ← (M) – I Skip if not borrow	001010	D_R	D_C	I
	SIB	M, I		Subtract immediate data from memory with borrow	M ← (M) – I – b	001011	D_R	D_C	I
	SIBS	M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN	M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU	r, M		Subtract memory from general register	r ← (r) – (M)	011000	D_R	D_C	R_N
	SUS	r, M	*	Subtract memory from general register, then skip if borrow	r ← (r) – (M) Skip if borrow	011001	D_R	D_C	R_N
	SUN	r, M	*	Subtract memory from general register, then skip if not borrow	r ← (r) – (M) Skip if not borrow	011010	D_R	D_C	R_N
	SB	r, M		Subtract memory from general register with borrow	r ← (r) – (M) – b	011011	D_R	D_C	R_N
	SBS	r, M	*	Subtract memory from general register with borrow, then skip if borrow	r ← (r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN	r, M	*	Subtract memory from general register with borrow, then skip if not borrow	r ← (r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N
Comparison instruction	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	100010	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
						IC 6 bit	A 2 bit	B 4 bit	C 4 bit
Transfer instruction	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) $\neq$ (M)	100011	D_R	D_C	R_N
	LD	r, M		Load memory to general register	r $\leftarrow$ (M)	100100	D_R	D_C	R_N
	ST	M, r		Store general register to memory	M $\leftarrow$ (r)	100101	D_R	D_C	R_N
	MVSR	M_1, M_2		Move memory to memory in the same row	(D_R, D_{C1}) $\leftarrow$ (D_R, D_{C2})	011111	D_R	D_{C1}	D_{C2}
	MVIM	M, I		Move immediate data to memory	M $\leftarrow$ I	001111	D_R	D_C	I
	MVGD	r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] $\leftarrow$ (M)	100110	D_R	D_C	R_N
	MVGS	M, r		Move source memory referring to G-register and general register to memory	M $\leftarrow$ [(G), (r)]	100111	D_R	D_C	R_N
Input and output instruction	IN1	M, C		Input IN1 port data to memory	M $\leftarrow$ [IN1] $_C$	111000	D_R	D_C	C_N
	OUT1	C, M		Output contents of memory to OUT1 port	[OUT1] $_C$ $\leftarrow$ (M)	111011	D_R	D_C	C_N
	IN2	M, C		Input IN2 port data to memory	M $\leftarrow$ [IN2] $_C$	111001	D_R	D_C	C_N
	OUT2	C, M		Output contents of memory to OUT2 port	[OUT2] $_C$ $\leftarrow$ (M)	111100	D_R	D_C	C_N
	IN3	M, C		Input IN3 port data to memory	M $\leftarrow$ [IN3] $_C$	111010	D_R	D_C	C_N
	OUT3	C, M		Output contents of memory to OUT3 port	[OUT3] $_C$ $\leftarrow$ (M)	111101	D_R	D_C	C_N
Logical operation instruction	ORR	r, M		Logical OR of general register and memory	r $\leftarrow$ (r) $\vee$ (M)	010110	D_R	D_C	R_N
	ANDR	r, M		Logical AND of general register and memory	r $\leftarrow$ (r) $\wedge$ (M)	010111	D_R	D_C	R_N
	ORIM	M, I		Logical OR of memory and immediate data	M $\leftarrow$ (M) $\vee$ I	000110	D_R	D_C	I
	ANIM	M, I		Logical AND of memory and immediate data	M $\leftarrow$ (M) $\wedge$ I	000111	D_R	D_C	I
	XORIM	M, I		Logical exclusive OR of memory and immediate data	M $\leftarrow$ (M) $\oplus$ I	001110	D_R	D_C	I
	XORR	r, M		Logical exclusive OR of general register and memory	r $\leftarrow$ (r) $\oplus$ (M)	011110	D_R	D_C	R_N

Inst. Gr.	Mnemonic	Skip Function	Explanation of Function	Explanation of Operation	Machine Language (16 bit)			
					IC 6 bit	A 2 bit	B 4 bit	C 4 bit
Bit judge instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	100000	D_R	D_C	R_N
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	100001	D_R	D_C	R_N
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	D_R	D_C	N
	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	110111	D_R	D_C	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	110100	D_R	D_C	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N)= not all "0"	110110	D_R	D_C	N
Subroutine instruction	CALL $ADDR_1$		Call subroutine	STACK ← (PC) + 1 and PC ← $ADDR_1$	1010	$ADDR_1$ (12 bit)		
	RN		Return to main routine	PC ← (STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	01	—	—
Jump instruction	JUMP $ADDR_1$		Jump to the address specified	PC ← $ADDR_1$	1011	$ADDR_1$ (12 bit)		
Other instruction	DAL $ADDR_2$, r		Load program memory in page 0 to DATA register	DATA ← $[ADDR_2 + (r)]_P$ in page 0	111110	$ADDR_2$ (6 bit)		R_N
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode) At P = "1" H, except for clock generator all function is waiting (hard wait mode)	Wait at condition P	111111	10	0000	P
	CKSTP		Clock generator stop	Stop clock generator in $\overline{HOLD}$ = "0"	111111	10	1000	—
	NOOP		No operation	—	111111	11	—	—

Note 11: Low order 4 bits out of the program memory address 10 bits designated by DAL instruction are to be indirectly address according to contents of the general register.

DAL instruction execution time is 80 μs (2 machine cycles).

Note 12: MVGS instruction execution time is 80 μs (2 machine cycles).

I/O Map

All ports within the device are expressed by a matrix of 6 I/O instructions (OUT1 to 3 instruction, IN1 to 3 instruction) and a 4 bit code number.

The allocation of these ports is described as I/O map in the following page. In this I/O map, port names treated in execution of I/O instructions are assigned on the axis of ordinates and port code numbers on the axis of abscissas. The G-register and data register are treated also as ports.

The OUT1 to 3 instruction and IN1 to 3 instruction are designated at an output port and input port, respectively.

Note 13: The oblique lined ports shown on the I/O map are actually not existed in the device.

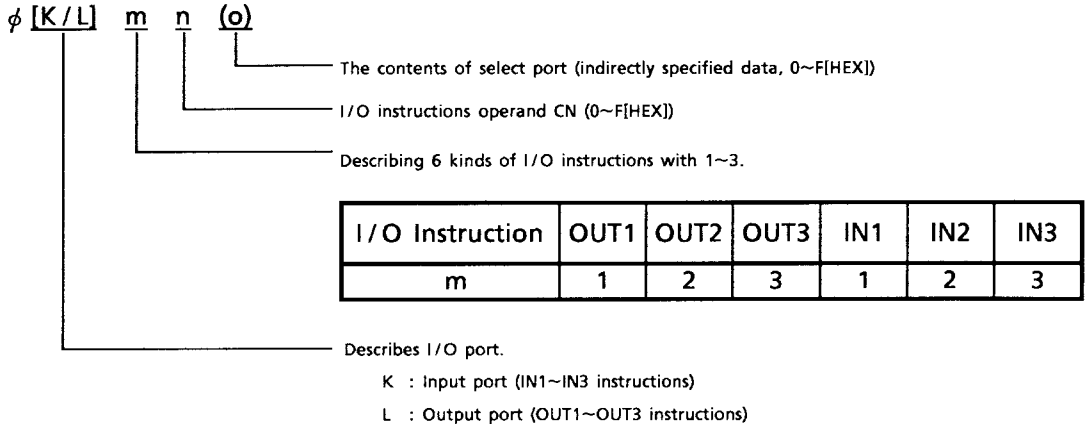
If data are outputted to a non-existing output port when an output instruction is executed, other ports or the contents of data memory are not especially affected.

If a non-existing input port is specified when an input instruction is executed, the contents loaded to data memory is all "1".

Note 14: Ports with *mark out of output ports on the I/O map are unused ports. Data outputted to these ports will become "don't care".

Note 15: The contents of the ports expressed by 4 bits, Y1 corresponds to LSB of data of the data memory and Y8 correspond to MSB.

Ports that are designated by 6 I/O instructions and No. C are expressed in coding as follows.



I/O Instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

(example) The G-register setting is allotted in the code "F" of OUT1 instruction. At this time the encoded expression is "φL1F".

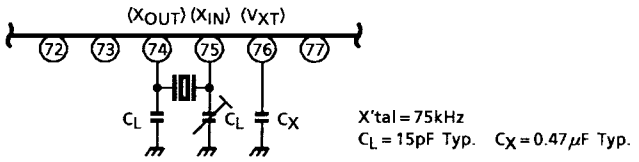
I/O Map

I/O / Code	φL1				φL2				φL3				φK1				φK2				φK3			
	OUT1 Instruction				OUT2 Instruction				OUT3 Instruction				IN1 Instruction				IN2 Instruction				IN3 Instruction			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	*	IF offset		FM	A/D control				I/O-1 data				IF control data			1	A/D data				I/O-1 data			
		+1	−1		AD SEL0	AD SEL1	REF SEL0	REF SEL1	−0	−1	−2	−3	BUSY	Manual	OVER		AD0	AD1	AD2	AD3	−0	−1	−2	−3
1	Programmable counter select		*		A/D control				I/O-2 data				IF data				A/D data			1	I/O-2 data			
	#1	#2			STA	DCREF ON	AD1 ON	AD2 ON	−0	−1	−2	−3	f0	f1	f2	f3	AD4	AD5	BUSY		−0	−1	−2	−3
2	Programmable counter				SIO control				I/O-3 data				IF data								I/O-3 data			
	PA	PB	PC	PD	edge	$\overline{SCK}$ - INV	$\overline{SCK}$ - I/$\overline{O}$	SIO ON	−0	−1	−2	−3	f4	f5	f6	f7					−0	−1	−2	−3
3	Reference port				SIO control			*	I/O-4 data				IF data				SIO contorl data			1	I/O-4 data			
	R0	R1	R2	R3	STA	SO - I/$\overline{O}$	4/$\overline{8}$ bit		−0	−1	−2	−3	f8	f9	f10	f11	BUSY	COUNT	SIO F/F		−0	−1	−2	−3
4	IF counter control				SIO output data				I/O-5 data				IF data				SIO input data				I/O-5 data			
	*	SC_{ON}	IF/$\overline{IN1}$	*	S0	S1	S2	S3	−0	−1	−2	−3	f12	f13	f14	f15	S0	S1	S2	S3	−0	−1	−2	−3
5	IF counter control				SIO output data				I/O-6 data				IF data				SI input data				I/O-6 data			
	STA/$\overline{STP}$	Manual	G0	G1	S4	S5	S6	S7	−0	−1	−2	−3	f16	f17	f18	f19	S4	S5	S6	S7	−0	−1	−2	−3
6	MUTE OUT				Timer reset		TEST data		I/O-7 data								Timer			STOP F/F	I/O-7 data			
	MUTE	I/O	POL	UNLOCK	2 Hz F/F	Timer	#4	#5	−0	−1	−2	−3					2 Hz F/F	10 Hz	100 Hz		−0	−1	−2	−3
7	UNLOCK RESET	DO1 control			Key scan start				I/O-8 data				UNLOCK		IN1	1	Key scan digit				I/O-8 data			
		OTC	OT	Hz	KS1	KS2	KS4	KS8	−0	−1	−2	−3	F/F	ENABLE			KR_1	KR_2	KR_4	KR_8	−0	−1	−2	−3
8	PWM/BUZR data				Key scan end				I/O-9 data				UNLOCK data			1	Key input data				I/O-9 data			
	PW_0/B0	PW_1/B1	PW_2/B2	PW_3/B3	KE1	KE2	KE4	KE8	−0	−1	−2	−3	UN1	UN2	UN3		K0	K1	K2	K3	−0	−1	−2	−3
9	PWM/BUZR data				Key scan control				I/O-10 data								Key scan data				I/O-10 data			
	PW_4/B4	PW_5/B5	PW_6/B6	PW_7/B7	KC0	KC1	KC2	KC3	−0	−1	−2	−3					K0	K1	K2	K3	−0	−1	−2	−3
A	PWM data				Key scan data select				I/O-11 data												I/O-11 data			
	PW_8	PW_9	PW_{10}	PW_{11}	KSD1	KSD2	KSD4	KSD8	−0	−1	−2	−3									−0	−1	−2	−3
B	PWM ON	BUZR ON	PWM/ BUZR	Buffer transfer					I/O-12 data				$\overline{HOLD}$	1	1	1					I/O-12 data			
									−0	−1	−2	−3									−0	−1	−2	−3
C	TEST data								I/O-13 data				DATA-reg								I/O-13 data			
	#0	#1	#2	#3					−0	−1	−2	−3	d0	d1	d2	d3					−0	−1	−2	−3
D					SEG data select				I/O-14 data				DATA-reg								I/O-14 data			
					S1	S2	S4	S8	−0	−1	−2	−3	d4	d5	d6	d7					−0	−1	−2	−3
E				CKSTP MODE	SEG-1 data				I/O control select				DATA-reg								IN3	1	1	1
					COM1	COM2	COM3	SEG	I/O1	I/O2	I/O4	I/O8	d8	d9	d10	d11								
F	G-reg				SEG-2 data				I/O control data				DATA-reg											
	#0	#1	#2	#3	COM1	COM2	COM3	SEG	IO-0	IO-1	IO-2	IO-3	d12	d13	d14	d15								

Connection of Crystal Resonator

Connect a 75 kHz crystal resonator to crystal oscillator terminal of the device (XIN, XOUT) as shown below.

This oscillation signal is supplied to clock pulse generator, reference frequency divider and generates various CPU timing signals and reference frequency signals. The crystal circuit uses voltage (VXT = 1.3 V typ.) supplied from a built-in regular voltage circuit as power supply. Because of this, it can stabilizes the crystal resonator and reduces the consumption current.



Note 16: Use a crystal oscillator of good starting characteristic such as low CI value.

System Reset

When "L" level signal is input to the $\overline{\text{RESET}}$ terminal or more than 0 to 1.8 V is supplied to the V_{DD} terminal (power on reset), system reset is applied to a device. After standby period of 100 ms has passed after system reset, a program will start from address 0.

Since it normally uses POWER ON RESET function, fix $\overline{\text{RESET}}$ terminal at "H" level.

Note 17: During system reset and the subsequent stand-by period, LCD common and segment outputs are fixed at "L" level.

Note 18: The internal ports shown in the following table are fixed after system reset, but the other ports are not fixed. Accordingly it is necessary to initialize them by program.

Fixed Internal Ports

Port Fixed to "0"	Port Fixed to "1"
SC_{ON} bit (ϕL14), Manual bit (ϕL15)	Reference port (ϕL13)
IO, POL, UNLOCK bit (ϕL16)	MUTE bit (ϕL16)
DO1 control port (ϕL17)	IF/$\overline{\text{IN1}}$ (ϕL14)
PWM_{ON}, $BUZR_{ON}$, PWM/BUZR, Transfer bit (ϕL1B)	
Test port (ϕL1C, ϕL26)	
CKSTP MODE bit (ϕL1E)	
AD control port (ϕL20, ϕL21)	
SIO control port (ϕL22, ϕL23)	
Timer port (ϕK26)	
Key scan start, control port (ϕL27, ϕL290 to ϕL295)	Key scan end port (ϕL28)
V_{LCD} OFF bit (ϕL2FF)	
IO-1 to IO-6 IO control port (ϕL3F0 to ϕL3F5)	DISP OFF bit (ϕL2FF)
	SEG bit (LCD/IO switching bit; ϕL2E0 to ϕL2EF, ϕL2F0 to ϕL2FE)

Backup Mode

When CKSTP or WAIT instruction is executed, the following three kinds of backup modes are selected.

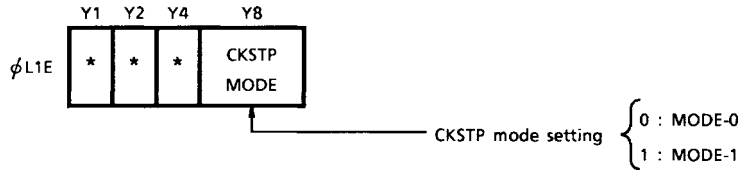
1. Clock Stop Mode

It is a function to stop operating system and holds the operation state of device just before stop with low current consumption (below 1 μA at V_{DD} = 3.0 V). At this time the crystal oscillation stops and the LCD display driver terminal and output ports are all fixed at "L" level or OFF state automatically. The supply voltage can be reduced to 1.0 V in this clock stop mode.

Program stops at the address of executing CKSTP instruction when CKSTP instruction is executed. If clock stop mode is released, the next address is executed after lapse of stand-by time of 100 ms.

(1) Clock stop mode setting

The clock stop mode setting has two kinds of mode. The setting is selected by CKSTP MODE bit. This bit is accessed when OUT1 instruction designated [C_N = EH] in the operand is executed.



1) MODE-0

In this mode, CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "L" level, it becomes clock stop mode. If CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "H" level, it does the same operation as that of NOOP instruction.

2) MODE-1

In this mode, CKSTP instruction is executed regardless of the level of $\overline{\text{HOLD}}$ terminal, it becomes clock stop mode.

Note 19: The PLL will be off state while CKSTP instruction is executed.

(2) Released condition of clock stop mode

1) MODE-0

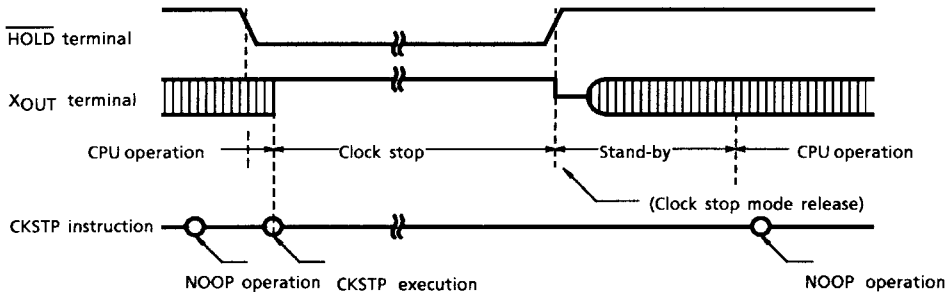
When clock stop mode is set by this mode, the clock stop mode is released when $\overline{\text{HOLD}}$ terminal is "H" level or changing the input condition of I/O port (P1-0 to 3) set at input port.

2) MODE-1

When clock stop mode is set by this mode, the clock stop mode is released by $\overline{\text{HOLD}}$ terminal or changing the input condition of I/O port (P1-0 to 3) set at input port.

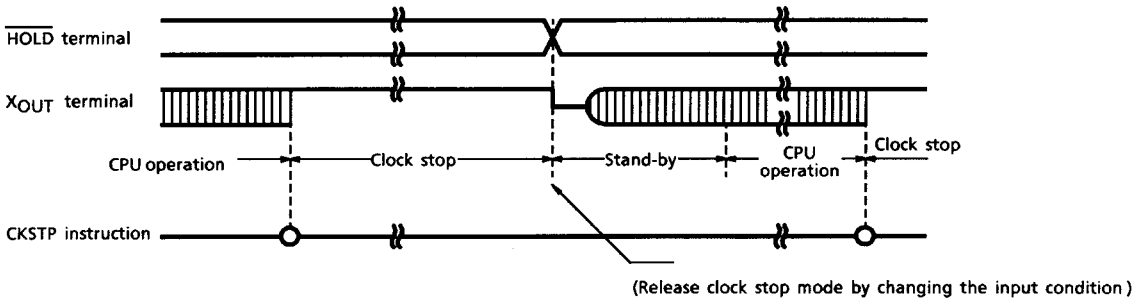
(3) Clock stop mode timing

1) MODE-0



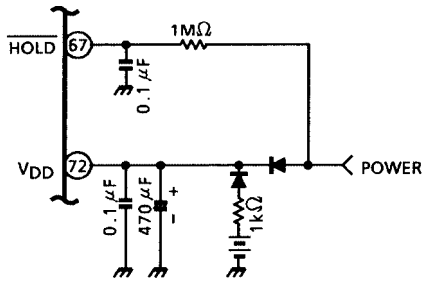
It sets to clock stop mode when CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "L" level.

2) MODE-1

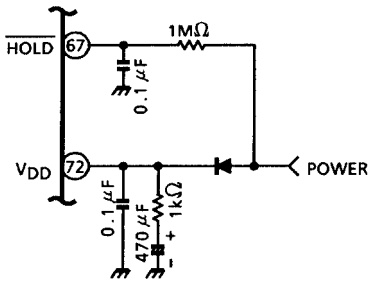


(it sets to clock stop mode whenever CKSTP instruction is executed.)

(4) Example of circuit (example of MODE-0 circuit)



Example of Backup Circuit Using Battery



Example of Backup Circuit Using Capacitor

2. Wait Mode

This mode stops system and holds the operation state of a device just before stop and therefore reduces current consumption. In this mode there are two kinds as follows:

- HARD WAIT mode
- SOFT WAIT mode

Program stops at the address of executing WAIT instruction when WAIT instruction is executed. If WAIT mode is released, the next address will be executed without stand-by time.

(1) SOFT WAIT mode

It stops only CPU operation internal a device when WAIT instruction is executed at designated operand port [P = 0H]. At this time others such as crystal oscillator and display circuit, etc. operate properly. SOFT WAIT mode is efficient in reducing current consumption for use in the program of clock function at clock operation.

Note 20: Current consumption differs depending on the program.

(2) HARD WAIT mode

It stops all operations except crystal oscillation circuit when WAIT instruction is executed at designated operand port [p = 1H]. For this reason, this mode can reduce further current consumption than SOFT WAIT mode. At this time, CPU and display circuit stop operation and LCD display output terminals are all fixed at "L" level automatically.

(10 μA typ. at V_{DD} = 3 V)

(3) WAIT mode setting

It will be in waiting condition whenever WAIT instruction is executed.

Note 21: It will be PLL off condition during HARD WAIT mode but not during SOFT WAIT mode. Therefore, it is necessary to set PLL off condition by program before SOFT WAIT mode is executed.

(4) Released condition of WAIT mode

The WAIT mode is released under one of following conditions;

1) When the input level of $\overline{\text{HOLD}}$ terminal changes,
2) When "H" level is inputted to key input terminal (K0 to K3) (only when key input mode)
3) When 2 Hz timer F/F is set to "1", (only SOFT WAIT mode)
4) When input level of I/O port (P1-0 to 3) set in input port is changed,

3. $\overline{\text{HOLD}}$ Input Port

	Y1	Y2	Y4	Y8
φK1B	$\overline{\text{HOLD}}$	1	1	1

The $\overline{\text{HOLD}}$ terminal is used as an input port. Data is read in the data memory when IN1 instruction designated [C_N = BH] in the operand.

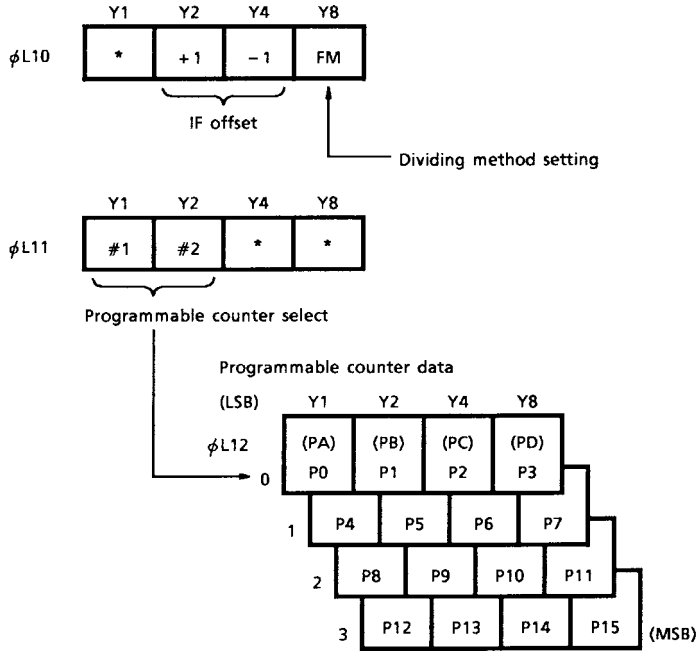
When this clock stop mode is set, it is necessary to access to this port before CKSTP instruction is executed. It may not be clock stop mode when CKSTP instruction is executed without accessing to this port.

Programmable Counter

It consists of external 2-modulus prescaler, 4 bit + 12 bit programmable counter and port to control these. Programmable counter controls ON/OFF according to the contents of reference port.

1. Programmable Counter Control Port

It is a port to control frequency division number, frequency division system and IF correction (IF offset) at FM band.



Note 22: Whenever accessing to ϕL12, the ϕL11 data is +1 incremented.

The frequency division system and IF offset are accesse by OUT1 instruction designated [C_N = 0H] in the operand.

The frequency division number setting is accessed by OUT1 instruction designated [C_N = 1H, 2H] in the operand and write to PA to PD bit (ϕL12).

This port is divided by the programmable counter select port (ϕL11) and the programmable counter data corresponding to the select port is set by setting data to them.

After the programmable data select is set to "3", set the programmable counter data (P12 to P15) and all of P0 to P15 data are updated. Because of this, make sure to access to P12 to P15 port and set the P12 to P15 port data at last even if changing only partially.

The programmable counter select is +1 incremented whenever accessing to the programmable counter data (ϕL12). Normally the setting can easily be done by setting "0" to the programmable counter select port and accessing to the programmable counter data successively.

2. Setting of Frequency Division System

The pulse swallow system or the direct frequency division system are selected according to FM port.

At AM band mode, the direct frequency division system is selected. When SW band, FM band or VHF/TV band mode, it selects the pulse swallow system which combines with external 2-modulas prescalers of TD6134AF, TD7101F and TD7103F.

FM	Frequency Division System	Example of Receiving Band	Operation Frequency Range	Input Terminal	Frequency Division Number (Note 24)	Prescaler
0	Direct frequency division system	MW/LW	0.5 to 12 MHz	AM_{IN}	n	None
1	(1/15 or 1/16) Pulse swallow system	SW	(Note 23) 1.5 to 35 MHz	FM_{IN}	n	TD7101F
	1/4 × (1/15 or 1/16) Pulse swallow system	FM	(Note 23) 50 to 150 MHz		4·n	TD6134AF TD7101F TD7103F
	1/8 × (1/15 or 1/16) Pulse swallow system	VHF/TV	(Note 23) 50 to 250 MHz		8·n	TD6134AF TD7103F

Note 23: It indicates the input frequency range for each prescaler of TD6134F, TD7101F and TD7103F.

Note 24: The “n” denotes a programmed divided frequency value.

3. IF Correction Function at FM Band

In the pulse swallow system, the actual frequency division number can be ±1 variable without changing programmable frequency division value by ΔIF + 1 port and ΔIF – 1 port.

This is used for IF offset condition at FM band.

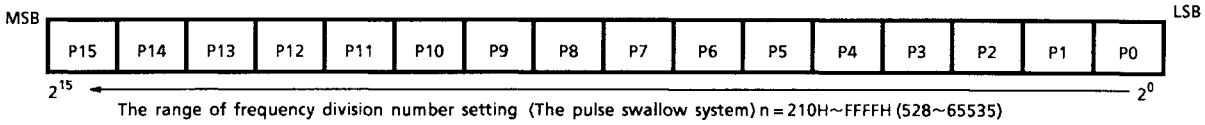
At the direct division system, the IF offset function does not operate.

ΔIF + 1	ΔIF – 1	Frequency Division Number (VHF)	Frequency Division Number (FM or HF)
0	0	2·n	n
0	1	2·(n – 1)	n – 1
1	0	2·(n + 1)	n + 1
1	1	Inhibit	Inhibit

4. Setting of Frequency Division Number

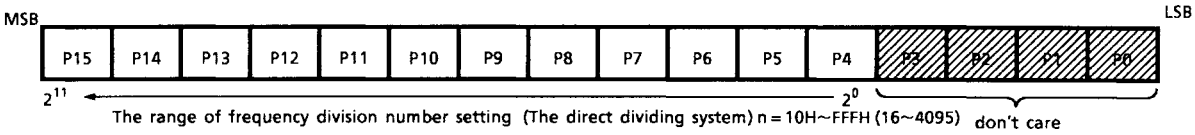
Set frequency division number of the program counter in binary number to P0 to P15 bit.

- The pulse swallow system (16 bits)



The range of frequency division number setting (The pulse swallow system) n = 210H~FFFFH (528~65535)

- The direct frequency division system (12 bits)



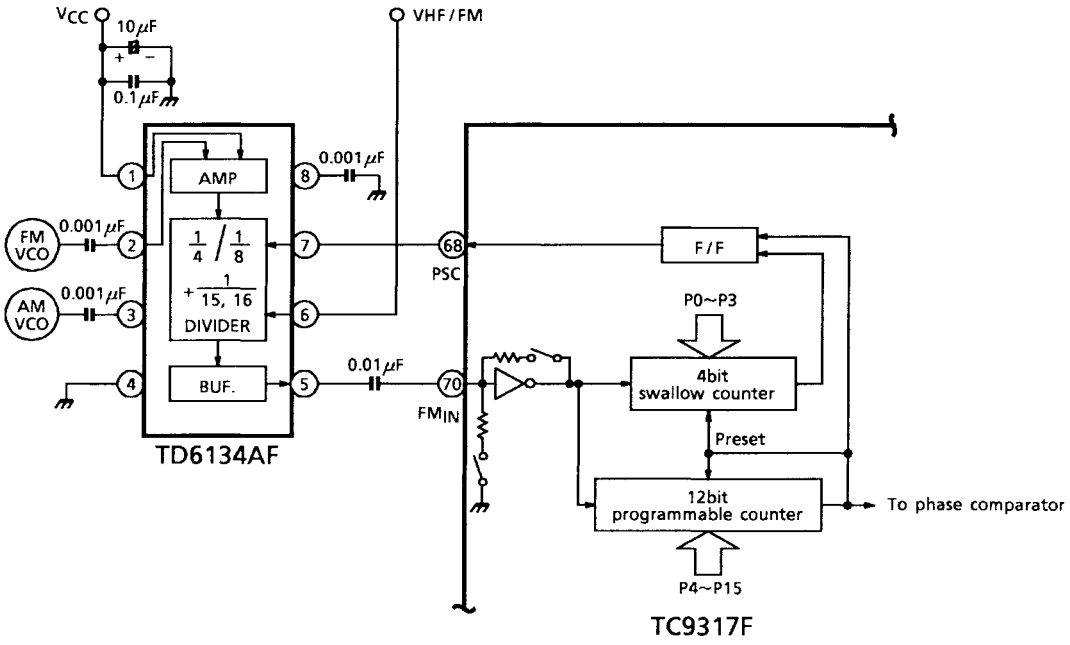
Note 25: Since offset is not provided to the program counter, a programmed division number will become an actual division number. However when a prescaler is used, the actual dividing value will become 4 times of the programmed value in case of FM band mode and 8 times at VHS/TV band mode.

Note 26: In the direct frequency division system, the P0 to P3 ports data (ϕL11) become unconcerned and P4 port are used as LSB.

5. Programmable Counter Circuit Configuration

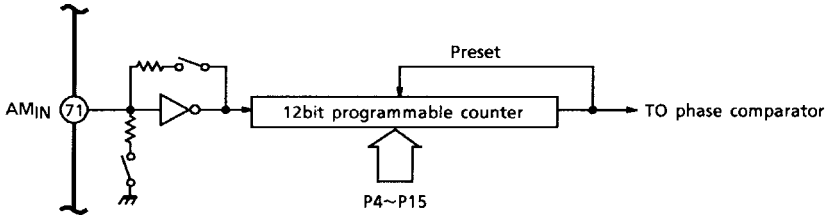
- Circuit configuration of the pulse swallow system

The circuit consists of: 2-modulus prescaler (TD6134AF, TD7101F, TD7103F), 4 bit swallow counter and 12 bit binary counter. At FM band, 1/4 divider is added to the front stage of the prescaler and 1/8 divider is added at VHF/TV band. The diagram with prescaler (TD6134AF) as shown below.



- Circuit configuration of direct frequency division system

In this case, the external prescaler is unnecessary and a 12 bit programmable counter is used.



Note 27: Both FM_{IN} and AM_{IN} terminals have built-in an amplifier respectively, and are operable at small amplitude with coupled capacitors. When the input terminal not selected according to the frequency division system and PLL off mode (setting be reference port) the input is pull-down.

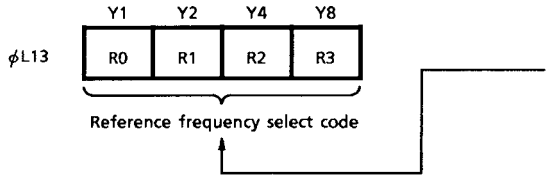
Reference Frequency Divider

This frequency divider generates 7 kinds of PLL reference frequency signals 1, 3, 3.125, 5, 6.25, 12.5 and 25 kHz by dividing external 75 kHz crystal oscillation signal.

This frequency selection is executed by the contents of reference port. The selected signal is used as reference frequency of the phase comparator as described below. According to the contents of the reference port, PLL ON/OFF is performed.

1. Reference Port

It is an internal port to select the 7 kinds of reference frequency signals. This port is accessed when OUT1 instruction designated [C_N = 3H] in the operand (ϕL13) is executed. When the contents of reference port are all "1", the programmable counter, IF counter and reference counter will stop and be in PLL off mode.



R3	R2	R1	R0	/	REFERENCE FREQUENCY
0	0	0	0	0	1kHz
0	0	0	1	1	3kHz
0	0	1	0	2	3.125kHz
0	0	1	1	3	5kHz
0	1	0	0	4	6.25kHz
0	1	0	1	5	12.5kHz
0	1	1	0	6	25kHz
0	1	1	1	7	Inhibit
⌇	⌇	⌇	⌇	⌇	⌇
1	1	1	0	E	Inhibit
1	1	1	1	F	PLL off mode

Phase Comparator&Lock Detection Port

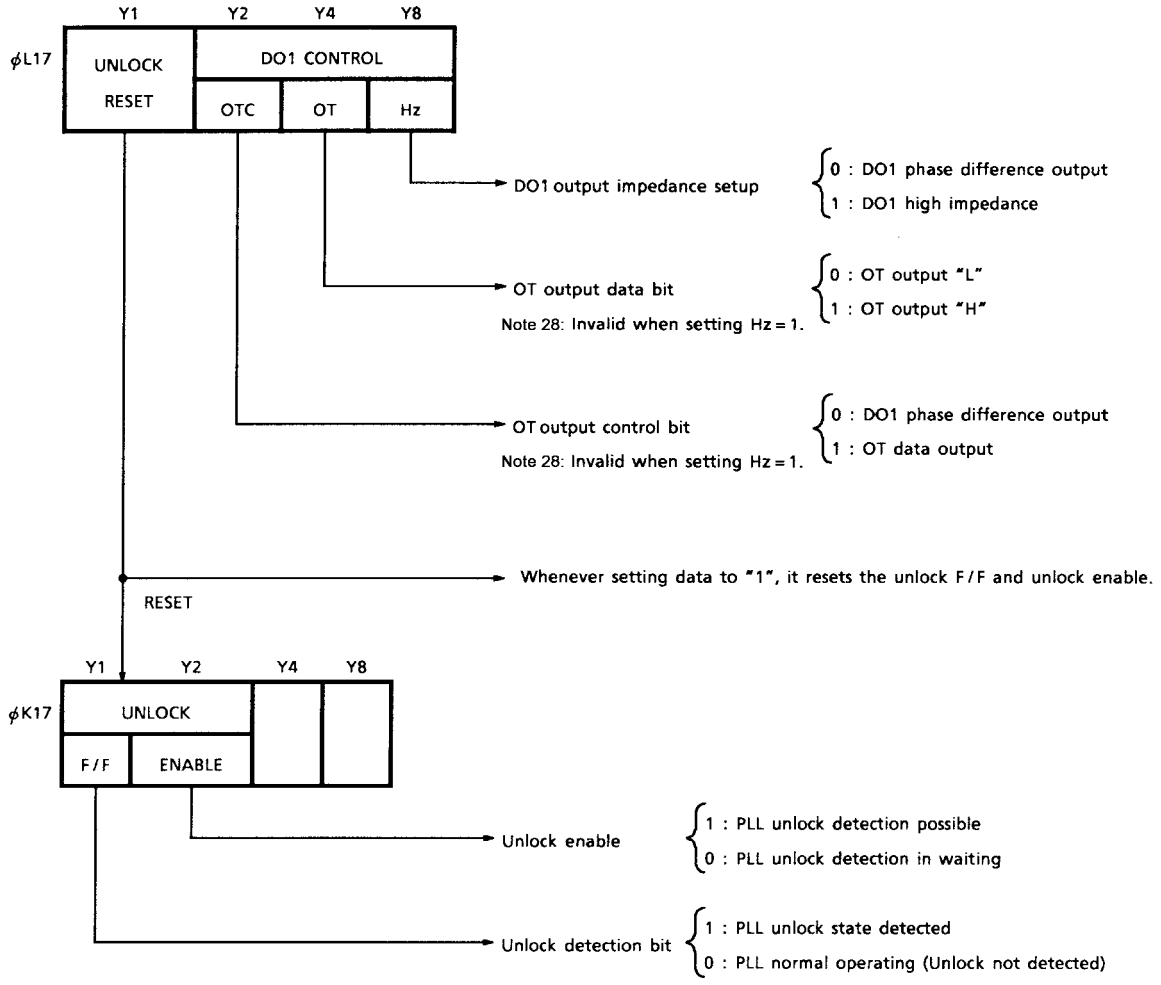
The phase comparator compares the phase between reference frequency signal supplied from reference frequency divider and programmable counter dividing output to output the difference. It controls VCO through a low pass filter so that the frequency and phase difference of these two signals can be equivalent.

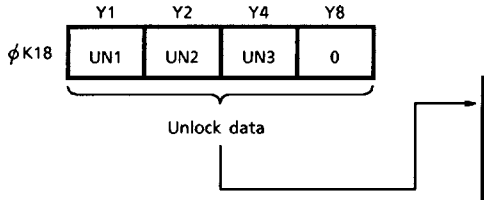
Because two tri-state buffers DO1 and DO2 terminals are outputted from the phase comparator, the filter constant can be optimally designed for each FM/VHF band and AM band.

The DO1 terminal is usable as general output terminal by means of DO1 control port. This terminal is capable of setting to high impedance. By using two terminals of DO1&DO2, it is possible to improve the characteristics of PLL loop lock-up type, etc.

The lock detection port is capable of detecting the lock state of PLL circuit.

1. DO1 Control Port and Unlock Detection Port





UN3	UN2	UN1		PHASE DIFFERENCE
0	0	0	0	0μs~ + 6.66μs
0	0	1	1	– 13.3μs~0μs, + 6.66μs~ + 20μs
0	1	0	2	– 13.3μs~ – 26.6μs, + 20μs~ + 33.3μs
0	1	1	3	– 26.6μs~ – 40μs, + 33.3μs~ + 46.6μs
1	0	0	4	– 40μs~ – 53.3μs, + 46.6μs~ + 60μs
1	0	1	5	– 53.3μs~ – 66.6μs, + 60μs~ + 73.3μs
1	1	0	6	– 66.6μs~ – 80μs, + 73.3μs~ + 86.6μs
1	1	1	7	under – 80μs, Over + 86.6μs

Each OTC, OT and Hz bit of DO1 control port is a control bit as below condition.

- DO1 output terminal is used as general output port.
- DO1 output terminal is set to high-inspendance state without outputting DO1 output phase difference.

These are set by program according to the specification.

The UNLOCK F/F bit detects the phase difference between the programmable counter divider output and the reference frequency when the phase is about 180° shift. If the phase difference does not accord at this time, that is, if in unlock state, UNLOCK F/F will be set.

UNLOCK F/F will be reset whenever setting "1" to UNLOCK RESET bit.

DO output detects the phase difference at the cycle of reference frequency. It's necessary to access the UNLOCK F/F that its has more time than a cycle of reference frequency after resetting the UNLOCK F/F. Because ENABLE bit is prepared. After confirm that UNLOCK enable bit sets to "1", UNLOCK F/F is accessed.

UNLOCK enable bit is reset whenever setting "1" to UNLOCK RESET bit.

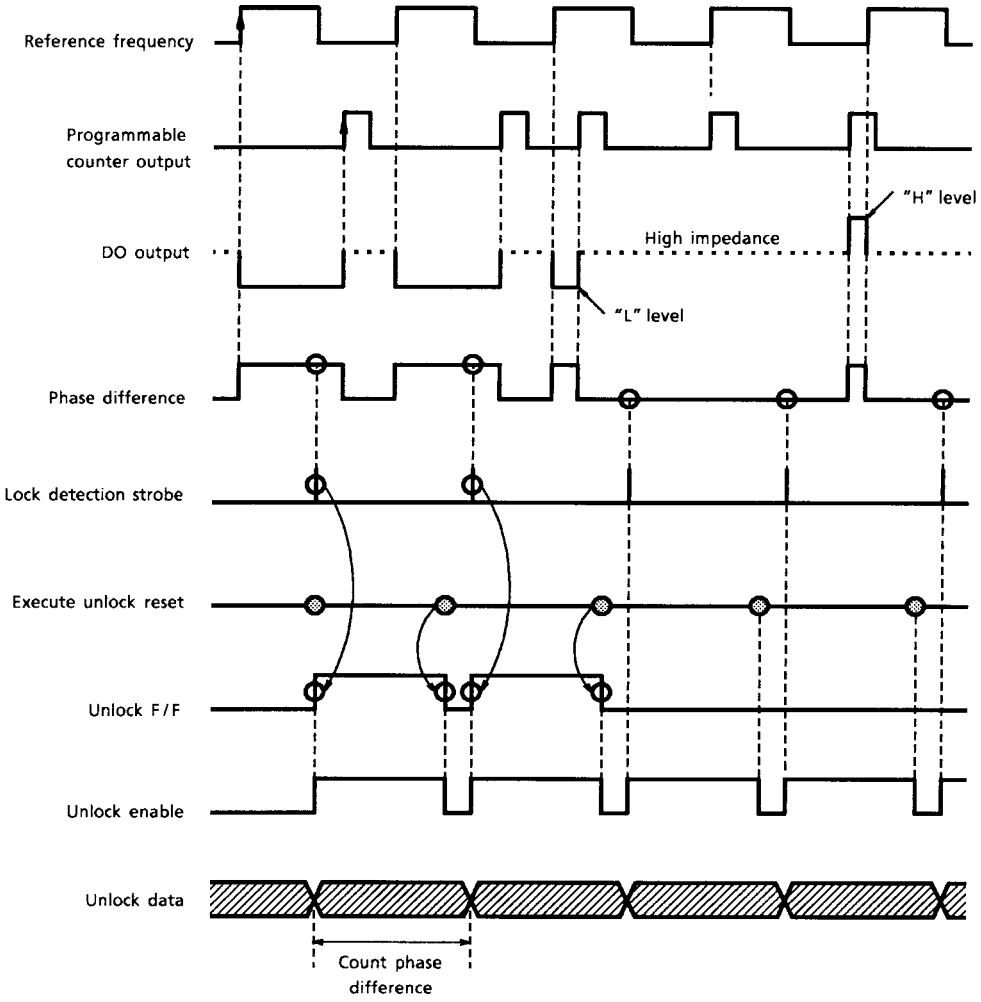
UNLOCK F/F detects when the phase is about 180° shift. It has the unlock data port that uses at more accurate detection of the phase difference. This port detects the phase difference as shown before table and is capable of detecting between –80 μs to +86.6 μs. However if setting to high reference frequency (at 25, 12.5 kHz setting), it can't detect under the half cycle of the reference frequency.

UNLOCK data port detects data constantly in the phase width between –180° to 180° of the reference frequency cycle. Normally after it is detected by UNLOCK F/F, the UNLOCK data will be referred.

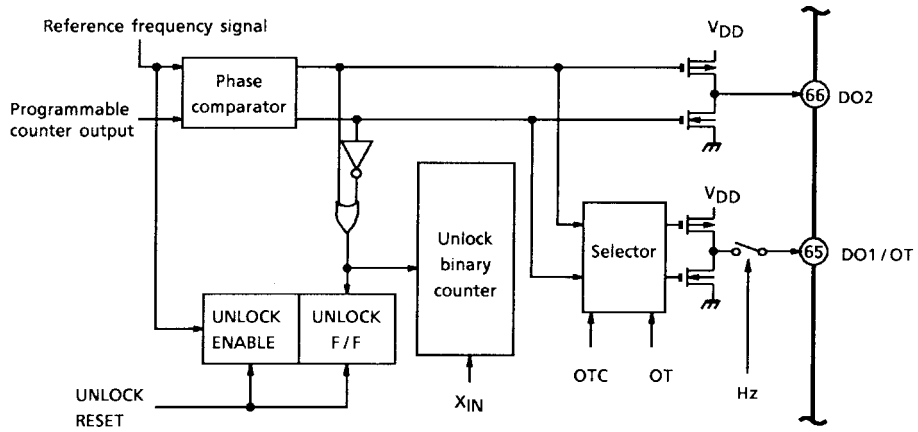
Control of each port and data loading are performed when OUT1/IN1 instruction designated [C_N = 7H or 8H] in the operand is executed.

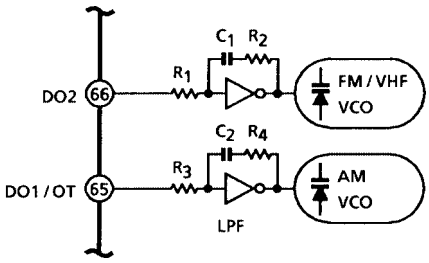
Note 28: When PLL OFF mode, the DO output becomes high impedance. However when DO1 is set as output port (OT output), the output data will be outputted directly.

2. Phase Comparator and Unlock Port Timing

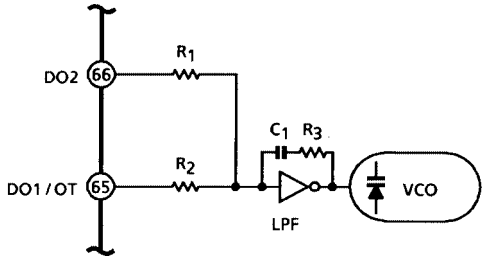


3. Phase Comparator and Unlock Port Circuit Construction

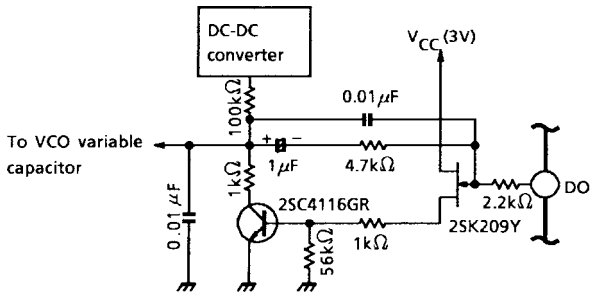




In Case of Setting the Filter Constant for Each Band



In Case of Using LPF in Common (switching of filter constant is done by setting DO1 to high impedance.)



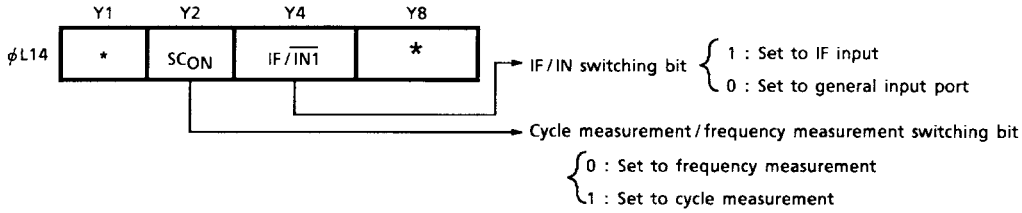
Example of Active Low Pass Filter Circuit (for reference)

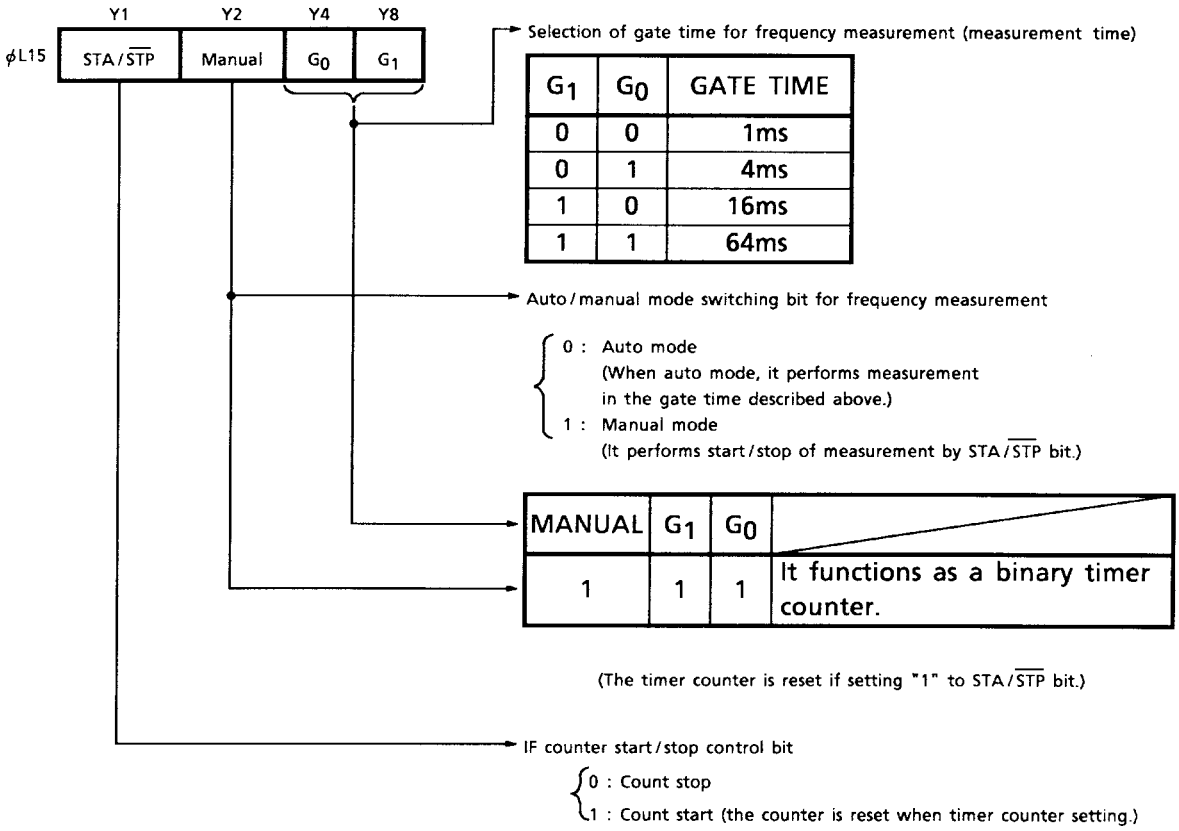
Note 30: Since the above filter circuit is just an example, the actual circuit should be examined and designed in accordance with the system band construction and desired characteristics.

IF Counter

It is a 20 bit general IF counter for counting FM/AM intermediate frequency (IF) and can be used for detecting the auto stop signal, etc. It also has a function to measure the cycle of a low frequency pilot signal. When not counting IF, this general IF counter can be used as a timer. The IF counter consists of 20 bit binary counter and control port.

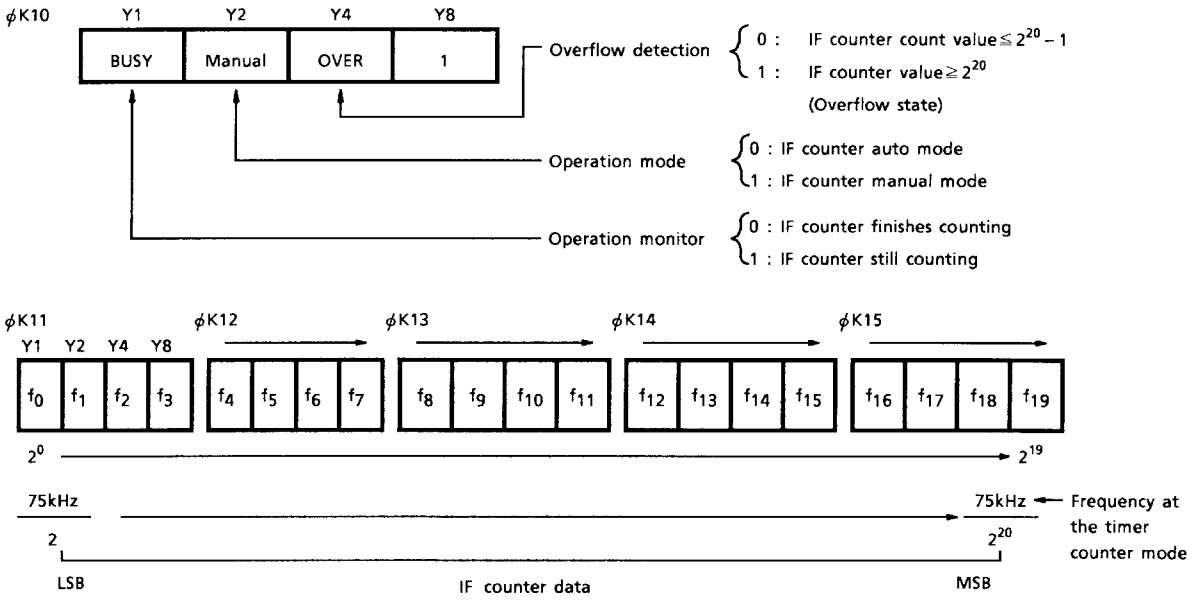
1. IF Counter Control Port, Data Port





G_1	G_0	GATE TIME
0	0	1ms
0	1	4ms
1	0	16ms
1	1	64ms

MANUAL	G_1	G_0	
1	1	1	It functions as a binary timer counter.



Note 31: The IF counter becomes disable at PLL off mode.

(it becomes enable at timer counter.)

(1) IF counter auto mode (frequency measurement)

The method to use IF counter auto mode is to set IF terminal to IF input by means of IF/IN switching bit and set SC_{ON} bit to "0".

To set the gate time for IF input frequency bandwidth and STA/$\overline{STP}$ bit to "1" while manual bit "0", then the IF counter is operated.

During the set gate time, the 20 bit binary counter is inputted a clock pulse from IF terminal, counted the inputted pulse and finished. Whether IF counter counting has finished or not, it can be judged by referring to BUSY bit. The OVER bit becomes "1" when a pulse number of more than 20 count value is inputted.

The frequency inputted to IF input terminal can be measured by loading f_0 to f_{19} IF data after judging that both BUSY bit and OVER bit are "0".

(2) IF counter manual mode (frequency measurement)

When the IF frequency is measured by the gate time which controlled by an internal time base (10 Hz, etc.), the manual mode is used.

In this mode, the setting IF counter input is set the same as auto mode. The G0/G1 bit data should be set except "1". Counting starts if setting Manual and STA/$\overline{STP}$ bits to "1". Counting stops if setting "0" to STA/$\overline{STP}$ bit and data will be loaded in binary.

(3) IF counter cycle mode (cycle measurement)

It is used for measuring the low frequency when it couldn't be measured by the frequency measurement.

In the cycle measurement, the cycle can be measured by judging this pulse number during the inputting reference clock (75 kHz) to the 20 bit binary counter.

As this input terminal, it uses as the IF input terminal, it switches to SC_{IN} terminal if setting SC_{ON} bit to "1".

It sets Manual, G0 and G1 bits to "0" when SC_{IN} setting.

The start of the cycle measurement is as same as the frequency measurement, the counting data is loaded after confirming the operation state by BUSY bit.

Note 32: Input rectang waveform by means of DC coupling when SC_{IN} input.

Note 33: The BUSY bit will not be "0" unless inputting a clock pulse to SC_{IN} bit.

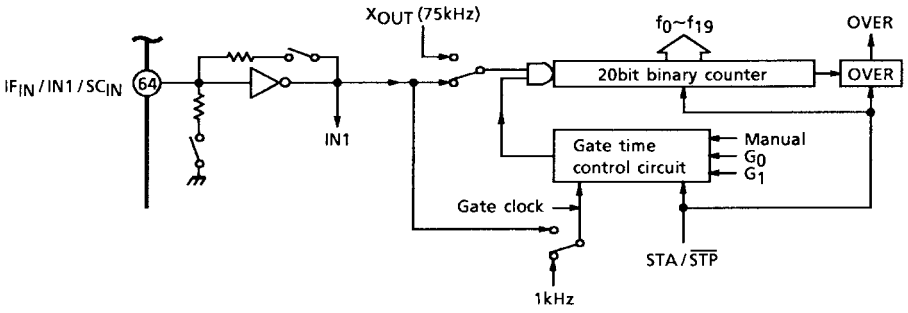
(4) Timer counter mode

When not using IF counter, it can be used as a timer binary counter.

If setting each Manual, G0 and G1 bit to "1", it will start counting a 75 kHz clock in binary as reference clock.

This counter will be reset whenever setting STA/$\overline{\text{STP}}$ bit to "1".

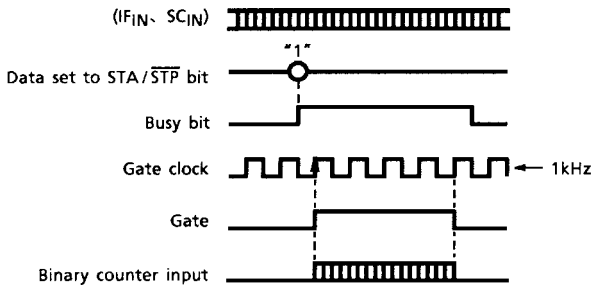
2. IF Counter Circuit Configuration



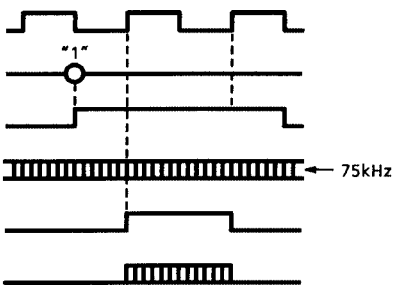
The IF counter consists of input amplifier, gate time control circuit and 20 bit binary counter.

The IF counter becomes OFF state when PLL OFF mode, but when timer counter is setting, the IF counter can be operatable.

Note 34: As an amplifier is built-in at IF_{IN} terminal, small amplitude operation is possible in coupling with capacitor.



Frequency Measurement Auto Mode



Cycle Measurement Mode

LCD Driver

The LCD driver is of 1/3 duty and 1/2 bias drive (167 Hz frame frequency) method.

The common output outputs three voltage potentials of V_{LCD}, $V_{LCD}/2$ (V_{EE}) and GND. The segment output outputs two voltage potentials of V_{LCD} and GND.

It is possible to display maximum 90 segments by combining three common outputs and 30 segment outputs.

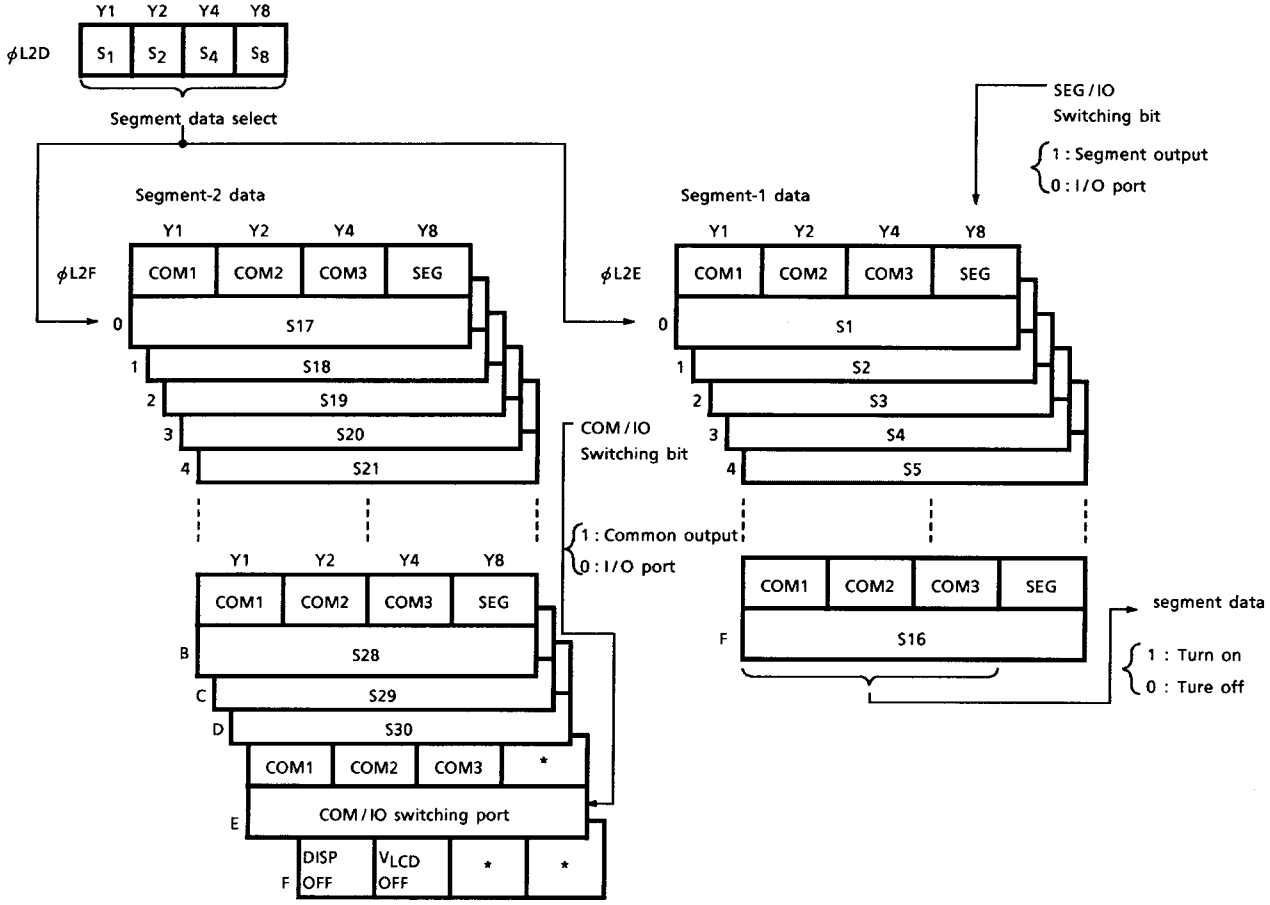
The LCD driver segment output of S_{19} to S_{30} is used both as the key return output for loading key matrix data.

As the LCD driver is built-in a constant voltage circuit for display (V_{EE} = 1.5 V) and voltage circuit to double (V_{LCD} = 3.0 V), the contrast of LCD display will not change even if supply voltage varies.

The LCD driver is capable of switching to I/O port in a unit of 1 bit and can be programmed according to the system.

(in this case, set V_{LCD} OFF bit to "1" and connect V_{LCD} terminal to V_{DD} terminal to use.)

1. LCD Driver Port



*: Don't care

Note 35: The segment data controls segment ON/OFF corresponding to the common and segment outputs.

Note 36: When system reset and clock stop mode cancellation, the DISP OFF bit is set to "1".

Note 37: When system reset, the contents of V_{LCD} OFF bit is set to "0".

Note 38: The S30 terminal becomes the input port (IN3) by switching to an I/O port.

The LCD driver control port consists of segment data select port and segment data port. These ports are accessed when OUT2 instruction designated [CN = DH-FH] in the operand is executed. The LCD driver can uses both as I/O port and this control is done by SEG/IO control bit (ϕL2E, ϕL2F). It will be segment output if setting "1" to this bit and I/O port if "0".

The LCD driver segment data is set at the segment data port (ϕL2E, ϕL2F). The LCD display turns off if setting "0" to the segment data port and turns on if setting "1". The segment –2 data (ϕL2FF) designated FH at the segment select port are DISP OFF bit and V_{LCD} OFF bit. The DISP OFF bit can turns off LCD display completely without setting segment data.

If setting "1" to this bit, the common output will be non-selected waveform and the LCD display will be completely OFF. The contents of the segment is held at this time and the preceding display will appear as it is if setting "0" to DISP OFF bit.

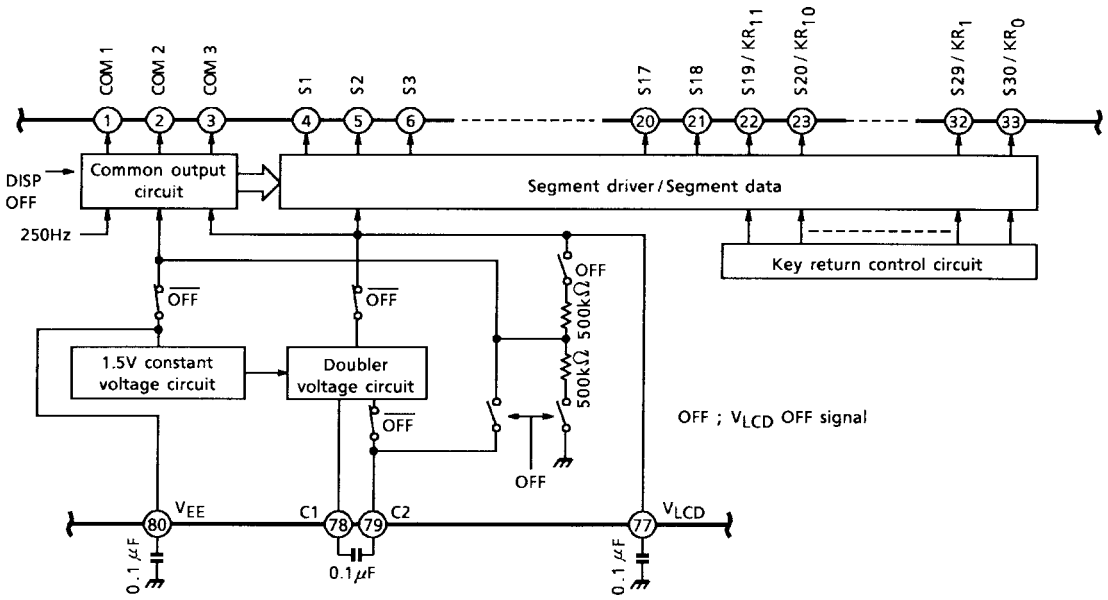
The segment data is rewritable during DISP OFF state. The DISP OFF bit be set to "1" after reset or after CKSTP instruction is executed.

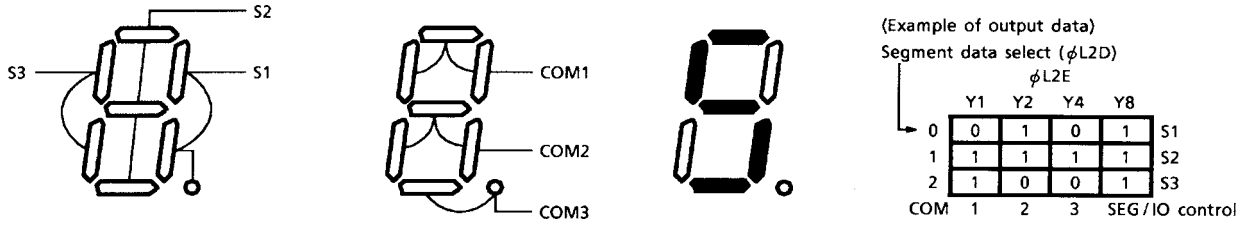
In case of using LCD terminal as I/O port, avoid LCD drive voltage supply booster (V_{LCD} terminal) as much as possible. The reason is that current consumption may increase dramatically by supply voltage (the relation between V_{LCD} and V_{DD} levels). In this case, the doubler voltage circuit is off state by setting "1" to V_{LCD} OFF bit and used as external input, then used connect V_{LCD} terminal to V_{DD}. At this time, LCD display contrast changes by supply voltage change, it's necessary to stabilize of supply voltage.

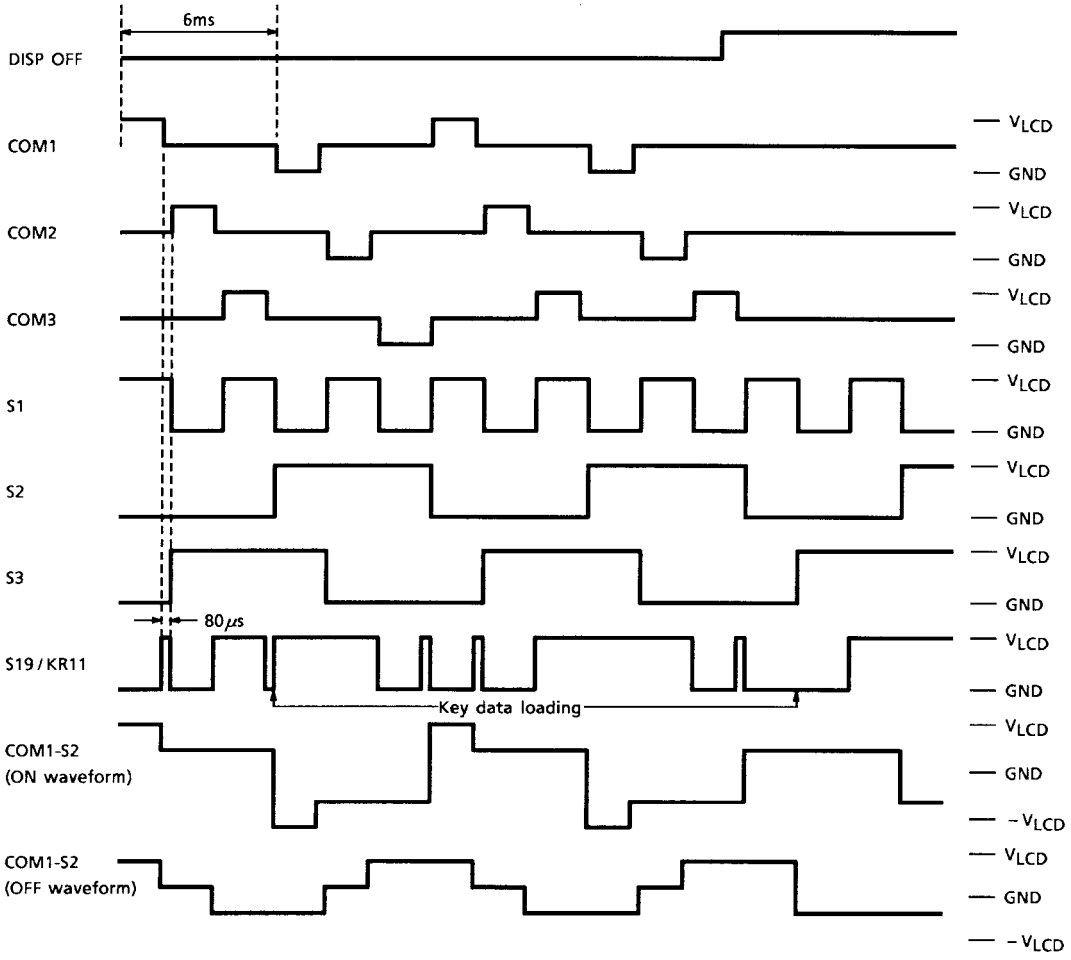
Further it can use the external supply which is efficient in changing the liquid crystal drive voltage by means of V_{LCD} OFF bit.

These data are outputted after they were divided by the segment data select port (ϕL2D). The segment output S_{19} to S_{30} terminal also uses both as the key return timing signal to load key matrix data. The segment output becomes the GND level by the timing as loaded a key data.

2. LCD Driver Circuit Configuration







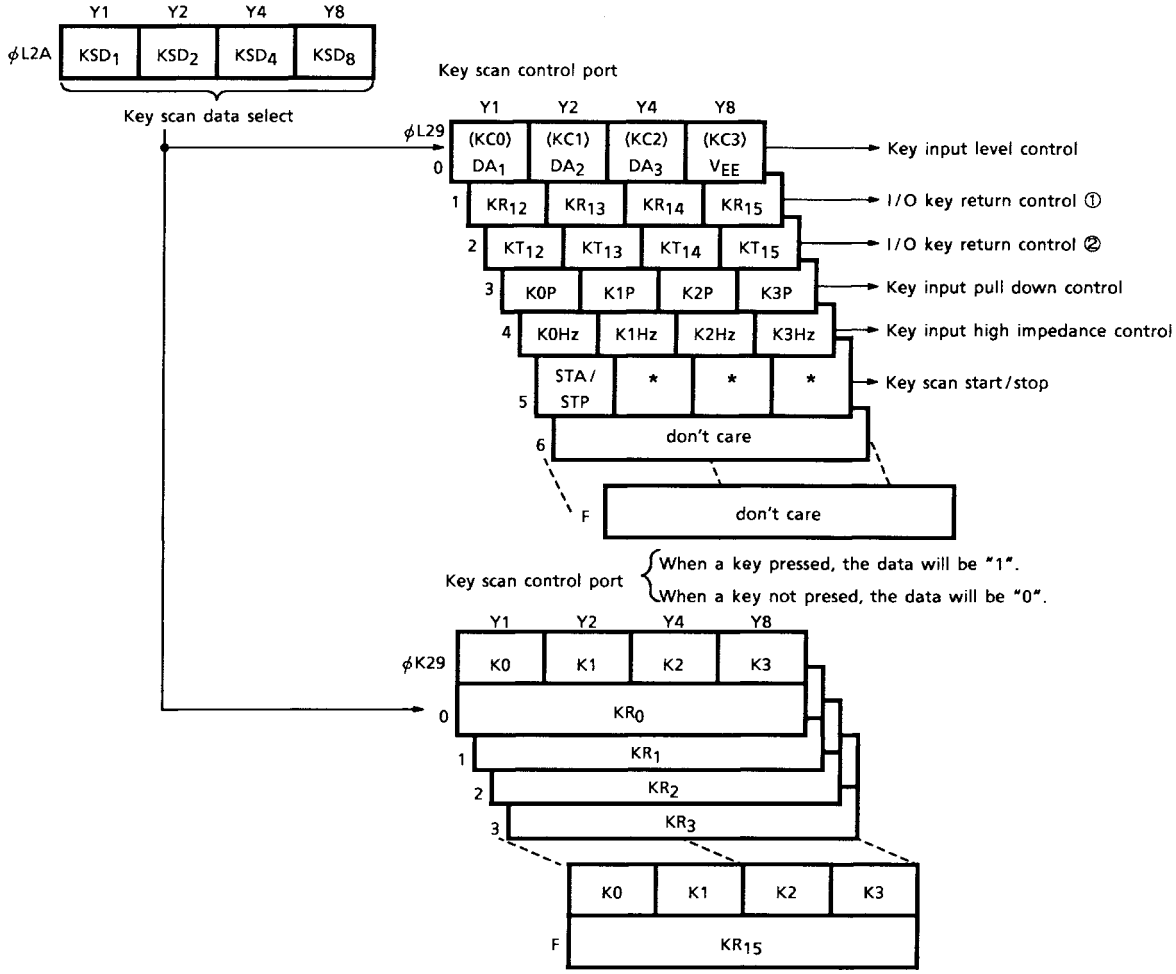
The LCD driver wave voltage potential outputs V_{LCD} and GND voltage potentials and half the intermediate level of these voltage potentials. A key return signal is outputted from S_{19} to S_{30} when this switching is performed. When loading key data, it becomes "L" level during 80 μs.

Note 39: When CKSTP instruction or initialization is executed, the common and segment terminal will be "L" level.

Key Input&Key Return Timing

Since there are four kinds of the key loading method, please design according to the system.

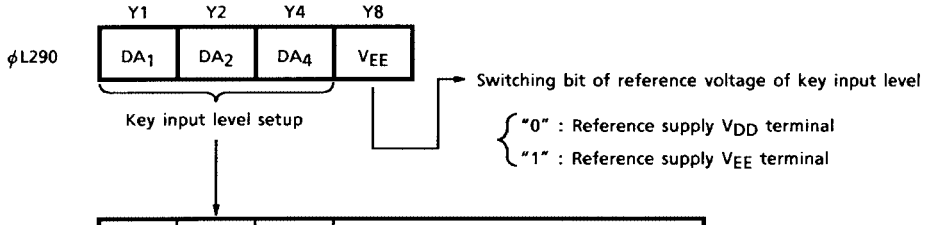
1. Key Control Port and Key Scan Data Port



The key scan control port is a port to excute the input level setting control key scan start/stop, setting of I/O port output form (P1-0 to P1-3) and key input form.

The key scanned key data are inputted to the key scan data port (φK29), and loaded into data memory by accessing to this port.

These ports are divided by the key scan data select port (φL2A), and by setting data to this port data corresponding to this data are accessed. When accessing to the key scan control port (φL29) or key scan data port, the key scan data select port (φL2A) is +1 incremented.

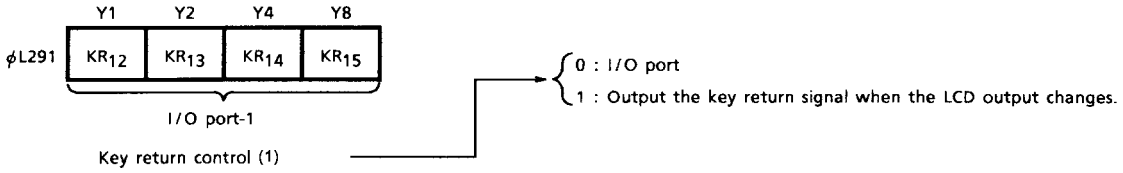


DA_3	DA_2	DA_1	KEY INPUT LEVEL (VKREF)
0	0	0	1/9×V
0	0	1	2/9×V
0	1	0	3/9×V
0	1	1	4/9×V
1	0	0	5/9×V
1	0	1	6/9×V
1	1	0	7/9×V
1	1	1	8/9×V

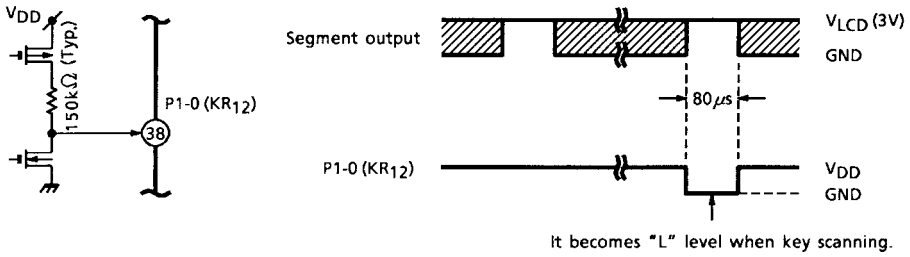
V: When V_{EE} bit is "1"; 1.5 constant voltage (V_{EE})

When V_{EE} bit is "0"; supply voltage (V_{DD})

It is a port to perform the key input level setting. The reference level of key input supply can be switched to V_{EE} terminal or supply voltage (V_{DD} terminal) by means of V_{EE} bit. By comparing the level that divides the reference supply by means of DA bit to the key input terminal level as shown in the above table, the result will be outputted to the key scan data port and key input data port.

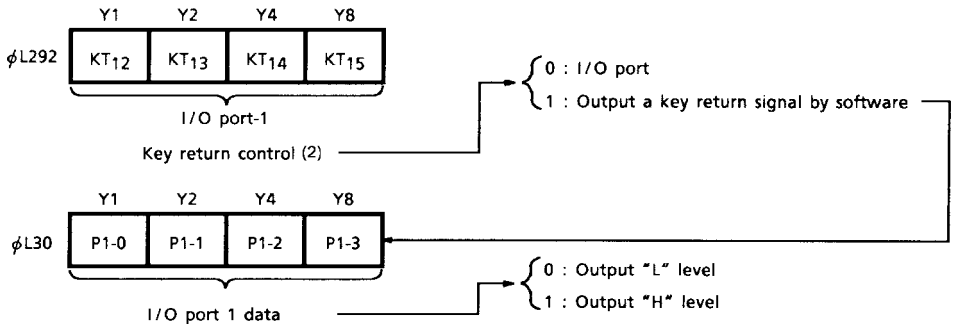


If setting "1" to this port, it becomes the output form as described below.

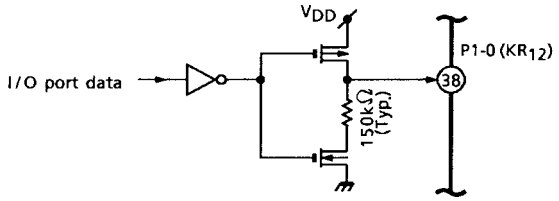


[output circuit and timing when setting KR_{12} bit to "1"]

The KR_{12} to KR_{15} bits correspond to P1-0 to P1-3 terminal, respectively. If setting "0" to this bit, it becomes an I/O port.



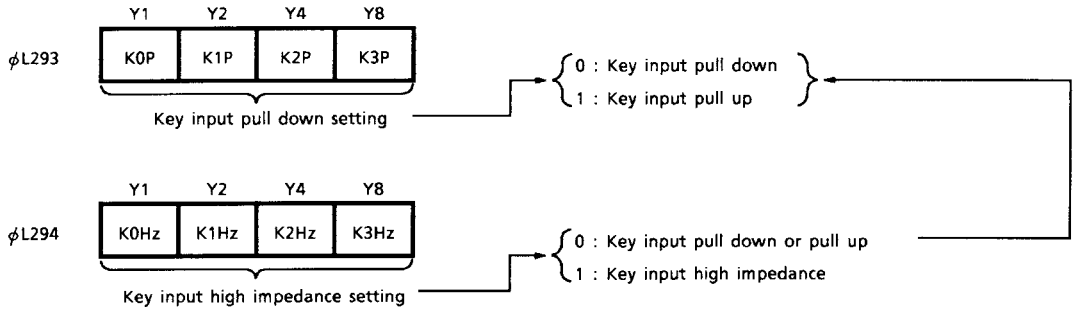
If setting "1" to the port of I/O port-1 key return control (2), it becomes the output form as described below. The "H" and "L" level settings of this output are controlled by the I/O port-1 data.



[output circuit when setting KT_{12} bit to "1"]

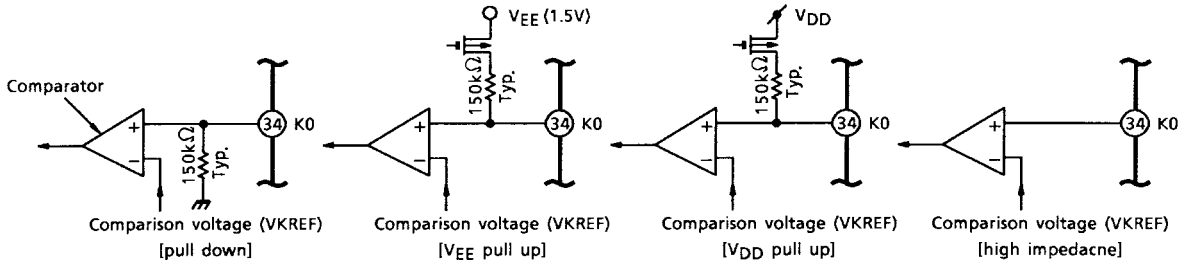
Each KT_{12} to KT_{15} bit corresponds to P1-0 to P1-3, respectively. If setting "0" to this bit, it becomes an I/O port.

When operating a key scan by means of the I/O port-1 key scan control port (1)&(2), the contents of I/O-1 control port is necessary to set the bit corresponding to the port to make key scan operate (the output port state [φL3F0]) to "1". In case of setting "1" to each of KR and KT bit, the KT bit is given priority.



These ports perform the input form setting of key input. The input form is set under the condition as below.

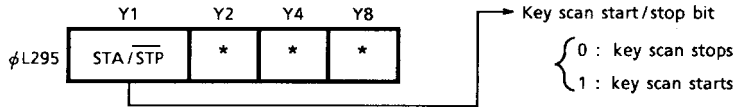
K0 Hz	K0P	Input Form
0	0	Pull down
0	1	V_{EE} pull up
1	0	V_{DD} pull up
1	1	High impedance



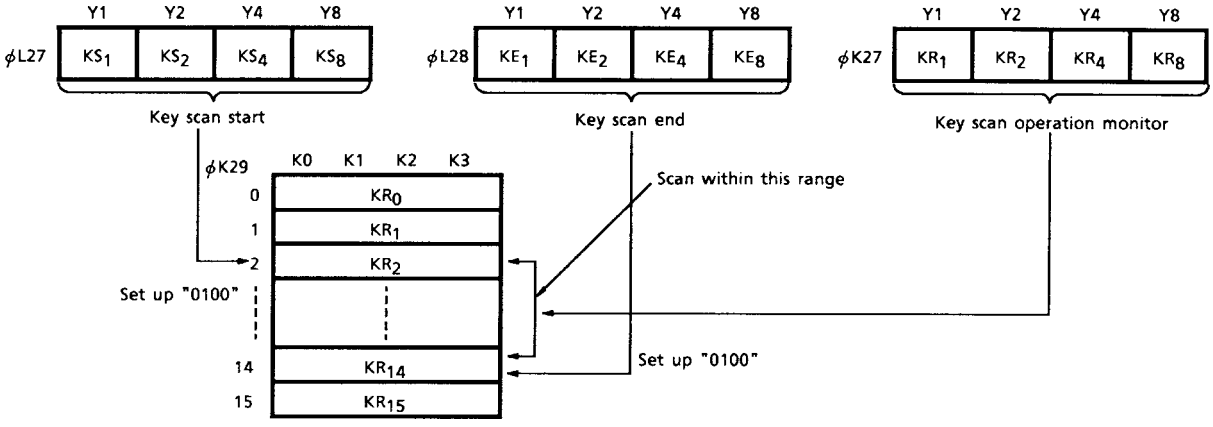
It will always be pull-down at pull down setting. At pull up setting, it will be pull-up only when LCD segment changes, otherwise it becomes high impedance.

At pull-down or pull-up setting, the key input terminal configures a key matrix in combination with the key return output signal. At high impedance setting, it can be used as a 3 bit A/D converter of the sequential comparison method by software.

Each of K0P to K3P bits and K0 Hz to K3 Hz bits correspond to K0 to K3 terminal. The key input terminal at pull-down setting, if "H" level ($V_{DD} \times 0.6$ V or more) is applied when WAIT mode, it cancels to execute WAIT instruction and it's possible to restart CPU operation. The CPU operation restarts only at "H" level setting and not at pull-up or high impedance setting.



Whenever setting "1" to STA/$\overline{\text{STP}}$ bit, it starts scanning from the key scan start port data. If setting "0" to this bit, it stops key scanning. When changing the key return control port or the contents of key scan start/end port described the following, to change after the key scan stopped and restart by setting "1" to STA/$\overline{\text{STP}}$ bit afterwards. If not set like this, a key except the ones between scan start data and scan end data may be loaded or key data within a cycle of scan may not be loaded.



The key scan start and end ports are ports to set up the range in which a key scan is performed and they perform scanning within the range between start data and end data.

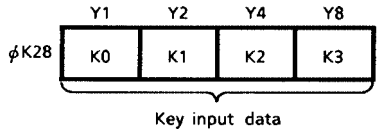
Set the data of these ports to be

"start data value ≦ end data value".

Which key line is loaded during scan operation can be judged by referring to the key scan operation monitor.

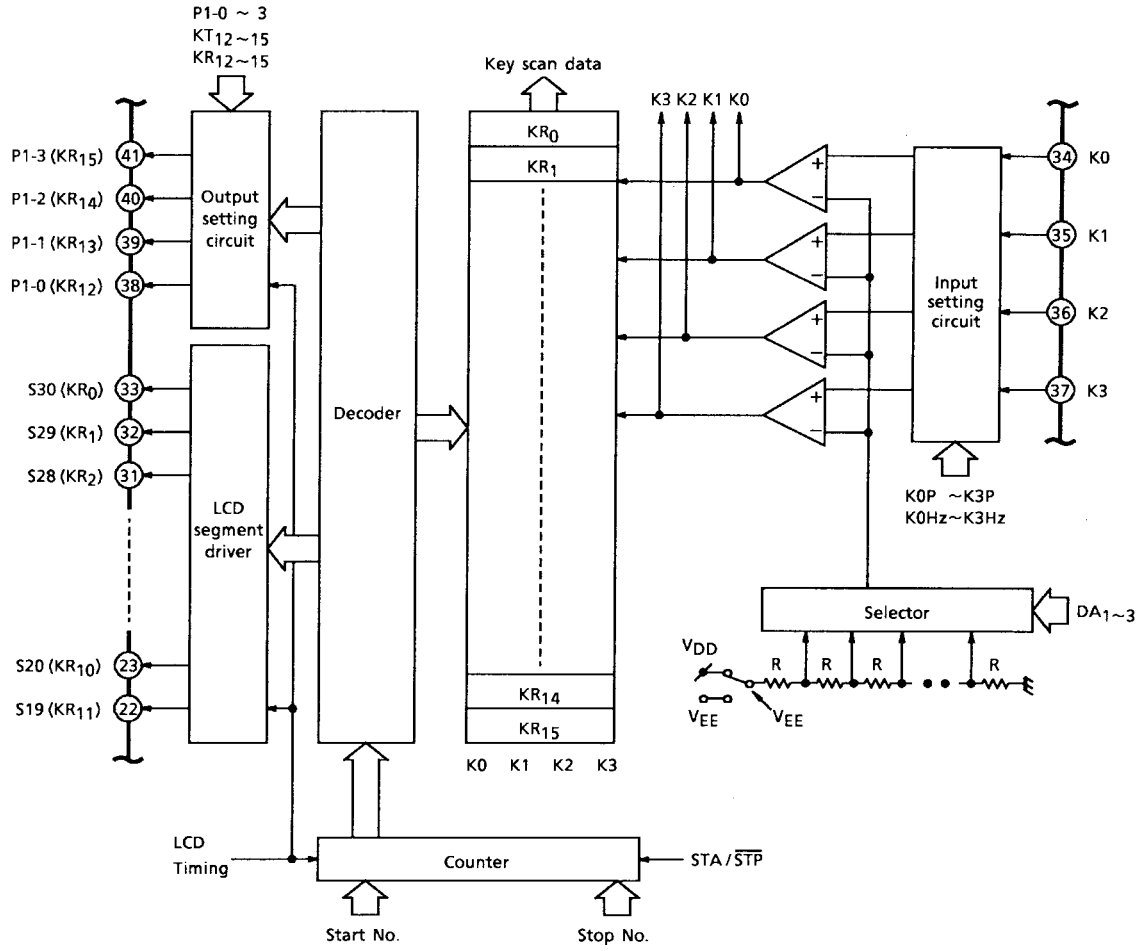
The key scan data (ϕK29) outputs "1" when a key pressed, and "0" when not.

Note 40: When supply voltage is less than 1.5 V by CPU stop function, the CPU stopped. And just after restarted, the key scan data is unknown. Due to this load key scan data into data memory after judging that key scan scanned one cycle by referring to STOP F/F.



From the key input data port, the key input data is loaded into data memory directly. If this is higher than comparison voltage, it becomes "1" and "0" if lower. These ports are accessed when OUT2/IN2 instructions designated [CN = 7H to AH] in the operand is executed.

2. Key Scan Circuit Configuration

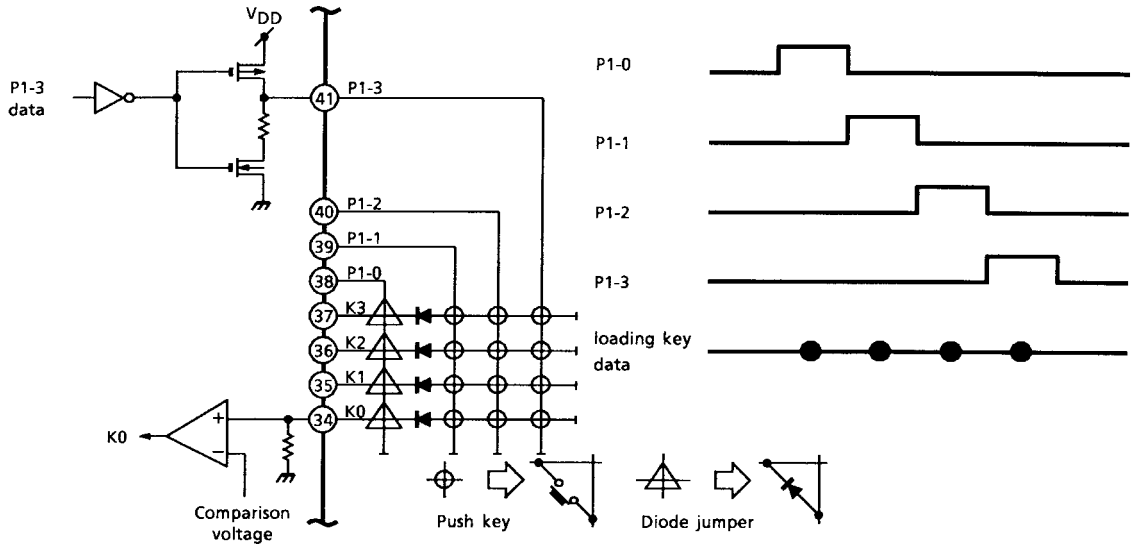


The key input of key scan circuit consists of input setting circuit, 3 bit D/A converter, comparator and latch circuit for loading key data. The key return timing output consists of output setting circuit of I/O port, LCD segment driver and counter/decoder to control I/O port output unit.

3. Key Matrix Configuration

The key matrix can be configured in the following four ways.

(1) Key data loading by software



When loading key data by program, it configures the key matrix as above.

The I/O port-1 data (ϕK30) which you want to load the key line is "H" level, is pressed load. The key input port (ϕL28) data into the data memory and judge whether the key or not. At this time, the I/O port -1 data not to be loaded should be set to "L" level.

If a key is pressed, the key input port data "1" is loaded into data memory and "0" if not pressed.

Only 4 × 4 = 16 key matrices are usable in this method. However, since data is loaded at high speed and the structure of high resistance is in N channel FET part of P1-0 to P1-3, it is unnecessary to have a diode for preventing reverse current owing to double key press.

As to the method for loading data by software, set the data to the port as described below.

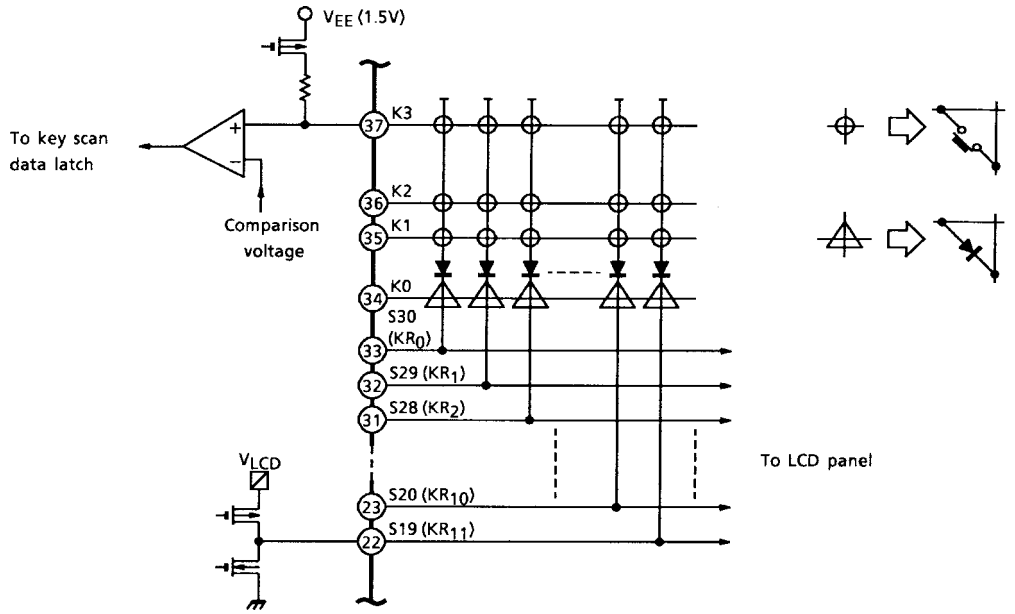
	DA1 to DA3	V_{EE}	KR_{12} to KR_{15}	KT_{12} to KT_{15}	K0P to K3P	K0 Hz to K3 Hz
With jumper	4/9 V_{DD}	0	All "0"	All "1"	All "0"	All "0"
Without jumper	3/9 V_{DD}	0	All "0"	All "1"	All "0"	All "0"

Note 41: In case of using as I/O output of I/O port -1, set the bit corresponding to KT_{12} to KT_{15} to "0".

Note 42: When configuring a diode jumper, voltage of diode VF (–0.6 V) lower than supply voltage is applied to the key input voltage. For this reason, the key input threshold value should be set low. As shown the above diagram, a diode for preventing reverse current owing to double key press is necessary. When configuring without a diode jumper, this diode is unnecessary.

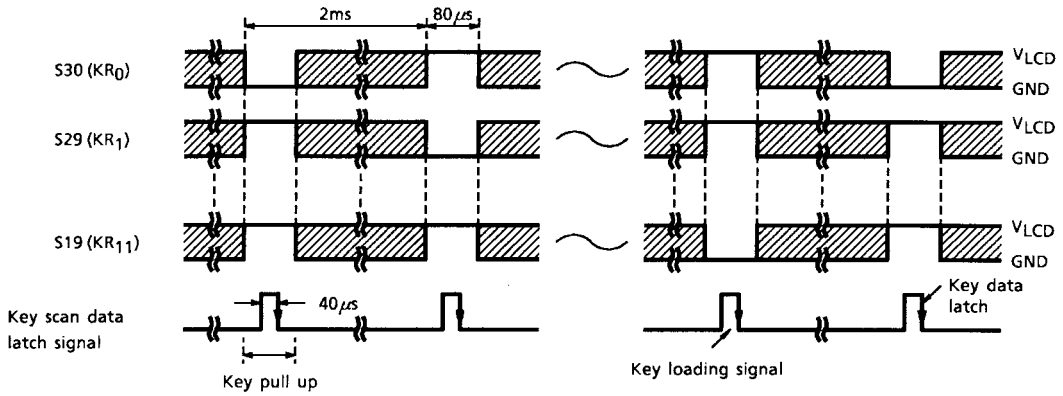
In such mode, adding "H" level (V_{DD} × 0.6 V or above) at WAIT mode, WAIT instruction execution is canceled and CPU operation is restarted. (the "H" level at this time is not related to DA_1 to DA_3 bits.)

(2) Key data loading by LCD segment output



Note 43: Maximum 4 × 12 = 48 key matrices can be configured.

Note 44: A push key and diode jumper cannot be mixed in the same key line. The position of diode jumper should be on the side of key return signal output.



In case of key data loading by means of LCD segment output, the key matrix as described in the preceding diagram is configured. A diode for preventing reverse current is necessary for this key matrix, therefore be careful for this diode and the diode jumper direction.

In this case, V_{LCD} (3 V) and GND voltage potentials are outputted from segment terminal when LCD output changes. When key data loading, the segment signal to load will be GND voltage potential at LCD output change and the key input terminal is pulled up to V_{EE} voltage potential. At this time, if a key is not pressed (or without diode jumper), V_{EE} level is inputted to the key input terminal and voltage worth of one diode voltage (–0.6 V) is inputted from GND voltage potential if a key is pressed (or with diode jumper).

The voltage potential inputted is compared with the D/A output level of which V_{EE} voltage potential is divided into nine and latches the signal comparated to the key scan data port corresponding to the segment output line of key loading.

This key data becomes "1" when a key is pressed and "0" when not.

As to the method for key loading by means of LCD segment output, set up the data described below to the port.

DA_1 to DA_3	V_{EE}	KR_{12} to KR_{15}	KT_{12} to KT_{15}	K0P to K3P	K0 Hz to K3 Hz
6/9 V_{EE}	1	All "0"	All "0"	All "1"	All "0"

If setting the range in which key scan is performed to the key scan start (ϕL27) and key scan end (ϕL28) and setting "1" to STA/$\overline{\text{STP}}$ bit after the above setting, key scan will load key data one after another within the setting range.

The time required to load one line key data takes 2 ms. Due to this the key scan data (ϕL29) will be loaded into data memory during referring to the key scan operation monitor.

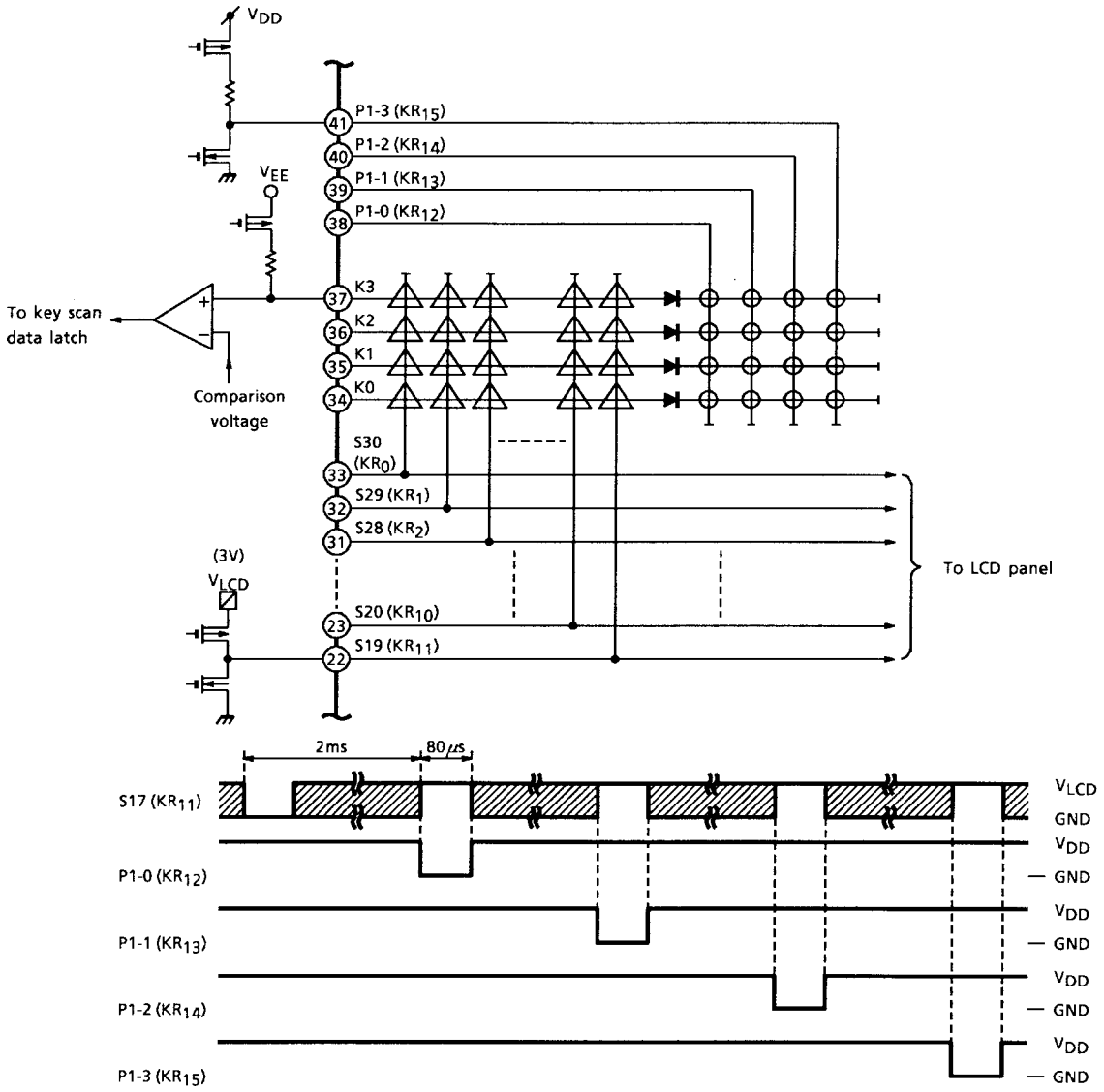
In case of changing the range in which key scan is performed, there are two ways as follows:

- Restart by setting "1" to STA/$\overline{\text{STP}}$ bit again after change.
- After stop the scan operation by setting "0" to STA/$\overline{\text{STP}}$ bit, change the range. Then start key scan again.

Note 45: Because the diode jumper data is stored in the latch, the data memory space can be utilized efficiently by referring to the contents of stored latch without loading into data memory, as needed. After CPU operation has stopped by CPU stop function and just after CPU restart, the contents of this latch will be unknown.

Note 46: The range in which key scan is performed is between KR_0 to KR_{11}.

(3) Key data loading by means of LCD segment output and I/O port (1)



The method to load key data by LCD segment output and I/O port is the same as that for loading key data by LCD segment output (3-(2)) except the following setting.

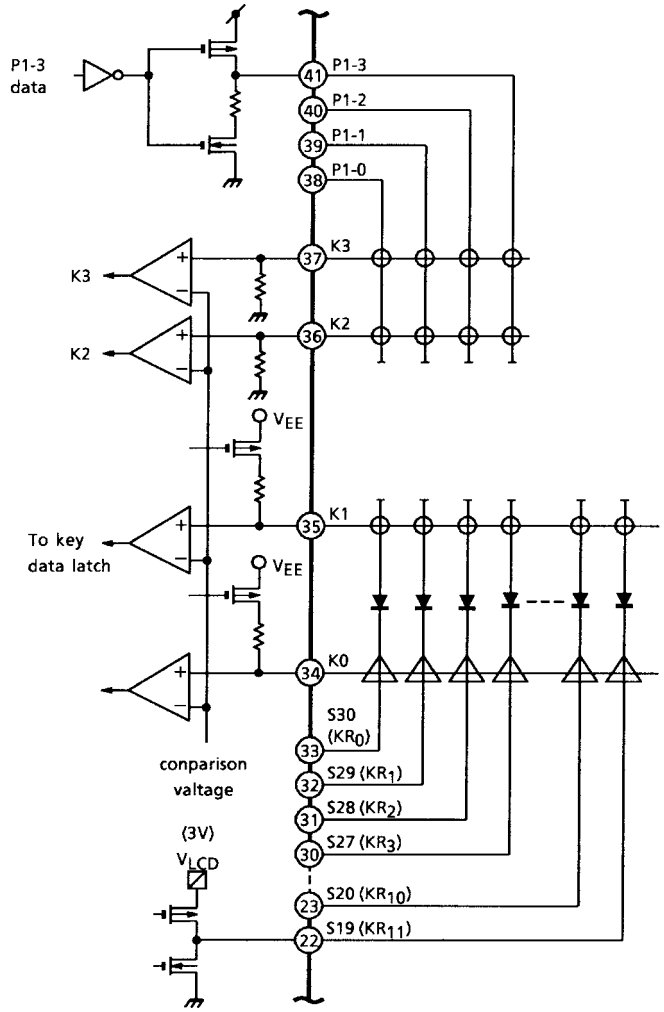
KR_{12} to KR_{15}	KT_{12} to KT_{15}
All "1"	All "0"

Note 47: In case of using as I/O output of I/O ports (P1-0 to P1-3), set the bit corresponding to KR_{12} to KR_{15} to "0".

Note 48: Maximum 4 × 16 = 64 key matrices can be configured.

Note 49: The configuration equivalent to the item 3-(2), [key data loading by means of LCD segment output] is possible at KR_0 to KR_{15}.

(4) Key data loading by LCD segment output and I/O port (2)



It is a usage method combining the key loading method by software and LCD segment output. (refer to 3-(1), (2).)

The characteristics of this method are below.

- It perform key loading on the I/O port side at high speed.
- It's possible to expand keys by allocating the keys which need not to load at high speed on the LCD segment output side.

As to key loading, the I/O port side performs it at input data port (ϕK28) and the segment output side at key scan data port (ϕK29).

Accessing to the key input data port can be done by switching comparison voltage of key input.

The setting of this method is performed as described below.

Setting of I/O Port Side

KR_{12}	KR_{13}	KR_{14}	KR_{15}	KT_{12}	KT_{13}	KT_{14}	KT_{15}
0	0	0	0	1	1	1	1

Key Input Setting

K0P	K1P	K2P	K3P	K0 Hz	K1 Hz	K2 Hz	K3 Hz
1	1	0	0	0	0	0	0

The key input settings on the I/O port side and on the LCD segment output side can be done in a unit of 1 bit.

Note 50: In WAIT mode, supplying "H" level ($V_{DD} \times 0.6$ V or more) to the key input terminal whose key input is set to pull down (K2 and K3 terminal in the above diagram), WAIT instruction execution is cancelled and CPU operation is restarted.

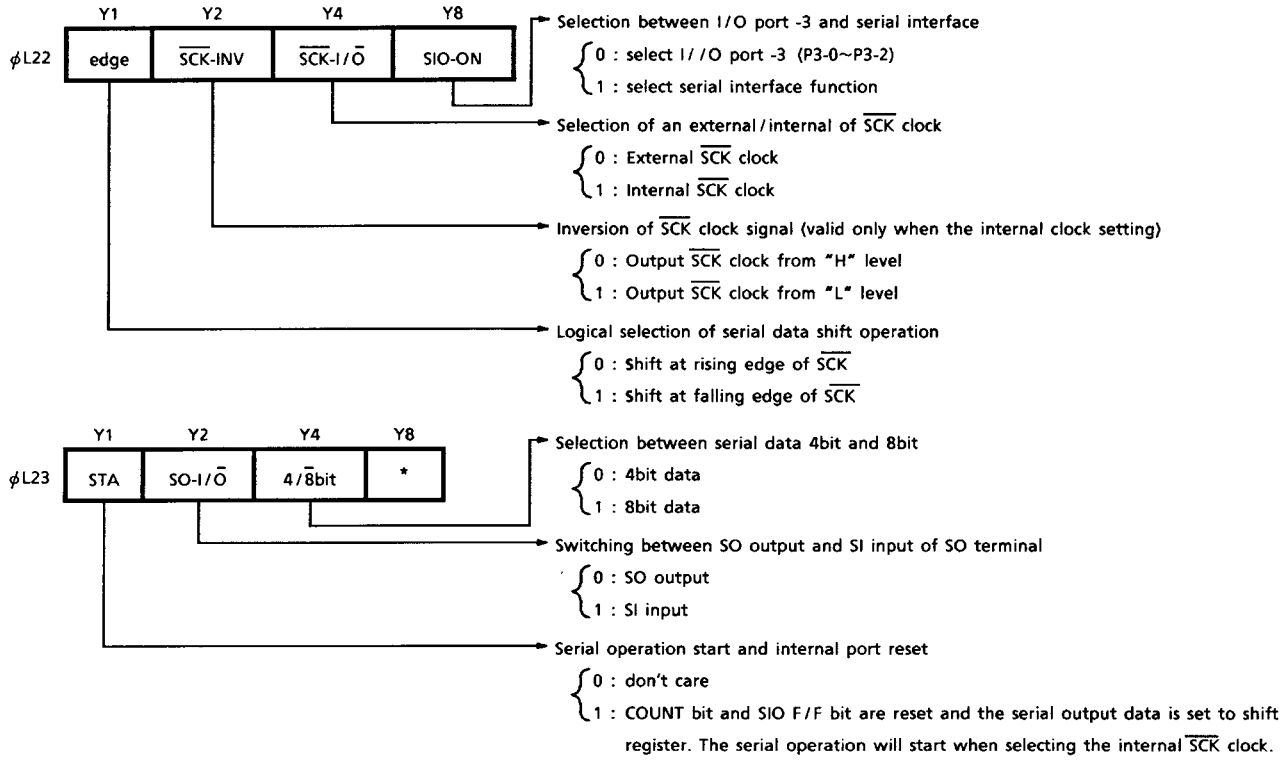
Note 51: Key data on the segment side is loaded when LCD segment changes. Therefore, if at the same time loading data on the I/O port, the key input threshold level will be different and data on the segment side will be loaded by mistake. For this reason, control by key scan operation monitor will be required.

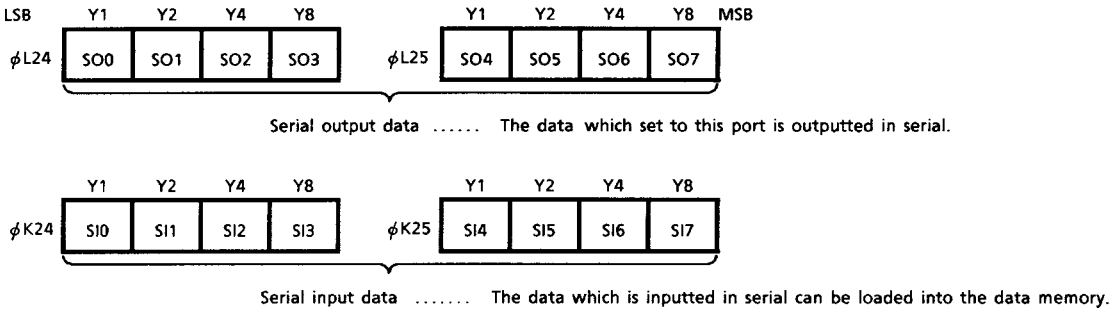
Note 52: Set the contents of I/O port -1 control port (ϕL3F0) to all "1" (output setting).

Serial Interface

The serial interface is a serial I/O port to send/receive synchronously 4 or 8 bit data with an internal/external serial chock. By means of SI, SO and $\overline{SCK}$ terminals, it performs sending/receiving data of LSI (for expansion) and microcomputer, etc.

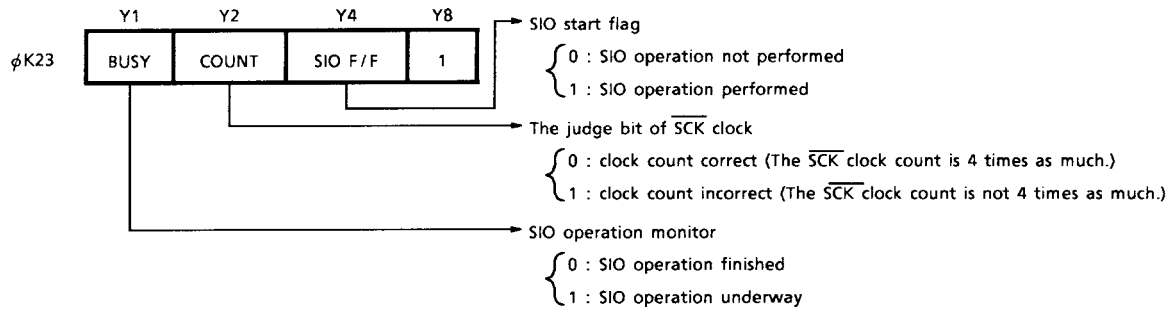
1. Serial Interface Control Port and Data Port





Note 53: As for the serial input data, the contents of shift register is directly acceessed.

Note 54: After system reset, the contents of serial interface control port (φL22, φL23) is reset to "0".



The serial interface control and serial data are accessed when OUT2/IN2 instruction designated [CN = 2H-5H] in the operand is executed. The serial interface terminal is combined with P3-0, P3-1, P3-2 of I/O port and if setting "1" to SIO ON bit, each I/O port-3 terminal is switched to SI, SO and $\overline{SCK}$ terminal, respectively.

(1) $\overline{SCK}$-INW, $\overline{SCK}$-I/$\overline{O}$ bit

The $\overline{SCK}$-INV and $\overline{SCK}$-I/$\overline{O}$ bits are bits to set the input and output form of $\overline{SCK}$ terminal. By means of this bit data, the condition as described following will be set.

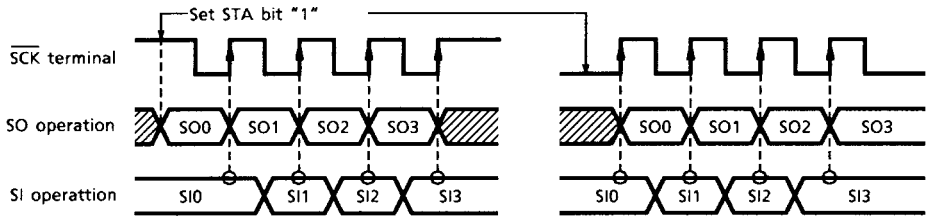
$\overline{SCK}$ Terminal State

INV	I/$\overline{O}$	Input/Output	$\overline{SCK}$ Clock Waveform
0	0	Output	
1	0	Output	
*	1	Input	—

(2) Edge bit

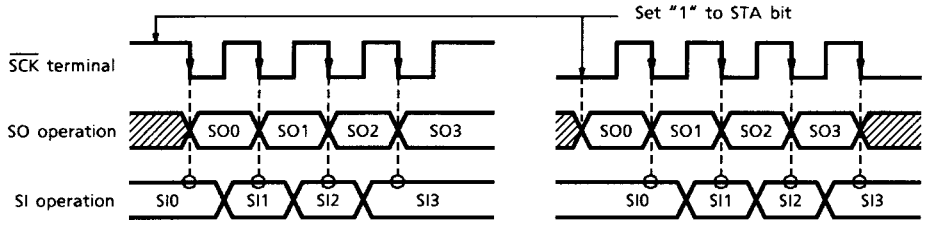
The edge bit sets the shift logic of serial data. By means of this data, data will be shifted as shown below.

- When edge = "0"



When setting the edge bit to "0", the SO output is outputted at rising edge of $\overline{SCK}$ clock, and the SI input, as well as the SO output, is inputted to shift register at rising edge of clock.

- When edge = "1"

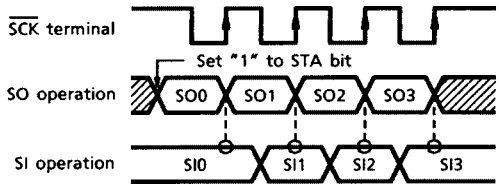


When setting edge bit to "1", SO output is outputted at falling edge of $\overline{SCK}$ clock, and SI input as well as SO output is inputted to shift register at falling edge of clock.

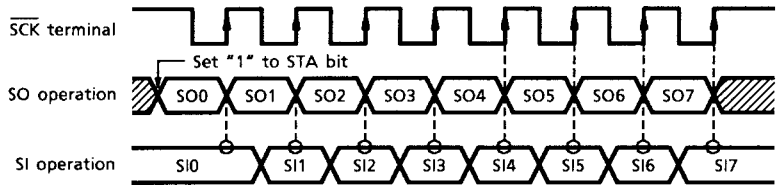
(3) $4/\overline{8}$ bit

The $4/\overline{8}$ bit is a bit to select the serial data length. When this bit is "0", it becomes 4 bit length and 8 bit length when "1". If selecting the 4 bit at an internal clock, $\overline{SCK}$ clock outputs 4 clocks and 8 clocks if 8 bit.

- When $4/\overline{8}$ bit is "0", (in case of edge = "0", SCK-INV = "0")



- When $4/\overline{8}$ bit is "1", (in case of edge = "0", SCK-INV = "0")

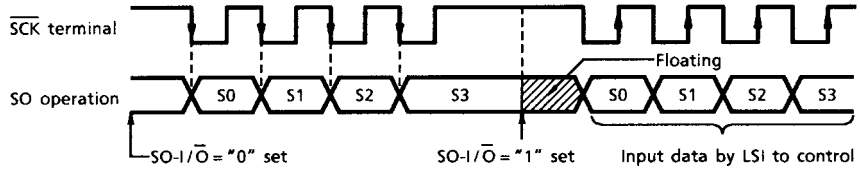


(4) SO-$I/\overline{O}$ bit

The SO-$I/\overline{O}$ bit is a bit to set the serial input/output of SO terminal.

When setting SO-$I/\overline{O}$ bit to "0", SO terminal outputs the serial data. When setting this bit to "1", it becomes the serial data input.

By means of controlled this bit, LSI of serial bus system such as T-BUS which conducts data input/output by one terminal can easily be controlled.



Note 55: In this case, it is necessary to pull up SO terminal for the floating timing.

In this system, when transmit mode, it performs SIO operation by setting data to the serial output data port. When receiving, it performs SIO operation after SO terminal is set to input and loads the contents of the serial input data port into the data memory. Also when selecting the serial interface, SI terminal is controllable as I/O port (P3-0). The I/O output (P3-0) can be used as strobe pulse terminal in T-BUS, etc.

Note 56: When SI terminal is use as serial data input mode, P3-0 bit of I/O control port which corresponding to I/O port-3 should be set to "0".

(5) Serial interface operation monitor

The operational state of serial interface can be judged by referring to BUSY, COUNT or SIO F/F bit.

Since BUSY bit will be "1" during SIO operation, control data switching and serial data access will be done when BUSY bit is "0".

The COUNT bit is a bit to judge whether data transmitting/receiving was performed in a unit of 4 bit. In case shift operation is performed by multiple of 4, this bit outputs "0" and in case shift operation is not performed by multiple of 4, it outputs "1".

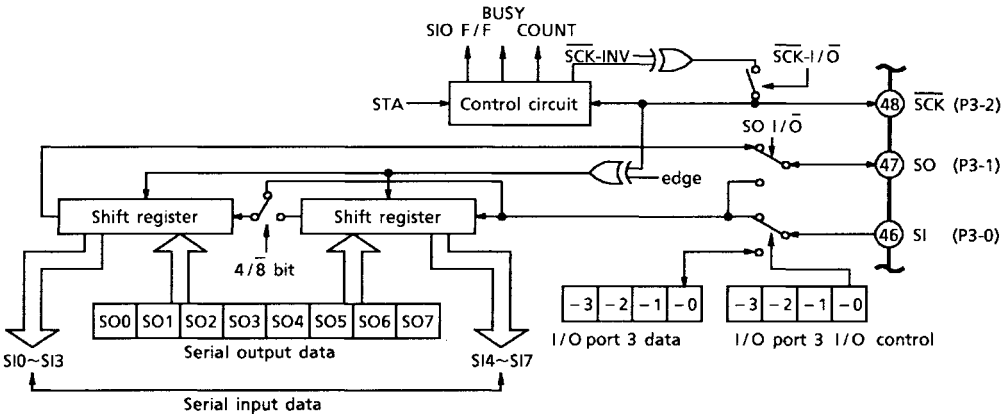
The SIO F/F bit is set to "1" when $\overline{SCK}$ terminal starts clock operation.

The COUNT bit and SIO bit are all reset to "0" if setting "1" to STA bit. These two bits are mainly used when $\overline{SCK}$ terminal is set to an external clock. It can be judged that information that an external clock was inputted and serial data was transfered/received and if operation was properly performed.

(6) STA bit

Whenever setting "1" to STA bit during $\overline{SCK}$ internal clock setting, serial output data will be set to shift register and clock pulse will be outputted from $\overline{SCK}$ terminal to start shift operation. At the same time COUNT bit and SIO F/F bit will also be reset to "0".

2. Serial Interface Configuration



The serial interface consists of: control circuit, shift register and I/O port.

Note 57: The SI terminal can directly be used as I/O port-3 (P3-0).

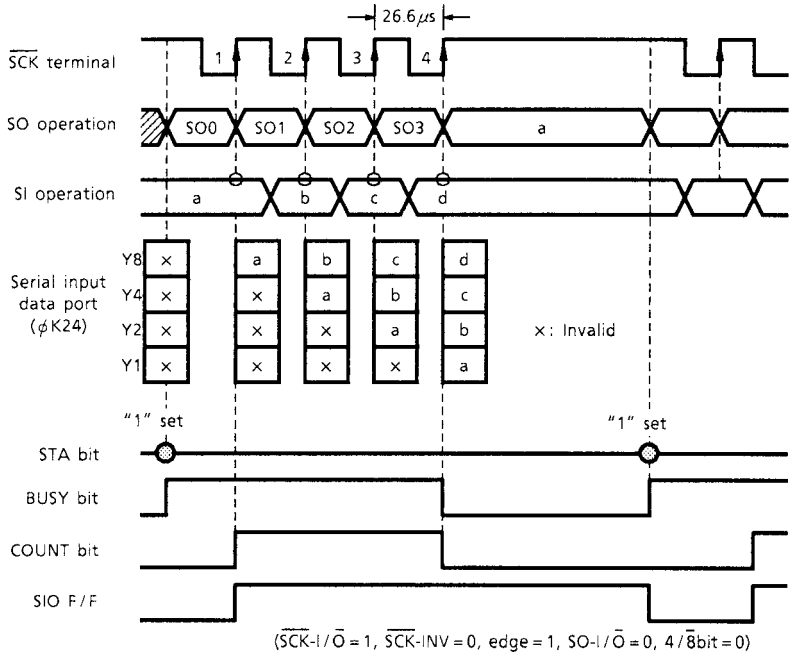
Note 58: The contents of data set to serial output data do not accord with the contents of serial input data.

Note 59: The SI terminal set as SI input, $\overline{SCK}$ terminal set as $\overline{SCK}$ input and SO terminal set at input will be all Schmitt inputs.

3. Serial Interface Timing

When setting $\overline{\text{SCK}}$ clock to an internal clock, the clock frequency outputted from $\overline{\text{SCK}}$ terminal is 37.5 kHz (duty 50%).

The example of serial interface timing is as shown below.

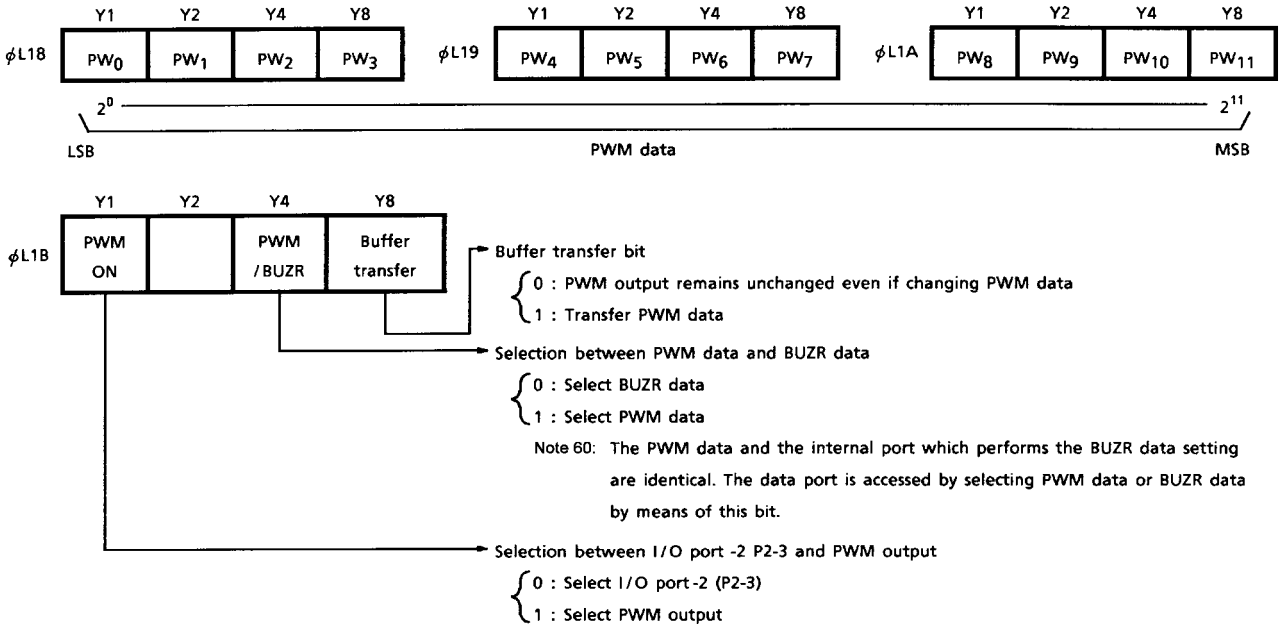


[example of serial interface timing]

D/A Converter (pulse-width modulation: PWM) Output

The pulse-width modulation output (PWM) can obtain D/A conversion output easily by external low-pass filter. The PWM output is a 12 bit resolution and has one-channel output.

1. PWM Control Port and Data Port



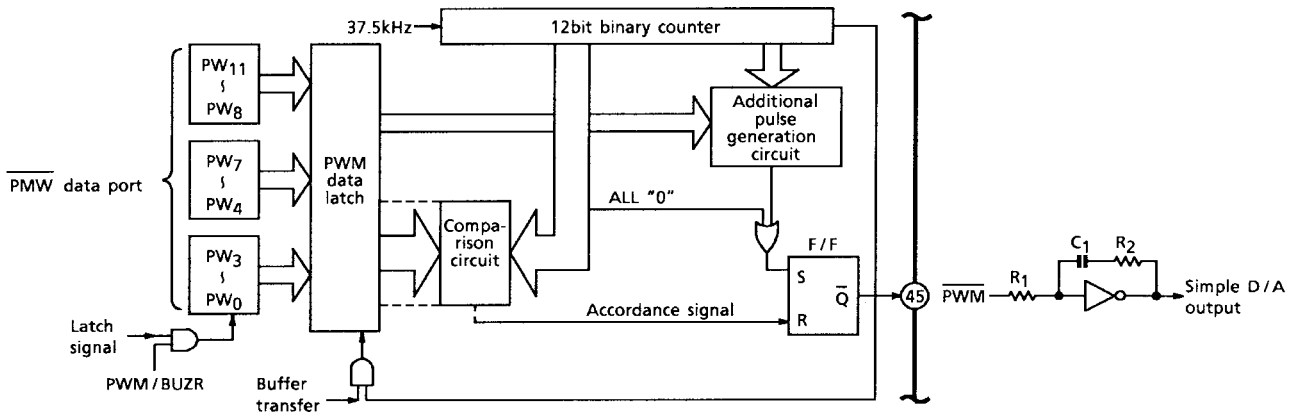
The $\overline{\text{PWM}}$ output combines the P2-3 I/O port. When the setting of $\overline{\text{PWM}}$ output, the P2-3 switches to $\overline{\text{PWM}}$ output by setting $\overline{\text{PWM}}$ ON bit to "1".

The PWM data setting is done after setting PWM/BUZR bit to "1" and buffer transfer bit to "0". If setting "1" to buffer transfer bit after PWM data setting, the PWM data will be transferred to PWM data latch. After setting "1" to buffer transfer bit, maximum times of 109 ms is required. The $\overline{\text{PWM}}$ output would not chnage if this bit is set to "0" before transferring to PWM data latch.

In PWM data, PW0 is LSB and PW22 is MSB. The high 8 bit (PW4-11) data controls the pulse-width of pulse output. The low 4 bit (PW0-3) data controls the position to output the pulse that was added during one cycle of $\overline{\text{PWM}}$ output.

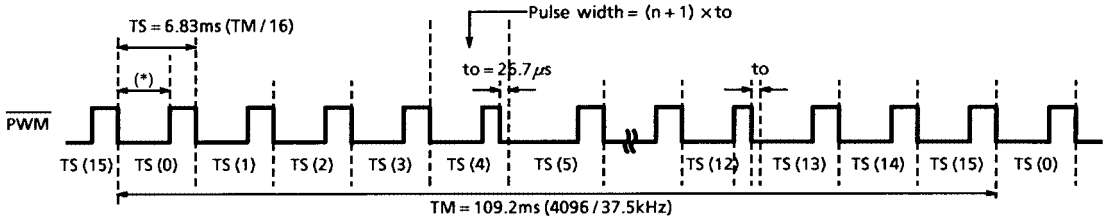
These data settings are performed when OUT1 instruction designated [CN = 8H to BH] in the operand is executed.

2. $\overline{\text{PWM}}$ Output Circuit Configuration



The $\overline{\text{PWM}}$ output circuit consists of: 12 bit binary counter, PWM latch and comparison circuit.

3. $\overline{PWM}$ Output Waveform



*: Pulse width n × to

n: PW_4 to PW_{11} data value (0 to 255)

to: 26.7 μs

Example of $\overline{PWM}$ Output Timing (there are additional pulses in TS (4), TS (12): PW_1 bit "1")

PW Data Bit	The Range in which an Additional Pulse is Outputted (○ marks the position to be added).															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PW_0									○							
PW_1					○								○			
PW_2			○				○				○				○	
PW_3		○		○		○		○		○		○		○		○

Note 61: The above numbers indicate the i value of TS (i). When PW data bit is "1", the additional pulse is outputted to the above ○ position.

One wave cycle of $\overline{PWM}$ output is TM = 2^{12}/37.5 kHz = 109.2 ms and it outputs a pulse of 12 bit resolution. The high-order 8 bits, PW4 to PW11 of PWM data controls the pulse-width of pulse output whose cycle is TS (TS = TM/16 = 6.834 ms). When the value of PW4 to PW11 is n (n = 0 to 255), the low level pulse width whose cycle is TS will be n × to (to = 1/37.5 kHz).

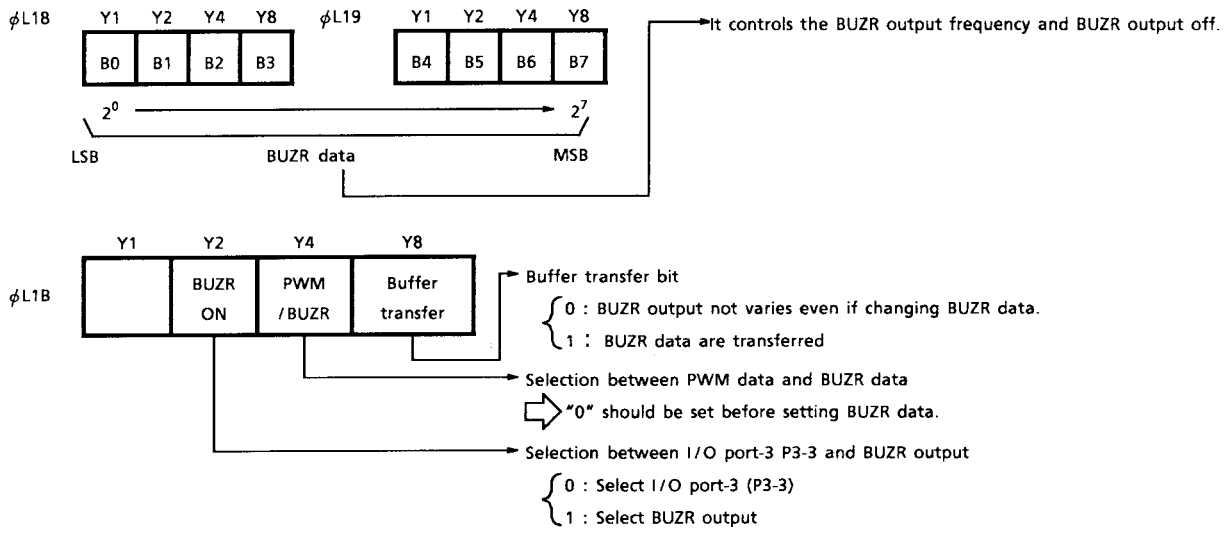
The low-order 4 bits, PW0-3 controls the position to output the additinal pulse of "to" width in TS (i) (i = 0 to 15) between 16 sections within TM cycle. In the section where an additional pulse is outputted, the low level pulse-width will be (n + 1) × to.

When the low-order bit data are m (m = 0 to 15), an additional pulse is outputted at m point within TS (i) section. The section where this additional pulse is outputted is shown in the preceding table. (however, the additional pulse is not outputted within TS (0) section.)

Buzzer Output (BUZR)

The buzzer output is usable for outputting the confirmation and alarm sounds when key operation or tuning scan mode. The buzzer frequency can freely be set and outputs a 50% duty waveform.

1. BUZR Control Port and Data Port



The BUZR output combines the P3-3 I/O port. When BUZR output setting, the BUZR on bit is set to "1", then the P3-3 output switches to BUZR output.

The BUZR data setting will be done after setting both PWM/BUZR bit and buffer transfer bit to "0". If setting "1" to buffer transfer bit after BUZR data setting, the BUZR data will be transferred to the BUZR data latch and the BUZR frequency will change.

The frequency of dividing 75 kHz into 2 × n (n: B0 to B7 value) is outputted to BUZR output and the B0 to B7 setting and frequency ranges are:

$$2 \leqq n \leqq 255 \qquad \frac{75\,\mathrm{kHz}}{2\times 2}=18.75\,\mathrm{kHz} \leqq f_{BUZR} \leqq \frac{75\,\mathrm{kHz}}{2\times 255}=147\,\mathrm{Hz}$$

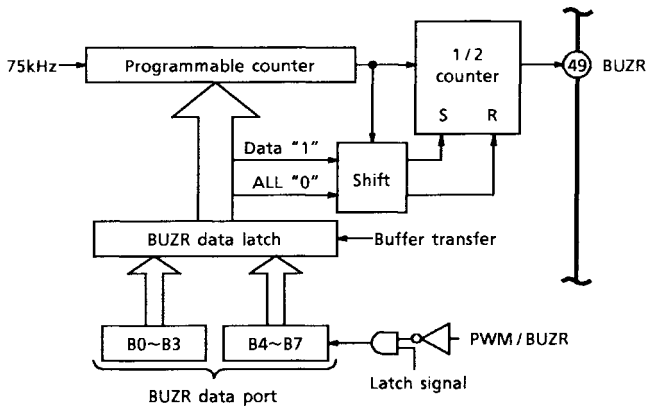
If the B0 to 7 setting is lower than 1, it will be the condition as described below.

B7	B6	B5	B4	B3	B2	B1	B0	BUZR Output
0	0	0	0	0	0	0	0	Fixed at "L" level
0	0	0	0	0	0	0	1	Fixed at "H" level

These data settings are performed when OUT1 instruction designated [C_N = 8H to BH] in the operand is executed.

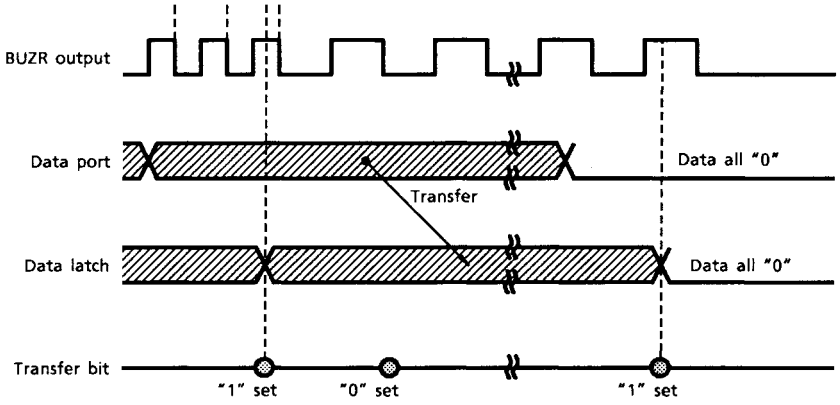
Note 62: The BUZR ON bit will be reset to "0" after system reset.

2. BUZR Circuit Configuration



The BUZR circuit consists of: 8 bit programmable counter, 1/2 counter, BUZR latch and BUZR port.

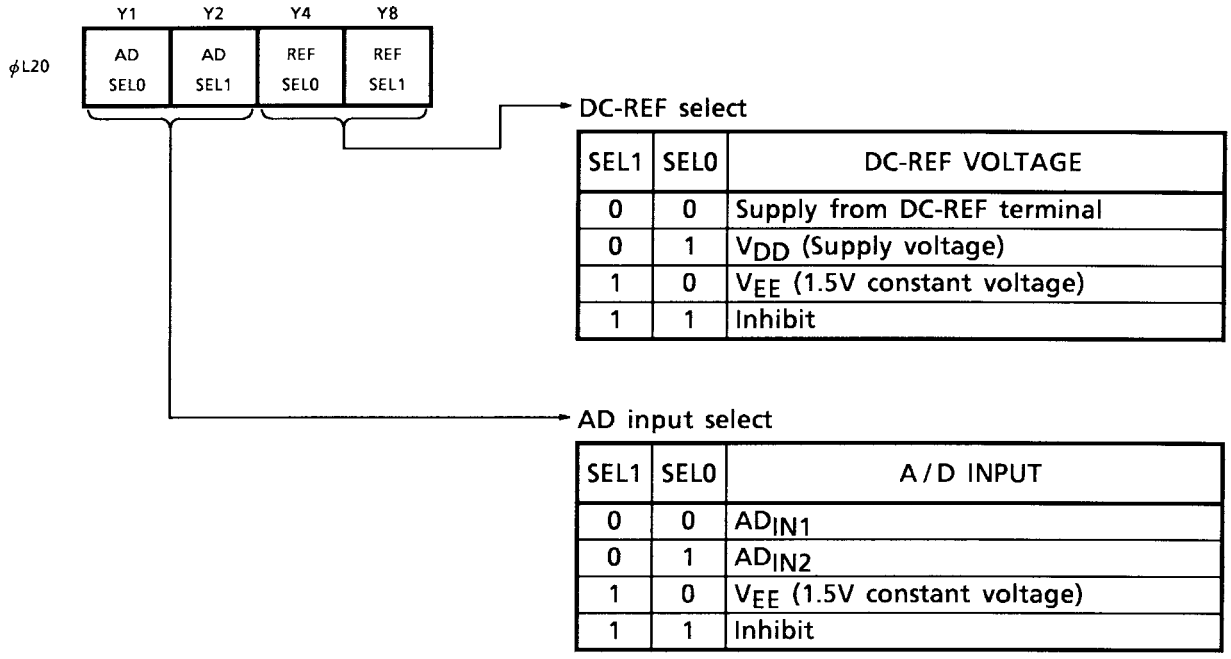
3. BUZR Output Timing



A/D Converter

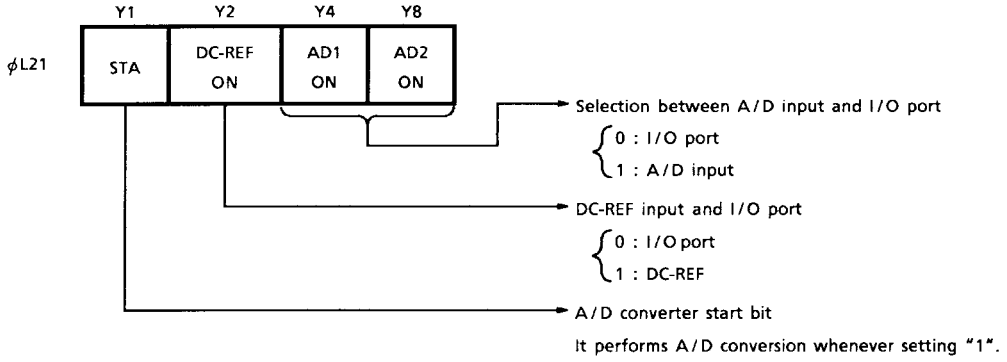
The A/D converter is a 2-channel, 6 bit resolution and usable for measuring field strength and battery voltage.

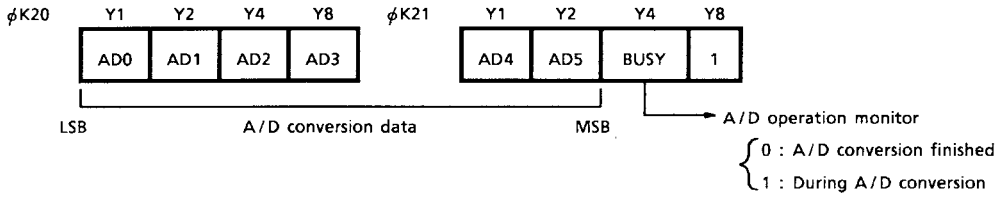
1. A/D Converter Control Port and Data Port



SEL1	SEL0	DC-REF VOLTAGE
0	0	Supply from DC-REF terminal
0	1	V_{DD} (Supply voltage)
1	0	V_{EE} (1.5V constant voltage)
1	1	Inhibit

SEL1	SEL0	A/D INPUT
0	0	AD_{IN1}
0	1	AD_{IN2}
1	0	V_{EE} (1.5V constant voltage)
1	1	Inhibit

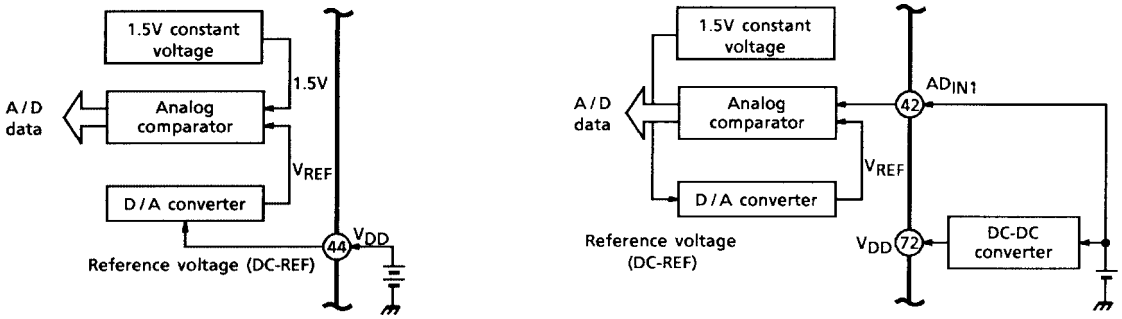




The A/D converter is a 6 bit resolution. The reference voltage of A/D conversion can select the external voltage (DC-REF terminal), supply voltage and 1.5 V constant voltage (V_{EE}). The A/D conversion input is a multiplex method of 2-channel external input terminal (AD_{IN1}, AD_{IN2} terminal) and also switchable to 1.5 V constant voltage (V_{EE}) as well.

Normally field strength and volume level are measured by selecting external voltage or supply voltage as reference voltage and A/D converting the external input level.

The A/D converter can also measure battery and supply voltages. It outputs a battery signal or performes control for backup mode when battery voltage or supply voltage drop. Following is the description as to this method.



(when battery direct driving) **(when battery boosting drive)**

The V_{DD} supply voltage application system has two methods:

- Method to drive directly from battery.
- Method to drive LSI by boosting low voltage battery using DC-DC converter.

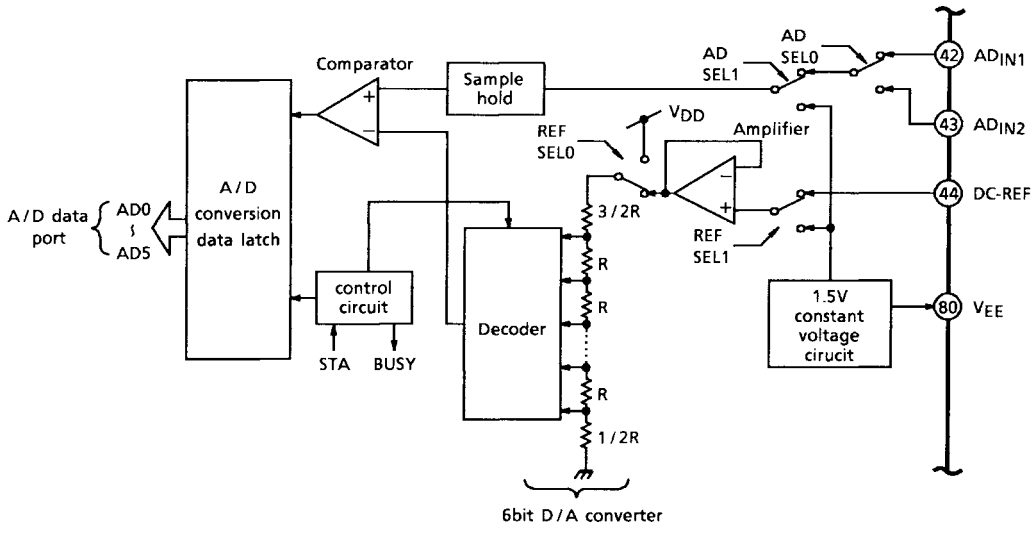
In the case of direct-driving from battery, by setting the reference voltage of A/D converter to supply voltage (V_{DD}) and A/D converting the internal 1.5 V constant voltage, battery voltage is judged. If, for example, A/D converting when V_{DD} = 3 V, the A/D bit data will be about 20H (32) and about 30H (48) when V_{DD} = 2 V.

In case of boosting battery of low voltage, the battery voltage level can be judged by inputting battery voltage (battery voltage at this time must be ≦ 1.5 V) to A/DIN terminal and setting the internal 1.5 V constant voltage (V_{EE}) to reference voltage for A/D conversion. For example, the A/D data when battery voltage = 1.5 V will be about 3FH (63) and about 2BH (43) when 1.0 V.

The A/D converter does A/D conversion whenever setting "1" to STA bit and the conversion will complete after 7 machine cycles (280 μs). Whether A/D conversion is completed can be judged by referring to BUSY bit. After A/D conversion is completed, the data will be loaded into data memory.

These controls are accessed when OUT2/IN2 instruction designated [CN = 0H, 1H] in the operand is executed.

2. A/D Converter Circuit Configuration



The A/D converter consists of: 6 bit D/A converter, comparator, A/D conversion latch, control circuit, A/D data port and 1.5 V constant voltage circuit (supply for LCD driver).

The A/D converter will latch the data to A/D conversion data latch sequentially by means of the 6 bit sequential comparison method.

Note 63: The DC-REF terminal is built-in an amplifier and is high impedance input.

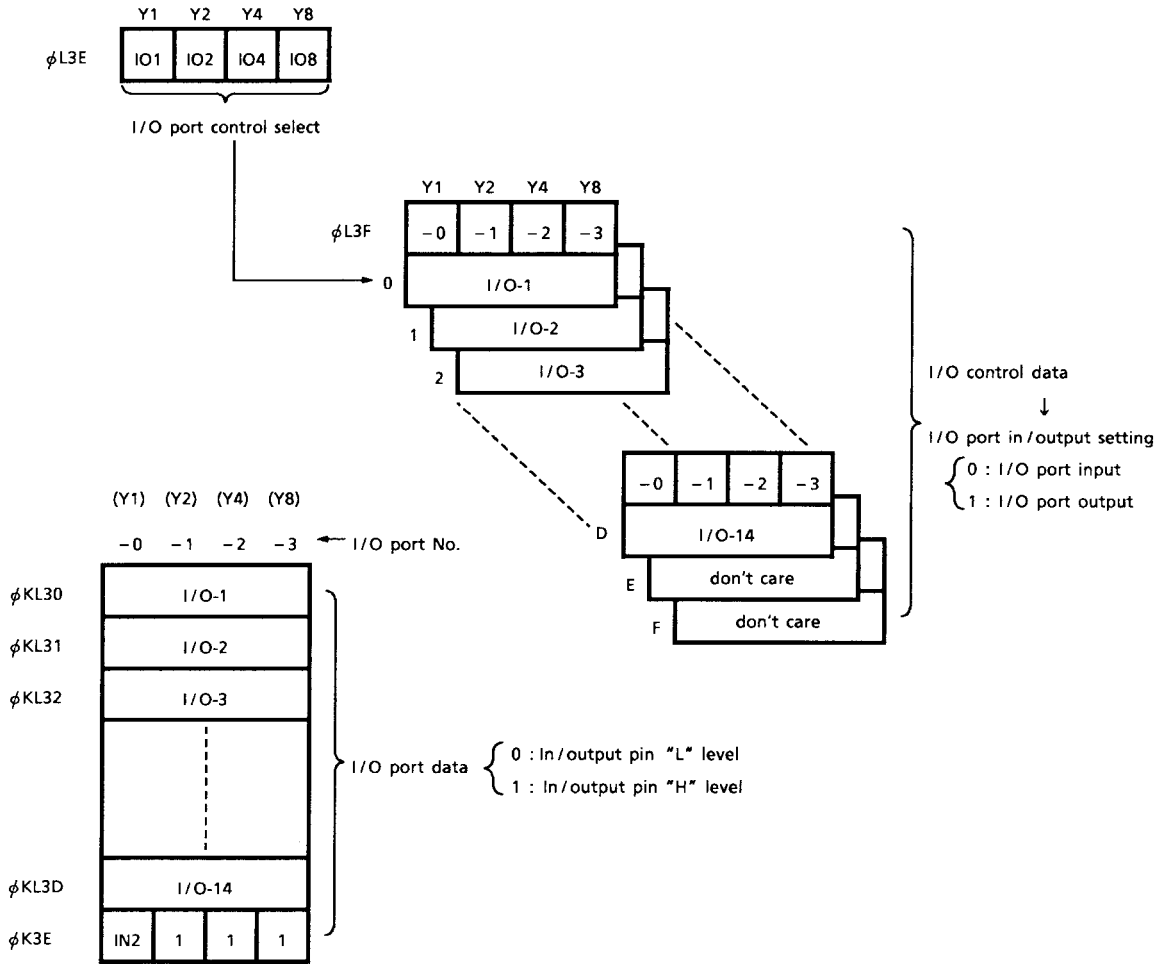
Note 64: During A/D conversion, a proper data is not obtainable even if referring to the A/D conversion data. Therefore, make sure to confirm that the conversion has finished by referring to the A/D operation monitor.

Input/Output Port (I/O port)

The I/O port consists of 56 ports (I/O port-1 to I/O port-14), which are usable as control signal input/output. Within the 56 I/O ports, the I/O port-1, I/O port-2, I/O port-3 and I/O port-7 to I/O port to I/O port-14 combines a key return signal, A/D converter and PWM output, serial interface and buzzer output and LCD driver output, respectively.

The I/O port-7 to I/O port-14 are normally used as LCD driver output.

1. I/O Port Control and I/O Port Data



Note 65: After system reset, the contents of I/O-1 to I/O-6 of the I/O control data will be set to "0" (input port).

Note 66: The I/O-1, I/O-2・・・I/O-14 correspond to the terminal names of P1-0 to 3, P-20 to 3・・・P14-0 to 3, respectively.

Note 67: The S30 terminal will be the input port (IN2) when I/O port switching.

The I/O port in/output will be set by the contents of I/O control data port. If setting to an input port, the bit of I/O control data port corresponding to the port should be set to "0" and "1" if output port.

The I/O control data port is divided by the I/O control select port (ϕL3E). The I/O control data port should be accessed by setting data corresponding to the port you wish to set to I/O control select port. Normally whenever accessing to I/O control data port, the I/O control select data will be +1 incremented. Therefore, the I/O control data will be set successively after "OH" is set to the I/O control select.

When output port setting, the output state of I/O port is controlled when OUT3 instruction corresponding to each I/O port is executed. The contents of data just outputted will be loaded into data memory when IN3 instruction is executed.

When input port setting, the input state of I/O port is controlled when IN3 instruction corresponding to each I/O port is executed. At this time the contents of latch on the output side will never affect the input data.

The I/O port-7 to 14 combines the LCD driver output. In case of using even one terminal of LCD driver for I/O port, it is recommended to use after setting "1" to V_{LCD} OFF bit and connecting V_{LCD} terminal to V_{DD} terminal. (refer to item of LCD driver)

I/O port-1 to 3 combines A/D converter and BUZR output. After system reset, these ports will be set to I/O port. Furthermore, after system reset, I/O port will be set to input port and combination terminal of LCD driver and I/O port will be set to LCD driver output.

In the I/O port-1, when the input state of I/O port designated at input port is changed, execution of WAIT/CKSTP instruction is cancelled and CPU operation is restarted. Likewise, when I/O bit of MUTE port is "1", MUTE bit of MUTE port will forcibly be set to "1" by changing of the input state.

Note 68: In the combined terminal of LCD driver and I/O port, the I/O port input/output and I/O port data will be "don't care" when LCD driver setting.

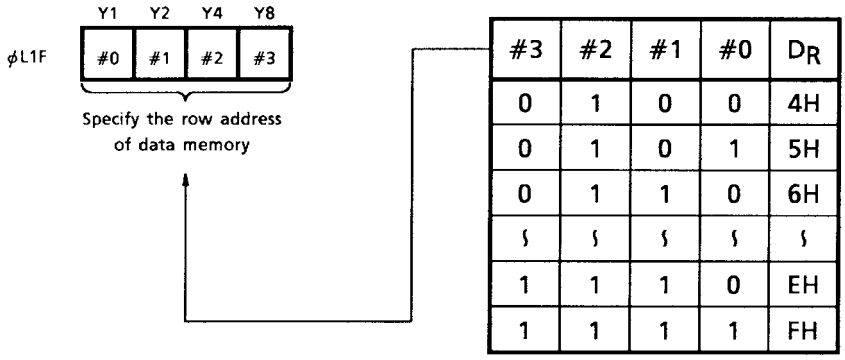
Register Port

The G-register and data register mentioned in the description of CPU are used also as internal ports.

1. G Register (ϕL1F)

It is a register for addressing data memory row addresses (D_R = 4H-FH) when MVGD/MVGS instruction is executed. This register is accessed when OUT1 instruction designated [C_N = FH] in the operand is executed.

Note 69: The contents of this register is valid only when MVGD/MVGS instruction is executed and not valid when other instructions are executed.



#3	#2	#1	#0	D_R
0	1	0	0	4H
0	1	0	1	5H
0	1	1	0	6H
⟆	⟆	⟆	⟆	⟆
1	1	1	0	EH
1	1	1	1	FH

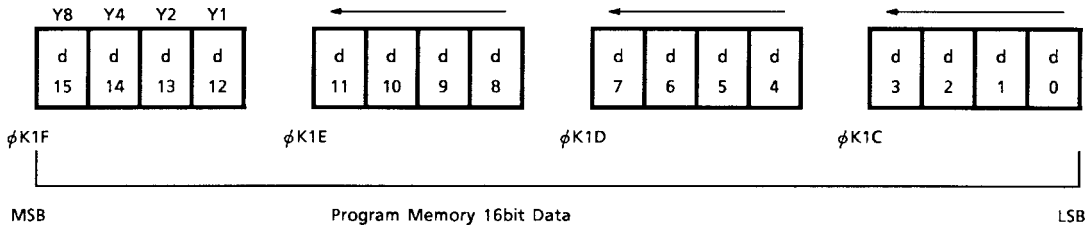
Note 70: Also all the row addresses of data memory can indirectly be specified by setting data 0H to FH to G-register. (D_R = 0H to FH)

2. Data Register (ϕK1C to ϕK1F)

It is a 16 bit register for loading program memory data when DAL instruction is executed.

The contents of this register is loaded into data memory in a unit of 4 bits when IN1 instruction designated [C_N = CH to FH] in the operand is executed.

This register can be used for loading LCD segment decoding operation, radio band egde data and coefficient data at "binary to BCD" conversion, etc.

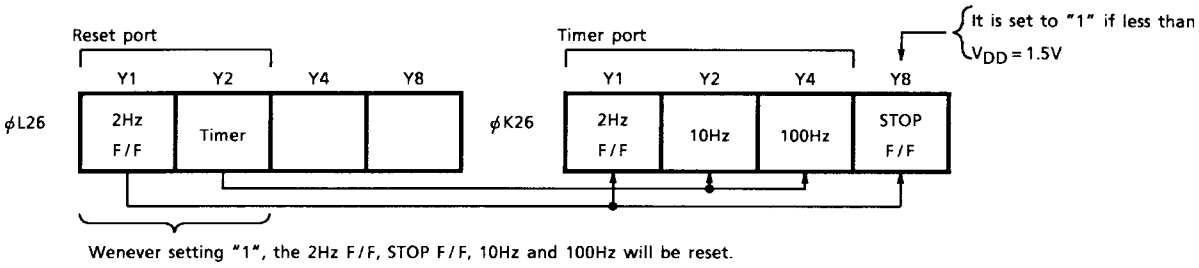


Timer&CPU Stop Function

The timer has 100 Hz, 10 Hz and 2 Hz F/F bits. It is used for counting clock operation and tuning scan mode, etc.

The CPU STOP function is a function to stop CPU by voltage detection circuit when V_{DD} supply voltage drops lower than 1.5 V, in order to prevent CPU miss-operation.

1. Timer Port and STOP F/F Bit

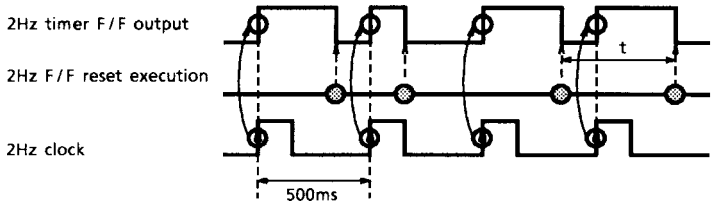


The timer port and STOP F/F bit are accessed when OUT2/IN2 instruction deisgnated [C_N = 6H] in the operand is executed.

2. Timer Port Timing

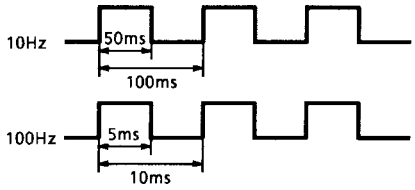
The 2 Hz timer F/F is set by 2 Hz (500 ms) signal. It is reset by setting "1" to 2 Hz F/F of reset port. This bit can normally be used for clock counting.

Since the 2 Hz timer F/F is reset only by 2 Hz F/F of reset port, count error will occur and correct time can not be obtained unless resetting within 500 ms cycles.



$t < 500$ ms

The 10 Hz and 100 Hz timers are outputted to 10 Hz and 100 Hz each by 50% duty pulse of 100 ms and 10 ms cycle. Wenever setting "1" to the timer bit of reset port, a counter lower than 1 kHz will be reset.

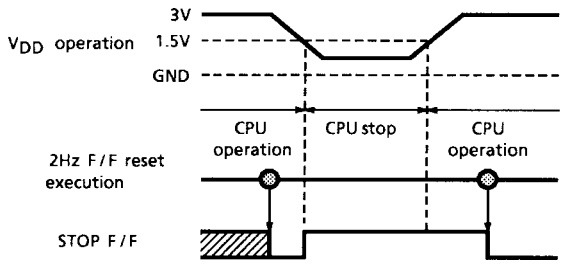


3. CPU Stop Function and STOP F/F Bit

In order to prevent miss-function of CPU operation, the STOP F/F bit is set to "1" when V_{DD} voltage lower than 1.5 V is supplied, and the CPU operation stops. The CPU operation stops program counter at a timing of which voltage lower than 1.5 V is supplied to V_{DD} terminal, and the execution of instruction stops.

If voltage more than 1.5 V is supplied to V_{DD} terminal again, the CPU operation will restart. Since the CPU operation, during this period, is not performed, the clock timing, etc. will be not correct. Whether such condition occurred can be judged by the contents of STOP F/F. Initialization and clock correction should be done as necessary.

The STOP F/F bit will be reset to "0" whenever setting "1" to the 2 Hz F/F of reset port.



Note 71: The contents of timer port and STOP F/F will be reset to "0" after system reset or CKSTP instruction is executed.

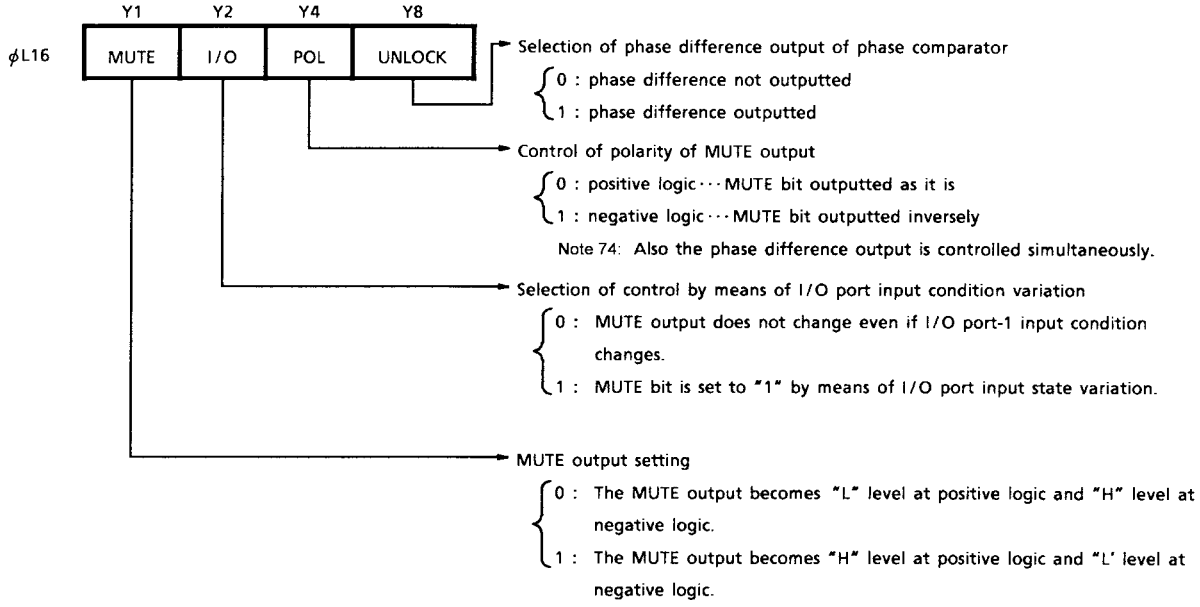
Note 72: When clock stop mode setting, the CKSTP instruction will not be executed if V_{DD} voltage is below 1.5 V. Execute the CKSTP instruction when V_{DD} voltage is above 1.5 V at the timing of radio off, etc.

Note 73: The key scan data just after CPU operation is restarted will be unknown.

MUTE Output

It is a 1 bit CMOS type output port exclusive for muting control.

1. MUTE Port



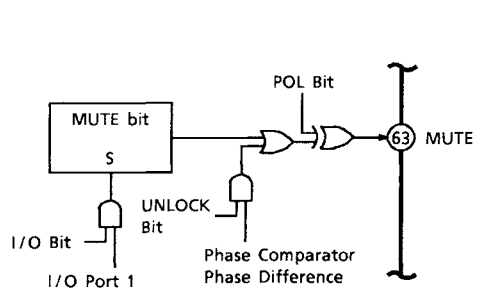
This port is accessed when OUT1 operation designated [C_N = 6H] in the operand is executed. The MUTE output is used for muting control. This has a function to set MUTE bit to "1" at band switching by means of I/O port-1 input, etc.

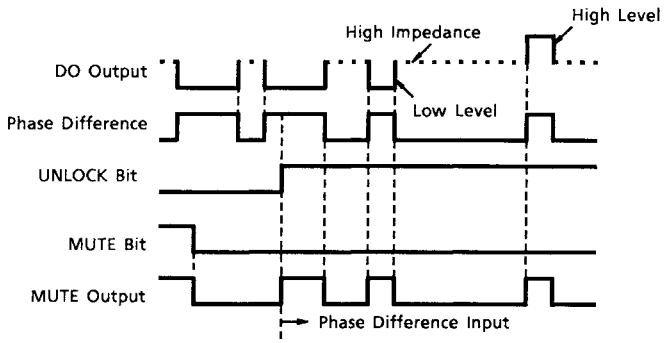
This function is to prevent noises which occur at the time of linear circuit switching, in case of band switching by I/O port-1 input with a slide switch, etc. This control is done by the contents of I/O bit.

The POL bit sets up the MUTE output logic.

The MUTE output is also capable of performing muting control by means of the phase difference output. The unlock state (when PLL system is not in lock state) is outputted as pulse. In this case, with an external low-pass filter this output is used for MUTE output. This selection can be done by UNLOCK bit.

2. MUTE Output Configuration and Timing





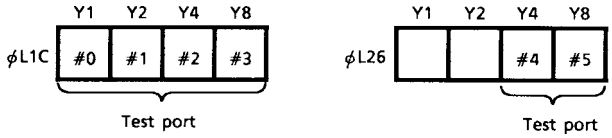
Note 75: When POL bit = "0"

Note 76: When using the phase difference output of phase comparator, MUTE output should be externally affixed with low-pass filter.

Test Port

It is an internal port to test the function of a device.

It is accessed when OUT1 instruction designated [C_N = CH] in the operand and OUT2 instruction designated [C_N = 6H] in the operand are executed. In normal program it should be set to “0”.



Note 77: These contents will be reset to “0” after system reset.

Application for Evaluator Chip

If “H” level is supplied to TEST terminal (test mode), the device will operate as evaluator chip.

Three kinds of the test modes are prepared. The software development tool is configured by means of three devices.

By connecting this software development tool to a tuner IC, confirming the radio operation while proceeding software development can be done.

As to the development tool specifications, please refer to the specifications of TC9317F software development tool.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 to 4.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	400	mW
Operating temperature	T_{opr}	−10 to 60	°C
Storage temperature	T_{stg}	−55 to 125	°C

Electrical Characteristics (unless otherwise noted, Ta = –25°C, V_{DD} = 3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Range of operating supply voltage	V_{DD}	—	*	1.8	3.0	3.6	V
Range of memory retention voltage	V_{HD}	—	Crystal ocillation stopped * (CKSTP instruction executed)	1.0	—	3.6	V
Operating current	I_{DD1}	—	Under ordinary operation and PLL on operation, no output load	—	0.5	1.5	mA
Memory retention current	I_{DD2}	—	CPU only operating (PLL off, display lit)	—	50	100	μA
	I_{DD3}	—	In stand-by mode (PLL off, crystal oscillator only)	—	10	20	
	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	1.0	
Crystal oscillation frequency	f_{XT}	—	*	—	75	—	kHz
Crystal oscillation startup time	t_{ST}	—	Crystal oscillation f_{XT} = 75 kHz	—	—	1.0	s

Note 78: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 to 3.6 V, Ta = 10 to 60°C.

Voltage Doubler Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Voltage doubler reference voltage	V_{EE}	—	GND reference (V_{EE})	1.3	1.5	1.7	V
Constant voltage temperature characteristics	D_V	—	GND reference (V_{EE})	—	−5	—	mV/°C
Voltage doubler boosting voltage	V_{LCD}	—	GND reference (V_{LCD})	2.6	3.0	3.4	V

Operating Frequency Ranges for Programmable Counter and if Counter

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
FM_{IN}	f_{FM}	—	Sine wave input when V_{IN} = 0.2 Vp-p	*	0.5	—	2.5	MHz
AM_{IN}	f_{AM}	—	Sine wave input when V_{IN} = 0.2 Vp-p	*	0.5	—	12	MHz
IF_{IN}	f_{IF}	—	Sine wave input when V_{IN} = 0.2 Vp-p	*	0.35	—	12	MHz
Input amplitude	V_{IN}	—	FM_{IN}, AM_{IN}, IF_{IN} input	*	0.2	—	V_{DD} − 0.5	V_{p-p}
FM_{IN}-PSC transmission delay time	tpd	—	PSC	*	—	—	400	ns

Note 78: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 to 3.6 V, Ta = 10 to 60°C.

LCD Common Output/Segment Output, General-Purpose I/O Ports (COM1/P7-0 to COM3/P7-2, S1/P7-3 to S30/IN2)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{LCD} = 3 V, V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL1}	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	300	600	—	
Output voltage 1/2 level		V_{BS}	—	No load	1.3	1.5	1.7	V
Input leak current		I_{LI}	—	V_{IH} = V_{LCD}, V_{IL} = 0 V (when I/O port or IN port)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH2}	—	(when I/O port or IN port)	V_{LCD} × 0.6	—	V_{LCD}	V
	"L" level	V_{IL2}	—	(when I/O port or IN port)	0	—	V_{LCD} × 0.1	

I/O Port 1 (P1-0/KR_{12} to P1-3/KR_{15})

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH2}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL2}	—	V_{OL} = 0.3 V	300	600	—	
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V (when I/O port)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH2}	—	(when I/O port)	2.4	—	3.0	V
	"L" level	V_{IL2}	—	(when I/O port)	0	—	0.6	
N-ch/P-ch load resistance		R_{ON}	—	V_{OL} = 3.0 V, V_{OH} = 0 V (when key return output)	50	100	200	kΩ

$\overline{HOLD}$ Input Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH3}	—	—	2.4	—	3.0	V
	"L" level	V_{IL3}	—	—	0	—	1.2	

A/D Converter (A/D_{IN1}, A/D_{IN2}, DC-REF)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	V_{AD}	—	AD_{IN1}, AD_{IN2}	0	—	V_{DD}	V
Analog reference voltage range	V_{REF}	—	DC-REF, V_{DD} = 2.0 to 3.6 V	1.0	—	$V_{DD} \times 0.9$	V
Resolution	V_{RES}	—	—	—	6	—	bit
Conversion total error	—	—	V_{DD} = 2.0 to 3.6 V	—	±1.0	±4.0	LSB
Analog input leak	I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V (AD_{IN1}, AD_{IN2}, DC-REF)	—	—	±1.0	μA

Key Input Ports (K0 to K3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Key input voltage range		V_{KI}	—	—	0	—	V_{DD}	V
A/D conversion resolution		V_{RES}	—	—	—	3	—	bit
A/D conversion combined error		—	—	V_{DD} = 1.8 to 2.0 V	—	—	±1.5	LSB
				V_{DD} = 2.0 to 3.6 V	—	—	±0.5	
N-ch/P-ch input resistance		R_{IN1}	—	—	50	100	200	kΩ
Output current	"H" level	V_{IH1}	—	When WAIT instruction released	1.8	—	3.0	V
	"L" level	V_{IL1}	—	When WAIT instruction released	0	—	0.3	
Input leak current		I_{LI}	—	When input resistance OFF, V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA

DO1/OT, DO2 Output; MUTE, PSC Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	300	600	—	
Output off leak current		I_{TL}	—	V_{TLH} = 3.0 V, V_{TLL} = 0 V (DO1, DO2)	—	—	±100	nA

General-Purpose I/O Ports (P2-0 to P6-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−300	−600	—	μA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	300	600	—	
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH2}	—	—	2.4	—	3.0	V
	"L" level	V_{IL2}	—	—	0	—	0.6	

IN1/SCIN, $\overline{\text{RESET}}$ Input Port

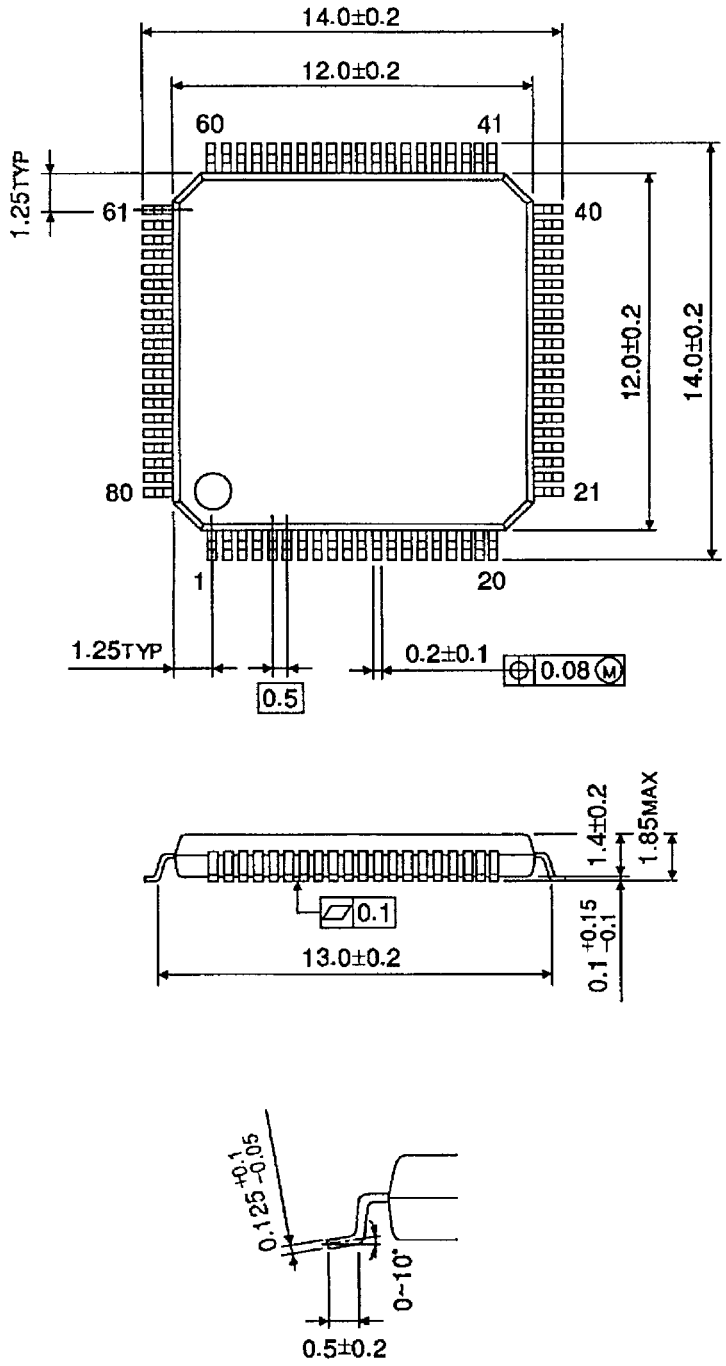
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V (excluding SC_{IN} input)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH2}	—	—	2.4	—	3.0	V
	"L" level	V_{IL2}	—	—	0	—	0.6	

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	R_{IN2}	—	(TEST)	15	30	60	kΩ
X_{IN} amp feedback resistance	R_{fXT}	—	(X_{IN}-X_{OUT})	—	20	—	MΩ
X_{OUT} output resistance	R_{OUT}	—	(X_{OUT})	—	4	—	kΩ
Input amp feedback resistance	R_{fIN1}	—	(FM_{IN}, AM_{IN}, IF_{IN}/SC_{IN})	500	1000	2000	kΩ
Voltage used to detect supply voltage drop	V_{STP}	—	(V_{DD})	1.35	1.5	1.6	V
Supply voltage drop detection temperature characteristics	D_S	—	(V_{DD})	—	−3	—	mV/°C

Package Dimensions

LQFP80-P-1212-0.50A Unit : mm



Weight: 0.45 g (typ.)

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