

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

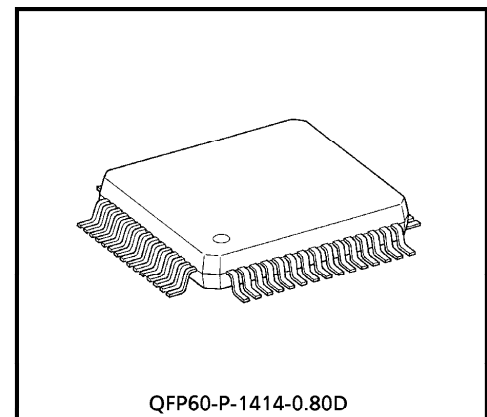
TC9321F**SINGLE CHIP DTS MICROCONTROLLER (DTS-10)**

The TC9321F is a 4bit CMOS microcontroller for single chip digital tuning system with built-in prescaler, PLL. The CPU has 4bit parallel addition/subtraction (AI, SI instructions, etc.) logical operation (OR, AN instructions, etc.) multiple bits judgment, comparison instructions (TM, SL instructions, etc.) and time base functions.

The TC9321F is housed in as pin 60 mini-flat package and is provided with ample I/O ports and exclusive key input ports which are controlled by powerful I/O instructions (IO, KEY instruction, etc.) and output ports.

In addition, the TC9321F has built-in 2 modulus prescaler, PLL circuit, and IF counter that counts intermediate frequency (IF) in FM and AM bands for detecting broadcasting stations.

Furthermore, the TC9321F has built in serial bus control function (SIO instruction) to powerfully control peripheral ICs, 6bit A/D converter and D/A converter that are usable for field strength measurement and electronic volume control, and provides with many functions needed for digital tuning system.



QFP60-P-1414-0.80D

Weight : 1.10g (Typ.)

FEATURES

- 4bit microcontroller single chip digital tuning system.
- $5V \pm 10\%$ single power supply, CMOS structure for low power dissipation.
- Built-in prescaler (Max. 140MHz signal is directly input in FM band), PLL.
- Easy back up of data memory (RAM) and various ports (by the $\overline{\text{INH}}$ terminal).
- Program memory (ROM) : 16bits \times 3968 steps
- Data memory (RAM) : 4bits \times 256 words
- 61 kinds of powerful instructions sets (all single word instructions).
- Instruction execution time 11.1 μ s (7.2MHz crystal connection).
- Abundant add and subtract instructions (Add instruction : 12, subtract instruction : 12)

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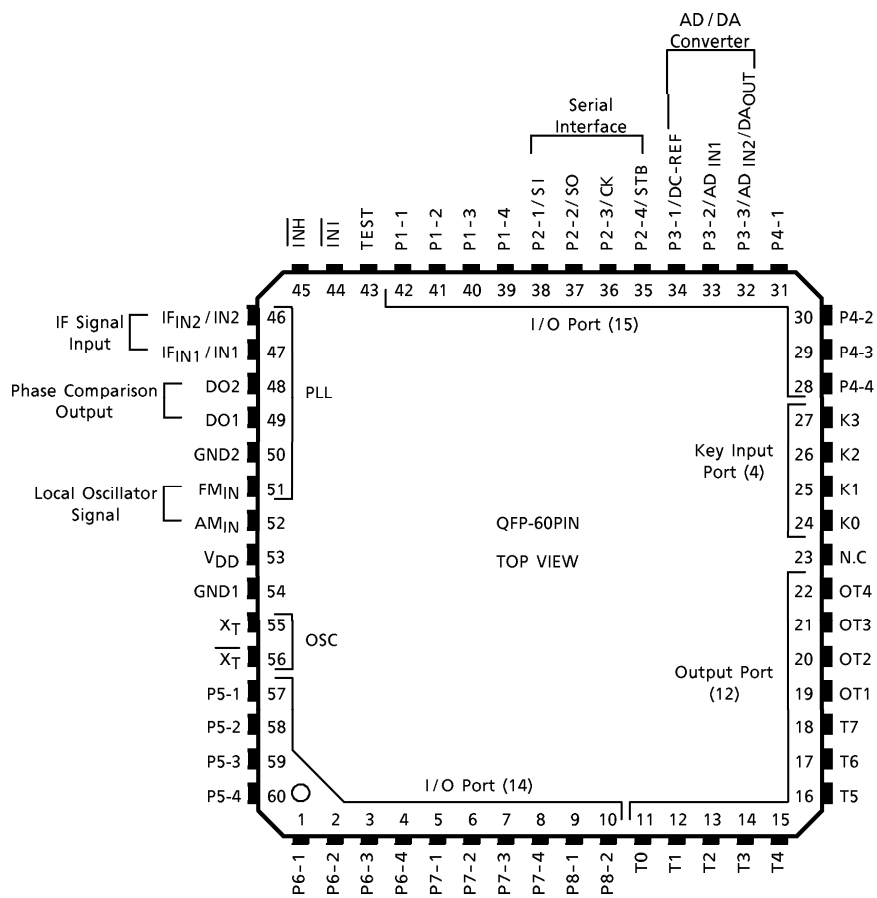
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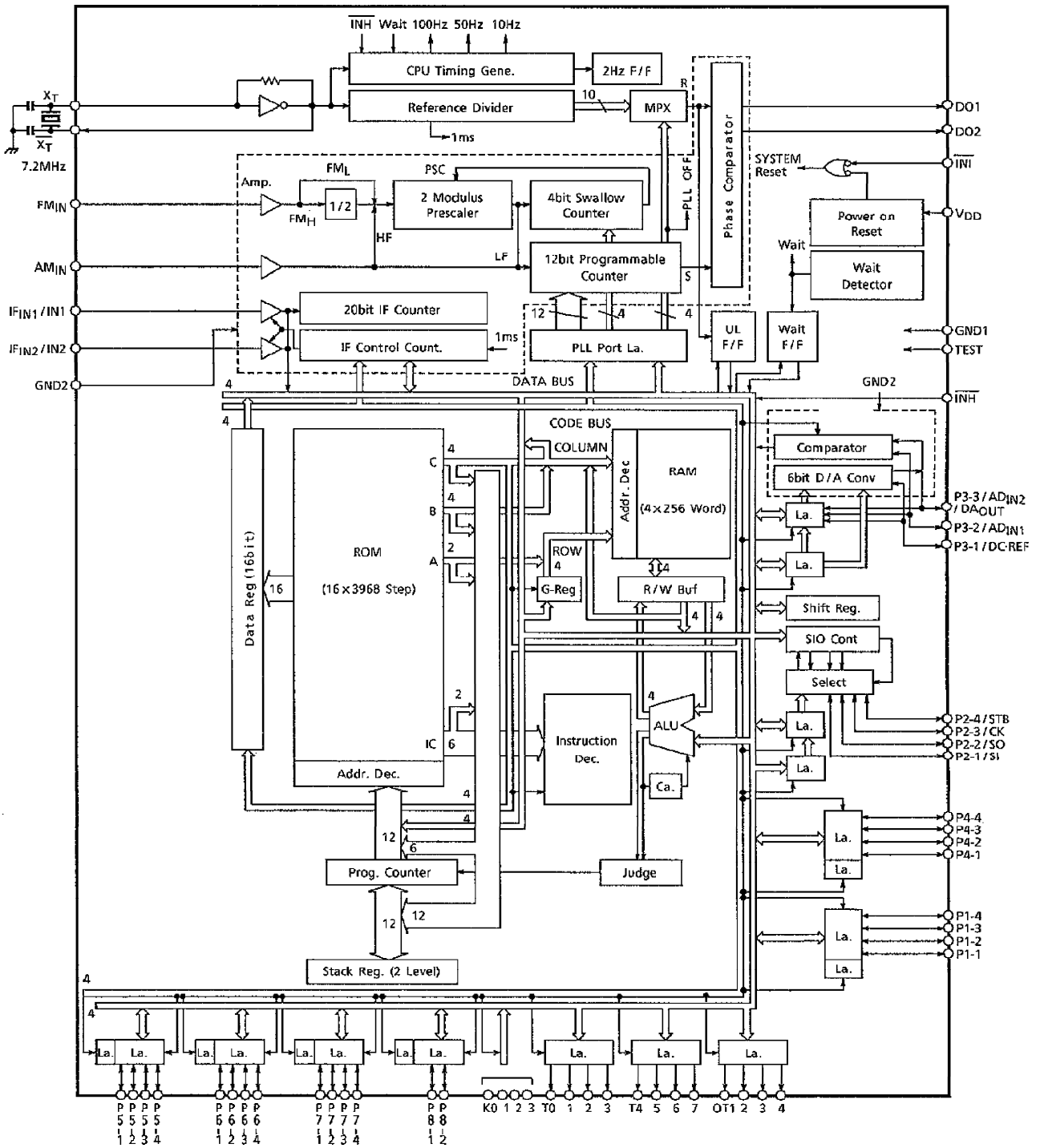
● The information contained herein is subject to change without notice.

- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF instructions, etc.)
- Data transfer at the same row address is possible.
- Register indirect transfer is possible (MVGD, MVGS instructions)
- Powerful 16 general registers (arranged in RAM)
- Stack level : 2 levels
- Program memory (ROM) has no conception of page and field, and JUMP and CAL instructions can be freely contained in 3968 steps.
Further, contents of 16bits data at any address in 1024 steps can be freely referred (DAL instruction)
- Built-in 20bit general-use IF counter (IF_{IN1}, IF_{IN2})
- Independent frequency input terminals for FM and AM (FM_{IN}, AM_{IN}), 2 phase comparator outputs (DO1, DO2)
- 10 reference frequencies are programmable selectable (1, 3.125, 5, 6.25, 9, 10, 12.5, 25, 50, 100kHz)
- Pulse swallow system and direct frequency division system are selectable by program according to receiving frequency band.
- IF correction at FM band is possible (Internal port for IF offset)
- Built-in powerful serial bus control function (I/O port-2 terminals are programmatically selectable.)
- Powerful I/O instructions (IO, KEY, SIO instruction, etc.)
- Exclusive key input port (K0~K3)
- IF counter inputs (IF_{IN1}, IF_{IN2}) and input ports (IN1, IN2) are programmatically selectable.
- Max. 44 I/O ports (I/O settable ports : 29, output ports : 12, input ports : max. 7)
- Clock stop is possible programmatically (at CKSP instruction : supply current below 10 μ A)
- Built-in 2Hz timer F/F, 10/100Hz internal pulse output (Internal port for time base)
- Locked state of PLL is detectable (Internal port for PLL lock detection)
- Built-in 6bit A/D and D/A converters (Selectable by selecting I/O port-3 terminals (P3-1~P3-3) programmatically).
- OTP product : TC93P21F

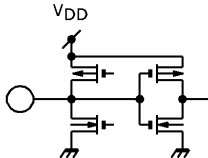
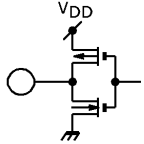
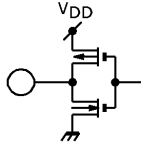
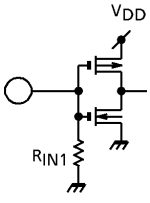
PIN CONNECTION

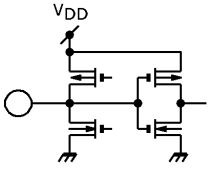
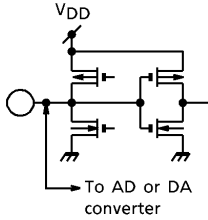


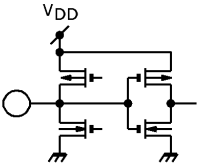
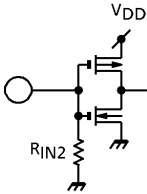
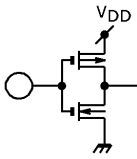
BLOCK DIAGRAM

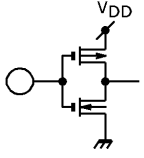
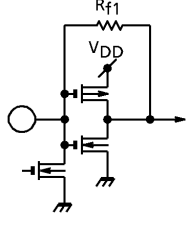
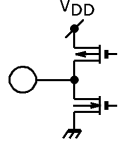


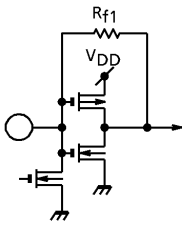
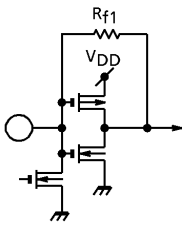
PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
57~60 1~4 5~8 9~10	P5-1~P5-4 P6-1~P6-4 P7-1~P7-4 P8-1~P8-2	I/O Port 5 I/O Port 6 I/O Port 7 I/O Port 8	4bit × 3 (P5-1~P7-3) and 2bit (P8-1~P8-2) I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal ports called PORT-5~PORT-8 I/O CONTROL. (Refer Notes 1, 2 and 3.)	
11~18	T0~T7	Key Timing Output Port	4bit (T0~T3) and 4bit (T4~T7) output terminals. These ports are normally used for key return timing signal output of key matrix. (Refer to Notes 2 and 3.)	
19~22	OT1~OT4	General-Purpose Output Port	4bit output ports. (Refer to Notes 2 and 3.)	
23	N.C	No Connection	As this terminal is not connected to internal chip, it can be left open or connected to GND or VDD freely. In case of OTP product TC93P21F, this terminal serves as V _{p-p} terminal and TC93P21F is readily usable when connected to VDD.	—
24~27	K0~K3	Key Input Port	4bit input ports for key matrix input. When KEY instruction these ports specified in the operand is executed, data of these terminals are read in RAM. ALL terminals have built-in pull-down resistors. Further, the output ports T0~T7 are normally used for key return timing signal.	

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
28~31 39~42	P4-4~P4-1 P1-4~P1-1	I/O Port 4 I/O Port 1	4bit (P4-1~P4-4) and 4bit (P1-1~P1-4) I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal ports called PORT-4~PORT-1 I/O CONTROL. (Refer Notes 1, 2 and 3.)	
32 33 34	P3-3 /ADIN2 /DAOUT P3-2 /ADIN1 P3-1 /DC-REF	I/O Port 3 /AD Analog Voltage Input /DA Analog Voltage Output /AD Analog Voltage Input /Reference Voltage Input	3bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-3 I/O CONTROL. Further, these terminals also serve for the analog input of the built-in 2-channel A/D converter and analog output of 1-channel D/A converter. A/D and D/A converter input/output selection is controlled according to contents of ADON, DAON, ADSEL bit. The built-in A/D converter is of programmably sequential comparison type, and P3-1 is the reference voltage input, P3-2 is the analog comparison voltage input, and P3-3 is the analog comparison voltage input or analog voltage output. (Note) A ladder resistance that generates internal D/A reference voltage is used commonly by the A/D and D/A converters. When both the A/D and D/A converters are used simultaneously, DAON bit is set to "0" and D/A output is made to high impedance at time of A/D conversion. It is therefore necessary to hold potential with a capacitor, etc. (Refer to Notes 1, 2 and 3.)	

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
35~38	P2-4 / STB P2-3 / CK P2-2 / SO P2-1 / SI	I/O Port 2 / Strobe Pulse Output / Serial Clock Output / Serial Data Output / Serial Data Input	4bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-2 I/O CONTROL. Further, these terminals are also used as the serial interface (SIO). Selection of SIO is controlled according to contents of SIO ON bit and in case of these serial interface, peripheral optional ICs can be controlled by executing SIO command. Serial transfer in \overline{NCD} / NCD mode is programmably selectable. When selectable NCD mode, P2-4 / STB and P2-1 / SI pins are used as P2-4, P2-1 I/O port. (Refer to Notes 1, 2 and 3.)	
43	TEST	Test Mode Control Input	Test mode control input terminal. The device is put in the test mode when "H" level signal is input and becomes the normal operating state when "L" level signal is input or in NC state. (A pull-down resistor has been built-in.)	
44	\overline{INI}	Initialize Input	Device system reset signal input terminal. As long as the \overline{INI} terminal is kept at "L" level, a system is kept in the reset state and when it becomes "H" level, a program starts from address 0. Normally, the system is reset when 0~3.5V is supplied to the V_{DD} terminal (Power ON Reset) and therefore, this terminal is used by fixing at "H" level. (Note) After the system reset, I/O ports are set in the input mode. However, the output state of output ports is indefinite and it is necessary to initialize them by program.	

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
45	$\overline{\text{INH}}$	Inhibit Input Terminal	<p>This is the $\overline{\text{INH}}$ port input terminal. Normally, this terminal is used for radio mode selecting signal input or battery detection signal input.</p> <p>When CKSTP instruction is used in a program and this CKSTP instruction is executed while the $\overline{\text{INH}}$ terminal is at "L" level, it is possible to stop the internal clock generator and CPU operation and put a system in the memory backup state with low current consumption (below $10\mu\text{A}$).</p> <p>(Note) CKSTP instruction is effective when the $\overline{\text{INH}}$ terminal is at "L" level and when this instruction is executed at "H" level, the same operation as NOOP instruction results.</p> <p>(Note) In the radio OFF mode or back-up mode, it is necessary to set reference internal ports (4 bits) at all "1" (PLL OFF mode).</p>	
46 47	IFIN2 / IN2 IFIN1 / IN1	IF Signal Input 2 / Input port 2 IF Signal Input 1 / Input port 1	<p>IF signal input terminal of IF counter that detects auto stop by counting IF signal in FM and AM bands. Input frequency range is 0.1~20MHz (0.3V_{p-p} min.)</p> <p>Having a built-in input amplifier, operates at small amplitude in C-connection.</p> <p>These terminals are usable programmably as input ports, and are selectable according to contents of the IN CONTROL Port.</p> <p>(Note) When IF counter is used, reference internal ports (4 bits) are set at all "1" or inputs that are not selected by IFIN1 bit (input selecting bit) are pulled down.</p> <p>(Refer to Note 1)</p>	
48 49	DO2 DO1	Phase Comparator Output	<p>PLL phase comparator output terminal Tri-state output.</p> <p>If divided output signal from the programmable counter is higher than reference frequency, "H" level signal is output and if it is lower, "L" level signal is output and if matched, it becomes high impedance.</p> <p>Signals from DO1 and DO2 are parallelly output.</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
50	GND2	Analog GND Terminal	GND terminal only for PLL, IF counter and AD/DA converter analog units.	—
51	FM _{IN}	FM Band Signal Input	<p>Programmable counter input terminal for FM band.</p> <p>The 1/2 + pulse swallow system (FM_H mode) and the pulse swallow system (FM_L mode) are selectable by PLL instruction.</p> <p>In case of the pulse swallow system, local oscillation output (VCO output) of 30~140MHz (0.3V_{p-p} min.) is input and in case of 1/2 prescaler input, 30~185MHz (0.5V_{p-p} min.) is input.</p> <p>Having a built-in input amplifier, operates at small amplitude with a capacitor connected.</p> <p>(Note) When reference internal ports (4 bits) are set at all "1" or LF mode or HF mode is set, this input is pulled down.</p>	
52	AM _{IN}	AM Band Signal Input	<p>Programmable counter input terminal for AM band.</p> <p>The direct dividing system (LF mode) and the swallow system (HF mode) are freely selectable by PLL instruction.</p> <p>In case of the direct dividing system (LF mode), local oscillation output (VCO output) of 0.5~20MHz (0.3V_{p-p} min.) and in case of the pulse swallow system, 1~40MHz (0.3V_{p-p} min.) is input.</p> <p>Having a built-in input amplifier, operates at small amplitude with a capacitor connected.</p> <p>(Note) When reference internal ports (4 bits) are set at all "1" or FM_H Mode or FM_L Mode is set, this input is pulled down.</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION / OPERATION	REMARKS
53	V _{DD}	Power Supply Terminal	<p>Power supply terminal. At time of PLL operation, 5V ± 10% is applied. In the back-up state (when executing CKSTP instruction), voltage can be reduced to 2V. Further, when voltage drops below 3.5V during the operation of CPU, CPU stops (CPU Wait Mode) to prevent malfunction it restarts when voltage increases above 3.5V. As (Wait Mode) resulted under this condition can be detected by Wait F/F bit, perform initialization, clock correction, etc. programmatically. Further, when 0 to 3.5V is applied to this terminal, a device is reset and a program starts from address 0 (Power On Reset). (Note) Rise time of supply voltage on a device shall be 10~100ms for the power ON reset operation. (Refer to Note 1)</p>	—
54	GND1	Digital GND Terminal	GND terminal for CPU and the logic unit.	—
55 56	X _T $\overline{X_T}$	Crystal Oscillation Terminal	<p>Crystal resonator connecting terminal. Connect a 7.2MHz crystal to this terminal. Adjust oscillation frequency (7.2MHz) while observing LCD segment waveform. When CKSTP instruction is executed, oscillation stops automatically.</p>	

- (Note 1) When a device is reset (V_{DD} = 0 → 3.5V and \overline{INI} = "L" → "H"), I/O ports are set to the input, terminals serving as I/O ports and AD/DA converters are to the input of I/O ports, terminals serving as I/O ports and serial I/O ports are set to the input of I/O ports, and terminals serving as IF counter input and input port are set to IF counter input.
- (Note 2) When CKSTP instruction is executed, outputs of the output ports and I/O ports are all set at "L" level.
- (Note 3) When a device is reset, contents of output ports and internal ports are indefinite and it is therefore necessary to initialize them programmatically.

OPERATIONAL DESCRIPTION

○ CPU

The CPU consists of a program counter, stack register, ALU, program memory, data memory, G-register, data register, carry F/F, and judge circuit.

1. Program counter (PC)

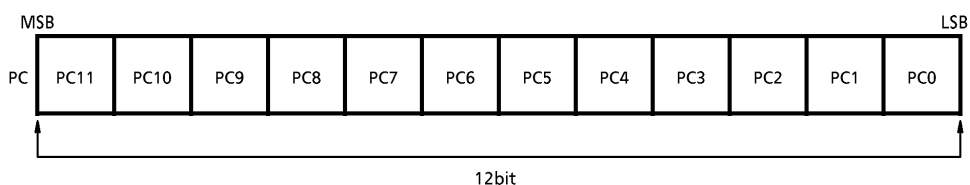
The program counter is a counter for addressing program memory (ROM) and consists of a 12bit binary up counter.

This counter is cleared by system resetting and a program starts from address 0.

Normally, whenever one instruction is executed, the count value is incremented by one.

When JUMP instruction or CAL instruction is executed, the address designated in the operand of that instruction is loaded.

Further, when an instruction having the skip function (AIS, SLT, TMT, RNS instructions, etc.) is executed and the result is a condition to be skipped, the program counter is incremented by two and skips next instruction.



2. Stack register (STACK)

This is a register consisting of 2×12 bits and a value of the program content + 1, that is, return address is stored in this register when the subroutine call instruction is executed.

The content of the stack register is loaded on the program counter when a return instruction (RN, RNS instruction) is executed.

The stack register has 2 stack levels and nesting is 2 levels.

3. ALU

The ALU has the binary 4bit parallel addition and subtraction, logical operation, comparison and multiple bit judging functions.

Further, this CPU has no accumulator and contents of the data memory are directly treated in all operation.

4. Program memory (ROM)

The program memory, consisting of 16 bits×3968 steps, stores programs.

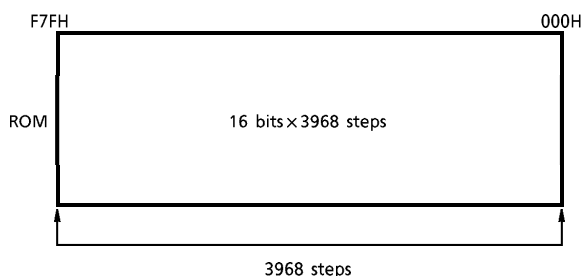
Usable address range is 3968 steps from address 000H to address F7FH.

The program memory has no concept of page and field, and JUMP and CAL instructions are freely usable in 3968 steps.

Further, it is possible to use any address of the program memory as data area and to load its contents in 16 bits in the data register by executing DAL instructions.

(Note) Data area in the program memory shall be provided at address outside the program loop.

(Note) Address in the program memory designatable as data area at time of DAL instruction execution is within 1024 steps from 000H to 3FFH.



5. Data memory (RAM)

The data memory consists of 4 bits×256 words and is used for data storage.

These 256 words are expressed by row address (4 bits) and column address (4 bits).

192 word (row address=4H~FH) in the data memory are indirectly addressed by G-register.

Therefore, when data in this area are processed, it is necessary to perform the processing after designating row address in advance with G-register.

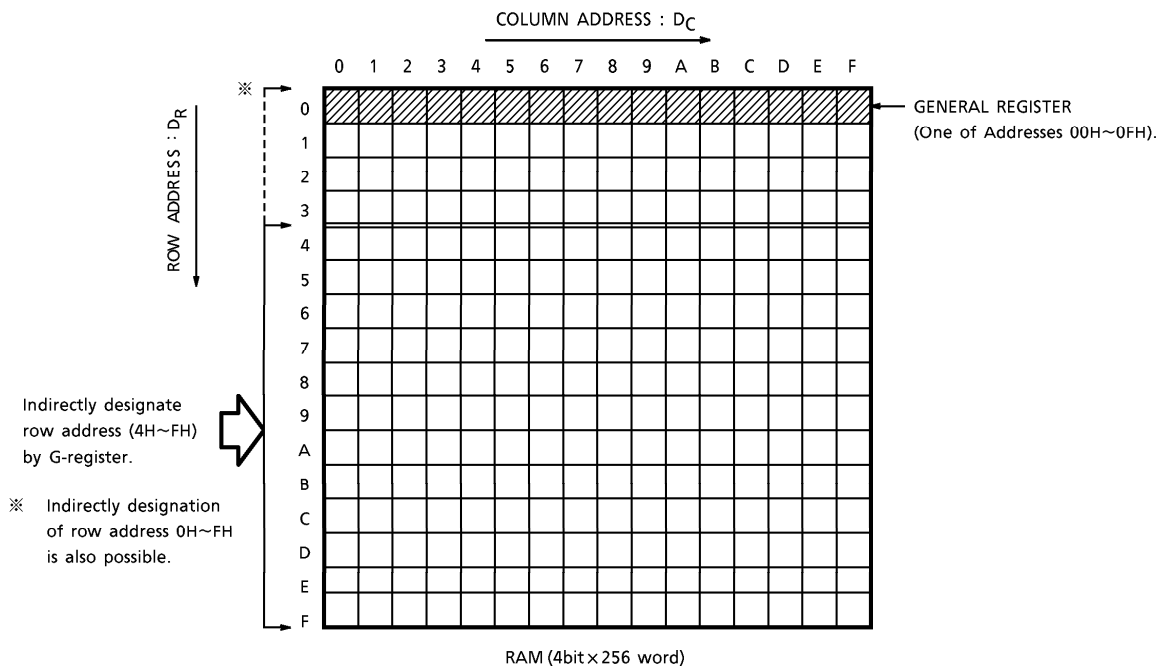
Further, address 00H~0FH in the data memory are called the general register and usable only by designating column address (4 bits).

These 16 general registers can be used for operation and transfer with the data memory.

In addition, it is also possible to use them as ordinary data memories.

(Note) Column address (4 bits) designating a general register becomes Register No. of that general register.

(Note) It is also possible to indirectly designate all row addresses (0H~BH) by G-register.



6. G-register (G-REG)

The G-register is a 4 bits register for addressing row addresses ($D_R = 4 \sim FH$) of 192 words of the data memory.

Contents of this register becomes effective when MVGD / MVGS instruction is executed and have nothing to do with execution of other instructions.

This register is treated as one of ports and its contents are set when IO instruction is executed.

(Refer to Item 1 of Register Ports.)

7. Data register (DATA REG)

This register consists of 1×16 bits and 16bit data of any address 000H~3FFH of the program memory is loaded when DAL instruction is executed.

This register is treated as one of ports and its contents are read in 4 bits unit into the data memory when KEY instruction out of I/O instructions is executed.

(Refer to Item 2 of Register Ports.)

8. Carry F/F (C.F / F)

This carry F/F is set when carry or borrow was generated as a result of execution of the calculation instruction and is reset when there is no carry nor borrow.

Contents of the carry F/F change only when the addition / subtraction instruction was executed and remain unchanged when other instructions were executed.

9. Judge circuit (J)

When any instruction having a skip function was executed, this circuit judges that skip condition. If the skip condition was satisfied, the program counter is incremented by two and skips a following instruction.

There are 29 instructions having the skip function.

(Refer to instructions with the *mark on the List of Function and Operation of in Item 11)

10. List of instructions sets

Total 61 instruction sets are available and they are all one word instruction.

These instruction are expressed in 6 bits instruction code.

HIGH ORDER 2 BITS LOW ORDER 4 BITS		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	CALL ADDR ₁	SLTI M, I
0001	1	AIS M, I	ADS r, M		SGEI M, I
0010	2	AIN M, I	ADN r, M		SEQI M, I
0011	3	SI M, I	SU r, M		SNEI M, I
0100	4	SIS M, I	SUS r, M	MVSR M ₁ , M ₂	JUMP ADDR ₁
0101	5	SIN M, I	SUN r, M	MVIM M, I	
0110	6	LD r, M	ORR r, M	MVGD r, M	
0111	7	ST M, r	ANDR r, M	MVGS M, r	
1000	8	AIC M, I	AC r, M	PLL M, C	TMTR r, M
1001	9	AICS M, I	ACS r, M	SEG M, C	TMFR r, M
1010	A	AICN M, I	ACN r, M	MARK M, C	TMT M, N
1011	B	SIB M, I	SB r, M	IO M, C	TMF M, N
1100	C	SIBS M, I	SBS r, M	KEY M, C	TMTN M, N
1101	D	SIBN M, I	SBN r, M	SIO M, C	TMFN M, N
1110	E	SEQ r, M	ORIM M, I	XORIM M, I	DAL ADDR ₂ , r
1111	F	SNE r, M	ANIM M, I	XORR r, M	RN, RNS, CKSTP, NOOP

11. List of functions and operation of instructions

(Explanation of symbols on list)

M	: Data Memory Address Usually, one of data memory addresses 00H~3FH
r	: General Register One of data memory addresses 00H~0FH
PC	: Program Counter (12 bits)
STACK	: Stack Register (12 bits)
G	: G-Register (4 bits)
DATA	: Data Register (16 bits)
I	: Immediate Data (4 bits)
N	: Bit Position (4 bits)
—	: All "0"
C	: Port Code No. (4 bits)
C _N	: Low order 3 bits of Port Code No.
R _N	: General Register No. (4 bits)
ADDR ₁	: Program Memory Address (12 bits)
ADDR ₂	: High order 6 bits of Program Memory Address in Page 0.
Ca	: Carry
b	: Borrow
PLL	: Port treated by execution of PLL instruction
SEG	: Port treated by execution of SEG instruction
MARK	: Port treated by execution of MARK instruction
IO	: Port treated by execution of IO instruction
KEY	: Port treated by execution of KEY instruction
SIO	: Port treated by execution of SIO instruction
()	: Contents of register or data memory
[] _C	: Contents of port shown by Code No. C (4 bits)
[]	: Contents of Data Memory shown by contents of Register or Data Memory
[] _p	: Contents of Program Memory (16 bits)
IC	: Instruction Code (6 bits)
*	: Instruction with skip function
D _C	: Data Memory Column Address (4 bits)
D _R	: Data Memory Row Address (2 bits)

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)			
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)
ADDITION INSTRUCTION	AI M, I		Add immediate data to memory	$M \leftarrow (M) + I$	000000	D _R	D _C	I
	AIS M, I	*	Add immediate data to memory, then skip if carry	$M \leftarrow (M) + I$ Skip if carry	000001	D _R	D _C	I
	AIN M, I	*	Add immediate data to memory, then skip if not carry	$M \leftarrow (M) + I$ Skip if not carry	000010	D _R	D _C	I
	AIC M, I		Add immediate data to memory with carry	$M \leftarrow (M) + I + ca$	001000	D _R	D _C	I
	AICS M, I	*	Add immediate data to memory with carry, then skip if carry	$M \leftarrow (M) + I + ca$ Skip if carry	001001	D _R	D _C	I
	AICN M, I	*	Add immediate data to memory with carry, then skip if not carry	$M \leftarrow (M) + I + ca$ Skip if not carry	001010	D _R	D _C	I
	AD r, M		Add memory to general register	$r \leftarrow (r) + (M)$	010000	D _R	D _C	R _N
	ADS r, M	*	Add memory to general register, then skip if carry	$r \leftarrow (r) + (M)$ Skip if carry	010001	D _R	D _C	R _N
	ADN r, M	*	Add memory to general register, then skip if not carry	$r \leftarrow (r) + (M)$ Skip if not carry	010010	D _R	D _C	R _N
	AC r, M		Add memory to general register with carry	$r \leftarrow (r) + (M) + ca$	011000	D _R	D _C	R _N
	ACS r, M	*	Add memory to general register with carry, then skip if carry	$r \leftarrow (r) + (M) + ca$ Skip if carry	011001	D _R	D _C	R _N
	ACN r, M	*	Add memory to general register with carry, then skip if not carry	$r \leftarrow (r) + (M) + ca$ Skip if not carry	011010	D _R	D _C	R _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)			
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)
SUBTRACTION INSTRUCTION	SI M, I		Subtract immediate data from memory	$M \leftarrow (M) - I$	000011	D _R	D _C	I
	SIS M, I	*	Subtract immediate data from memory, then skip if borrow	$M \leftarrow (M) - I$ Skip if borrow	000100	D _R	D _C	I
	SIN M, I	*	Subtract immediate data from memory, then skip if not borrow	$M \leftarrow (M) - I$ Skip if not borrow	000101	D _R	D _C	I
	SIB M, I		Subtract immediate data from memory, with borrow	$M \leftarrow (M) - I - b$	001011	D _R	D _C	I
	SIBS M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ Skip if borrow	001100	D _R	D _C	I
	SIBN M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	$M \leftarrow (M) - I - b$ Skip if not borrow	001101	D _R	D _C	I
	SU r, M		Subtract memory from general register	$r \leftarrow (r) - (M)$	010011	D _R	D _C	R _N
	SUS r, M	*	Subtract memory from general register, then skip if borrow	$r \leftarrow (r) - (M)$ Skip if borrow	010100	D _R	D _C	R _N
	SUN r, M	*	Subtract memory from general register, then skip if not borrow	$r \leftarrow (r) - (M)$ Skip if not borrow	010101	D _R	D _C	R _N
	SB r, M		Subtract memory from general register with borrow	$r \leftarrow (r) - (M) - b$	011011	D _R	D _C	R _N
	SBS r, M	*	Subtract memory from general register with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ Skip if borrow	011100	D _R	D _C	R _N
	SBN r, M	*	Subtract memory from general register with borrow, then skip if not borrow	$r \leftarrow (r) - (M) - b$ Skip if not borrow	011101	D _R	D _C	R _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)			
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)
COMPARISON INSTRUCTION	SLTI M, I	*	Skip if memory is less than immediate data	Skip if $(M) < I$	110000	D _R	D _C	I
	SGEI M, I	*	Skip if memory is greater than or equal to immediate data	Skip if $(M) \geq I$	110001	D _R	D _C	I
	SEQI M, I	*	Skip if memory is equal to immediate data	Skip if $(M) = I$	110010	D _R	D _C	I
	SNEI M, I	*	Skip if memory is not equal to immediate data	Skip if $(M) \neq I$	110011	D _R	D _C	I
	SEQ r, M	*	Skip if general register is equal to memory	Skip if $(r) = (M)$	001110	D _R	D _C	R _N
	SNE r, M	*	Skip if general register is not equal to memory	Skip if $(r) \neq (M)$	001111	D _R	D _C	R _N
TRANSFER INSTRUCTION	LD r, M		Load memory to general register	$r \leftarrow (M)$	000110	D _R	D _C	R _N
	ST M, r		Store general register to memory	$M \leftarrow (r)$	000111	D _R	D _C	R _N
	MVSR M ₁ , M ₂		Move memory to memory in the same row	$(D_R, D_{C1}) \leftarrow (D_R, D_{C2})$	100100	D _R	D _{C1}	D _{C2}
	MVIM M, I		Move immediate data to memory	$M \leftarrow I$	100101	D _R	D _C	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	$[(G), (r)] \leftarrow (M)$	100110	D _R	D _C	R _N
	MVGS M, r		Move source memory referring to G-register and general register to memory	$M \leftarrow [(G), (r)]$	100111	D _R	D _C	R _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)				
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)	
INPUT AND OUTPUT INSTRUCTION	PLL	M, C	Input PLL port data to memory	$M \leftarrow [PLL]_C$	101000	D _R	D _C	0	C _N
			Output contents of memory to PLL port	$[PLL]_C \leftarrow (M)$				1	C _N
	SEG	M, C	Input SEG port data to memory	$M \leftarrow [SEG]_C$	101001	D _R	D _C	0	C _N
			Output contents of memory to SEG port	$[SEG]_C \leftarrow (M)$				1	C _N
	IO	M, C	Input IO port data to memory	$M \leftarrow [IO]_C$	101011	D _R	D _C	0	C _N
			Output contents of memory to IO port	$[IO]_C \leftarrow (M)$				1	C _N
	MARK	M, C	Input MARK port data to memory	$M \leftarrow [MARK]_C$	101010	D _R	D _C	0	C _N
			Output contents of memory to MARK port	$[MARK]_C \leftarrow (M)$				1	C _N
	KEY	M, C	Input KEY port data to memory	$M \leftarrow [KEY]_C$	101100	D _R	D _C	0	C _N
			Output contents of memory to KEY port	$[KEY]_C \leftarrow (M)$				1	C _N
	SIO	M, C	Serial input port data of external device to memory	$M \leftarrow [SIO]_C$	101101	D _R	D _C	0	C _N
			Serial output contents of memory to port of external device	$[SIO]_C \leftarrow M$				1	C _N

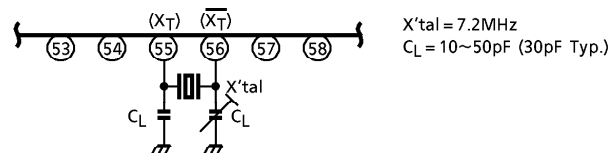
INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)			
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)
LOGICAL OPERATION INSTRUCTION	ORR r, M		Logical OR of general register and memory	$r \leftarrow (r) \vee (M)$	010110	D _R	D _C	R _N
	ANDR r, M		Logical AND of general register and memory	$r \leftarrow (r) \wedge (M)$	010111	D _R	D _C	R _N
	ORIM M, I		Logical OR of memory and immediate data	$M \leftarrow (M) \vee I$	011110	D _R	D _C	I
	ANIM M, I		Logical AND of memory and immediate data	$M \leftarrow (M) \wedge I$	011111	D _R	D _C	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	$M \leftarrow (M) \oplus I$	101110	D _R	D _C	I
	XORR r, M		Logical exclusive OR of general register and memory	$r \leftarrow (r) \oplus (M)$	101111	D _R	D _C	R _N
BIT JUDGE INSTRUCTION	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if $r [N (M)] = \text{all "1"}$	111000	D _R	D _C	R _N
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if $r [N (M)] = \text{all "0"}$	111001	D _R	D _C	R _N
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if $M (N) = \text{all "1"}$	111010	D _R	D _C	N
	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if $M (N) = \text{all "0"}$	111011	D _R	D _C	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if $M (N) = \text{not all "1"}$	111100	D _R	D _C	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if $M (N) = \text{not all "0"}$	111101	D _R	D _C	N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16BIT)			
					IC (6BIT)	A (2BIT)	B (4BIT)	C (4BIT)
SUBROUTINE INSTRUCTION	CALL ADDR ₁		Call subroutine	STACK←(PC) + 1 and PC←ADDR ₁	1000	ADDR ₁ (12bit)		
	RN		Return to main routine	PC←(STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC←(STACK) and skip	111111	01	—	—
JUMP INSTRUCTION	JUMP ADDR ₁		Jump to the address specified	PC←ADDR ₁	1101	ADDR ₁ (12bit)		
OTHER INSTRUCTIONS	DAL ADDR ₂ , r		Load program memory in page 0 to DATA register	DATA←[ADDR ₂ + (r)] _p in page 0	111110	ADDR ₂ (6bit)		R _N
	CKSTP		Clock generator stop	Stop clock generator if $\overline{INH} = "0"$	111111	10	—	—
	NOOP		No operation	—	111111	11	—	—

- (Note 1) When executing I/O instruction, input/output of the instruction is automatically controlled according to a value of the most significant bit of Port Code No. (C).
- MSB of Code No. (C) = "1" : Output instruction
 - MSB of Code No. (C) = "0" : Input instruction
- (Note 2) Basically execution of SIO instruction is treated similar to execution of other I/O instructions (PLL instruction, SEG instruction, etc.) except the following points :
- First, it is necessary to select an external device that becomes a destination of transferring serial data by the chip select code ((C) = FH). (Refer Item 1 of Serial Interface.)
 - SIO instruction execution time is 55.5μs (5 machine cycle).
- (Note 3) As the TC9321F has no input port that is treated in the execution of SEG and MARK instructions, this input instruction cannot be used.
- (Note 4) Low order 4 bits out of the program memory address 10 bits designated by DAL instruction are to be indirectly addressed according to contents of the general register.
DAL instruction execution time is 22.2μs (2 machine cycle).

○ Connection of crystal resonator

Connect a crystal resonator to the crystal oscillator terminal (X_T , $\overline{X_T}$ terminal) of a device as illustrated below. This oscillation signal is supplied to the clock generator and the reference frequency divider for generating various CPU timing signals and reference frequency signals.



(Note) Use a crystal resonator having a low CI value and good starting characteristic.

○ System reset

When "L" level signal is input to the \overline{INI} terminal or 0~3.5V is supplied to the V_{DD} terminal (Power ON Reset), system reset is applied to a device.

After 10ms of standby time passed after the system reset, a program starts from address 0.

Normally, as the Power ON reset function is used, the \overline{INI} terminal shall be fixed at "H" level.

(Note 1) During the system reset, general output port (T0~T7, OT1~OT4) are fixed at "L" level.

(Note 2) After the system reset, I/O ports are all set in the input mode.

However, no initialization of output ports and internal ports (G-Register, etc.) is performed. In particular, contents of these ports become indefinite when the power source is initially turned on and therefore, it becomes necessary to initialize them programmatically as necessary.

I/O PORT CODE No.	PLL (φ1)								SEG (φ2)								MARK (φ3)								IO (φ4)								KEY (φ5)								SIO (φ6)															
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8																				
0	I/O PORT-5								I/O PORT-5								I/O PORT-5								I/O PORT-1																															
1	I/O PORT-6								I/O PORT-6								I/O PORT-6								I/O PORT-2																															
2	I/O PORT-7								I/O PORT-7								I/O PORT-7								I/O PORT-3/DA REF DATA								KEY INPUT																							
3	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
4	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
5	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
6	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
7	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
8	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
9	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
A	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
B	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
C	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
D	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
E	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
F	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							
	I/O PORT-8								I/O PORT-8								I/O PORT-8								I/O PORT-4								AD OUT								0								0							

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○ I/O map

All ports in the device are expressed by a matrix of 6 I/O instructions (PLL, SEG, MARK, IO, KEY and SIO, instruction) with 4bit Code No. C. Allocation of these ports are shown above as the I/O Map. In this Map, port names treated in execution of I/O instructions are assigned on the axis of ordinates and port code numbers on the axis of abscissas. G-register and data register are also treated as ports.

Basically, data of all ports are treated in unit of 4 bits, and Code No. (C)=0H~7H are designated as the input ports and Code No. (C)=8H~FH as the output ports.

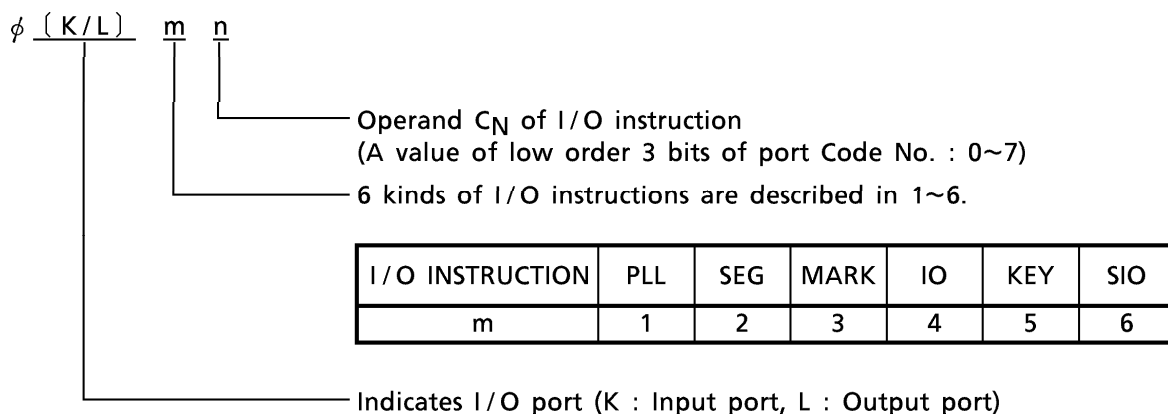
(Note 1) The oblique lined ports shown on the I/O map are actually not existed in the device. If data was output to an unexisted port when an output instruction was executed, contents of other parts and the data memory are not especially affected.

If an unexisting input port was designated when executing an input instruction, contents of data to be read in the data memory will become indefinite.

(Note 2) Ports with *mark out of output ports on the I/O map are unused ports. Data being output to these ports will become don't care.

(Note 3) Contents of ports expressed in 4 bits, that is, Y1 corresponds to LSB of data of the data memory and Y8 corresponds to MSB. Data of all ports are treated in positive logic.

(Note 4) Ports that are designated by 6 I/O instructions and Code No. C are expressed by encoding as shown below.



○ Programmable counter

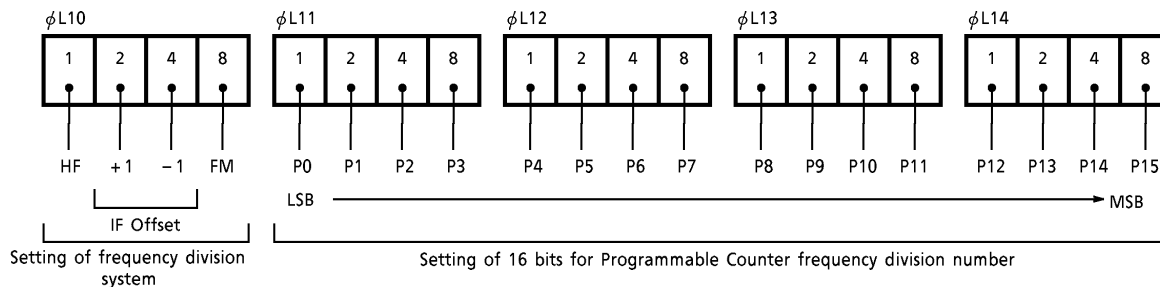
The programmable counter consists of 2-modulus prescaler, 4bit + 12bit programmable binary counter, and PLL I/O port group that controls these prescaler and counter.

Further, the programmable counter is turned ON/OFF according to contents of the reference port, that is, when contents of the reference port (4 bits) are all "1", the programmable counter is put in the PLL OFF Mode and otherwise, it is put in the PLL ON Mode.

1. PLL I/O ports (ϕ KL10~ ϕ KL14)

These are exclusive ports for PLL to control all of frequency division number, frequency division system, and IF correction (IF offset) at FM band, and are accessed by PLL output instructions designated [$C_N=0\sim 4$] in the operand field (ϕ L10~ ϕ L14).

1) Construction of PLL ports



2) Setting of frequency division system

The pulse swallow system or the direct frequency division system are selected according to HF and FM ports.

Select any of 4 systems available as shown in the following table according to frequency band to be used.

MODE	HF	FM	FREQUENCY DIVISION SYSTEM	EXAMPLE OF RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT TERMINAL	FREQUENCY DIVISION NUMBER
LF	0	0	Direct frequency division system	LW, MW, SW _L	0.5~ 20MHz	AM _{IN}	n
HF	1	0	$\left(\frac{1}{15} / \frac{1}{16}\right)$ pulse swallow system	SW _H	1~ 40MHz	AM _{IN}	n
FM _L	0	1	$\left(\frac{1}{15} / \frac{1}{16}\right)$ pulse swallow system	FM	30~140MHz	FM _{IN}	n
FM _H	1	1	$\left(\frac{1}{2} \times \frac{1}{15} / \frac{1}{16}\right)$ pulse swallow system	WB *	30~185MHz	FM _{IN}	2·n

* : Weather Band

(Note) n denotes a programmed divided frequency value.

3) IF correction function at FM band

When the pulse swallow system was selected, actual frequency division number is variable of ± 1 without changing programmed frequency division value by $\Delta IF \pm 1$ port.

This function can be used for IF offset at FM band.

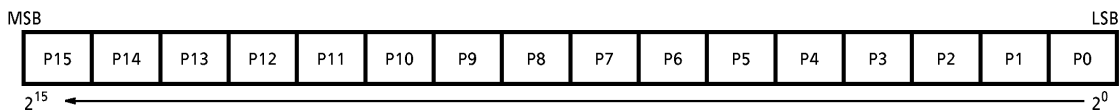
And when the direct division system was selected, the IF offset function does not operate.

$\Delta IF + 1$	$\Delta IF - 1$	FREQUENCY DIVISION NUMBER (FM _H)	FREQUENCY DIVISION NUMBER (FM _L)
0	0	2·n	n
0	1	2·(n - 1)	n - 1
1	0	2·(n + 1)	n + 1
1	1	2·(n - 1)	n - 1

4) Setting of frequency division number

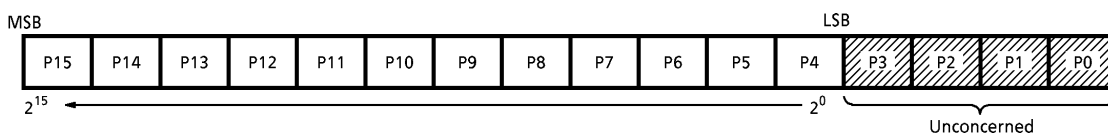
Set frequency division number of the program counter in binary number in P0~P15 ports.

- Pulse swallow system (16bit)



* Frequency division number setting range (pulse swallow system)
 $n = 210H \sim FFFFH$ (528~65535)

- Direct frequency division system (12bit)



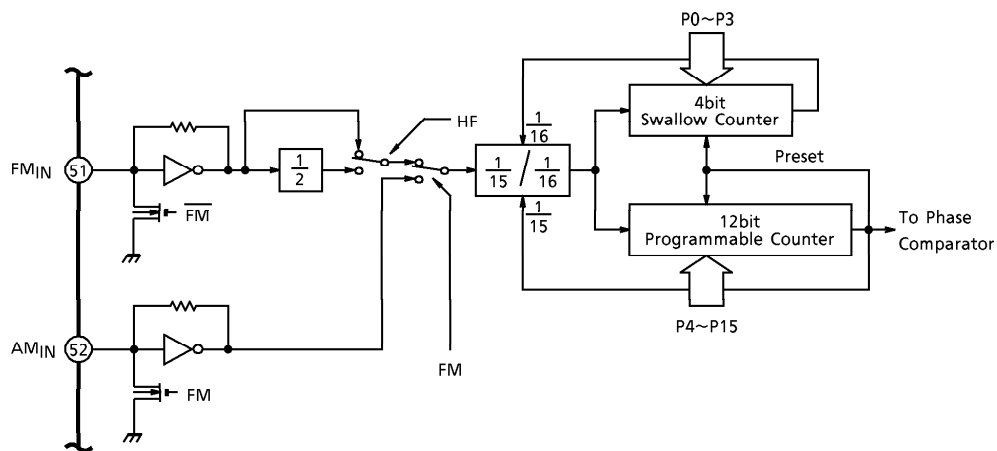
* Frequency division number setting range (Direct Frequency Division system)
 $n = 10H \sim FFFH$ (16~4095)

- (Note) Since no offset is provided to the program counter, a programmed division number will become an actual division number. However, it will become 2 times of a programmed value in case of FM_H mode.
- (Note) In case of the direct division system, data of P0~P3 ports (ϕ L11) become unconcerned and P4 port becomes LSB.
- (Note) All data of frequency division number are updated at the same time when MSB port (ϕ L14) data are set. This is to prevent the lock-up time from being adversely affected by successive change of frequency division number. Therefore, MSB port (ϕ L14) data must be set lastly when frequency division numbers are set. Further, even if data set is considered unnecessary (if data is the same as the previous data), it is necessary to execute data setting only for MSB port (ϕ L14).

2. Circuit configuration of prescaler and programmable counter

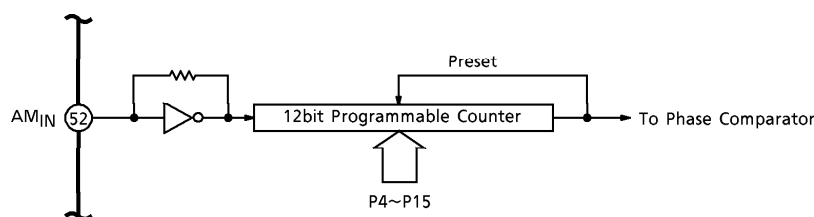
1) Circuit configuration in case of pulse swallow system

The circuit consists of 1/15/1/16 2-modulus prescaler, a 4bit swallow counter, and a 12bit binary programmable counter. Further, in case of FM mode, 2 1/2 divider is added to the front stage of the prescaler.



2) Circuit configuration in case of direct frequency division system

In this case, a 12bit programmable counter is only used instead of the prescaler.



(Note) Both the FM_{IN} and AM_{IN} terminals have built-in an amplifier respectively, and are operable at small amplitude with coupled capacitors. Further, when the input terminal not selected according to the frequency division system and the reference port data (4 bits) are all "1", the inputs are pulled down.

○ Reference frequency divider

This frequency divider generates 10 kinds of PLL reference frequency signals 1, 3.125, 5, 6.25, 9, 10, 12.5, 25, 50, and 100kHz by dividing external 7.2MHz crystal oscillation frequency signals.

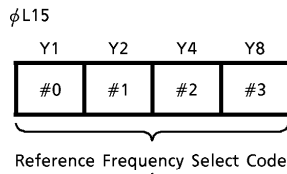
These frequency signals are selected according to the reference port data.

A selected signal is supplied as the reference frequency of the phase comparator described below.

Further, according to the contents of the reference port, PLL ON/OFF is performed.

1. Reference port (ϕ L15)

This is the internal port to select 10 kinds of reference frequency signals. It is normally accessed by PLL output instruction having [C_N=5] designated in the operand. Further, when the contents of the reference port are all "1", the programmable counter and the reference counter stop and it becomes PLL OFF mode.

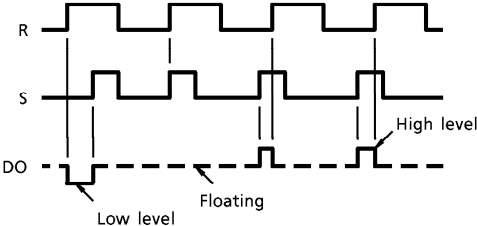
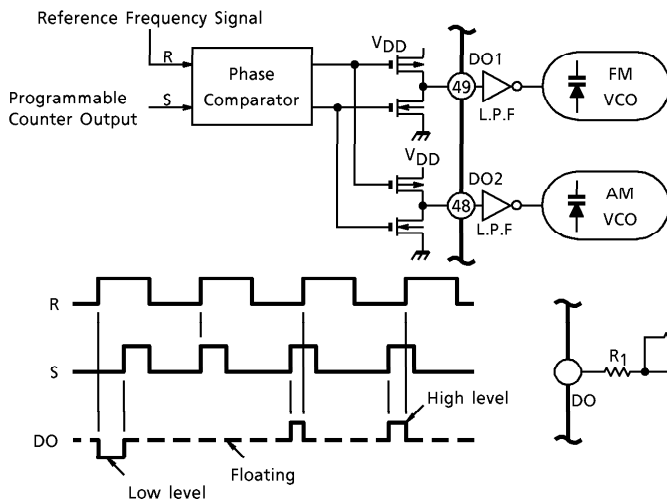


Reference Frequency Table

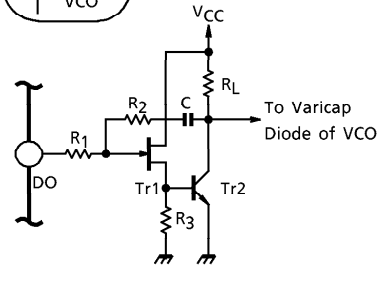
#3	#2	#1	#0		REFERENCE FREQUENCY
0	0	0	0	0	1kHz
0	0	0	1	1	50kHz
0	0	1	0	2	5kHz
0	0	1	1	3	100kHz
0	1	0	0	4	9kHz
0	1	0	1	5	10kHz
0	1	1	0	6	12.5kHz
0	1	1	1	7	25kHz
1	0	0	0	8	3.125kHz
1	0	0	1	9	6.25kHz
1	0	1	0	A	Inhibit
1	1	1	0	E	
1	1	1	1	F	PLL OFF Mode

○ Phase comparator

The phase comparator compares phase difference between the reference frequency signal supplied from the reference frequency divider and the programmable counter division output and transmits their difference and then, controls VCO through a low-pass filter so that these two signal frequencies and phases agree with each other. As there are two parallel tri-state buffer terminals DO1 and DO2 for output from the phase comparator, it is possible to design optimum filter constant for every FM/AM band.



DO output Timing Chart



Example of Active Low-Pass Filter Circuit

Standard
 Tr1 : 2SC1815
 Tr2 : 2SK246
 Examples of Low-Pass Filter Constants (Reference Values at FM band)
 C = 0.33 μF
 R₁ = 10kΩ
 R₂ = 8.2kΩ
 R₃ = 330Ω
 R_L = 10kΩ

A DO output timing chart and an example of the active low-pass filter circuit through the Darlington connection of FET and transistors are shown in the above diagram. Further, the filter circuit shown in the above diagram is one example for reference and an actual circuit shall be examined and designed according to the receiving band structure of a system and desired characteristics.

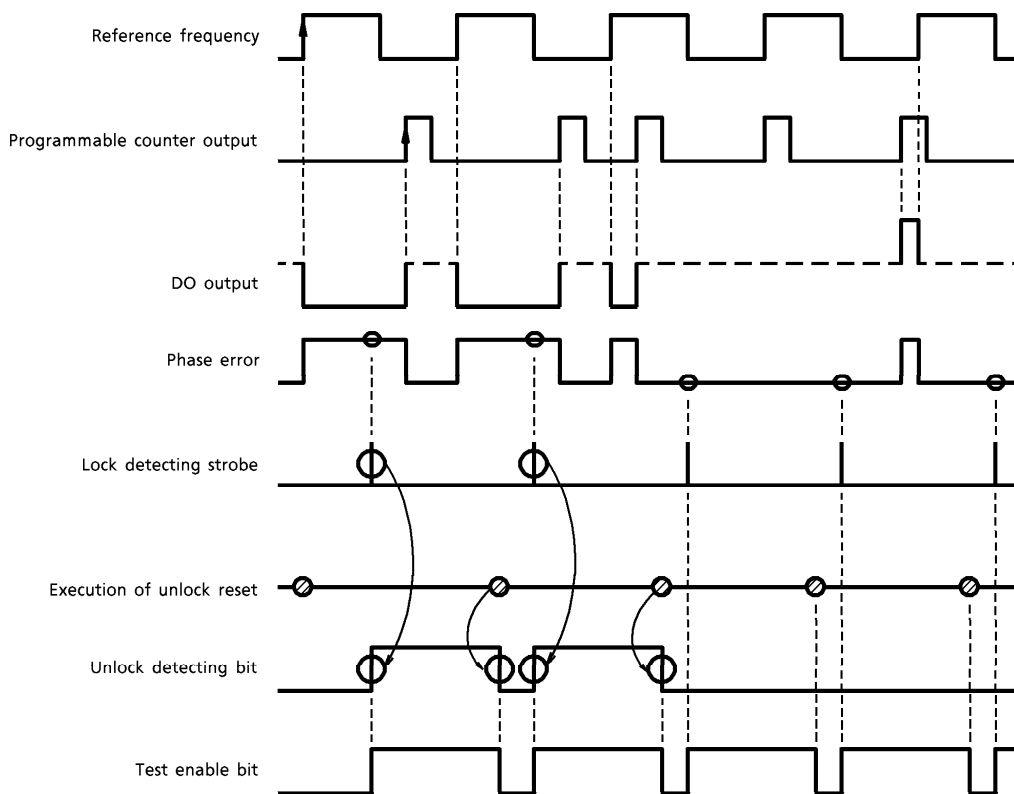
○ Unlock detecting bit (ϕ LK17)

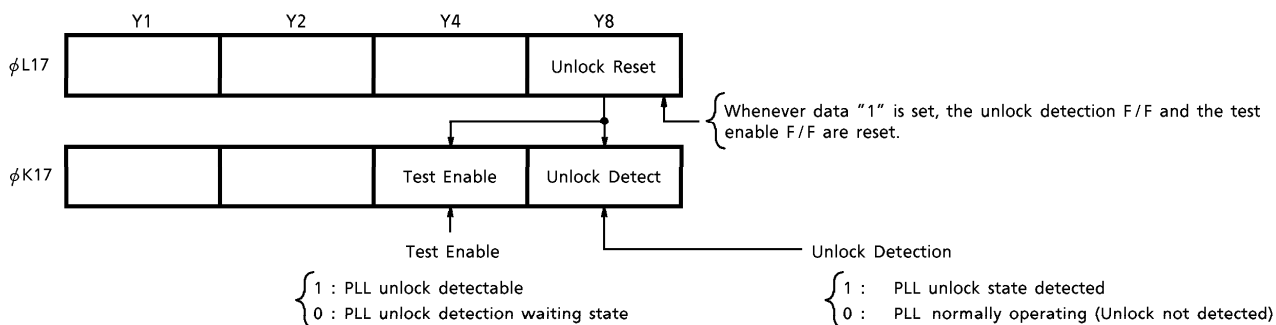
This is a bit to detect the lock state of PLL system. In the unlocked state, that is, the state where reference frequency is not in accord with the programmable counter division output, (phase error) pulses are output to the unlock F/F at reference frequency cycle from the phase comparator. The unlock F/F is set by these phase pulses. Further, whenever the unlock reset bit is set to "1" by the PLL output instruction designated [$C_N=7$] in the operand, the unlock F/F is reset (ϕ L17).

After resetting the unlock F/F, the lock state can be detected by accessing the unlock detecting bit by the PLL input instruction designated [$C_N=7$] in the operand (ϕ L17).

Since pulses are input at reference frequency cycle, it is necessary to access the unlock detecting bit with providing a time more than reference frequency cycle after resetting the unlock F/F. If this time was short, the proper lock state cannot be detected.

Therefore, the test enable F/F is provided. This test enable F/F is reset whenever "1" is set for the unlock reset bit and is set to "1" at the unlock detection timing. That is, the unlock state can be properly detected only when this test enable bit (ϕ K17) is set at "1".





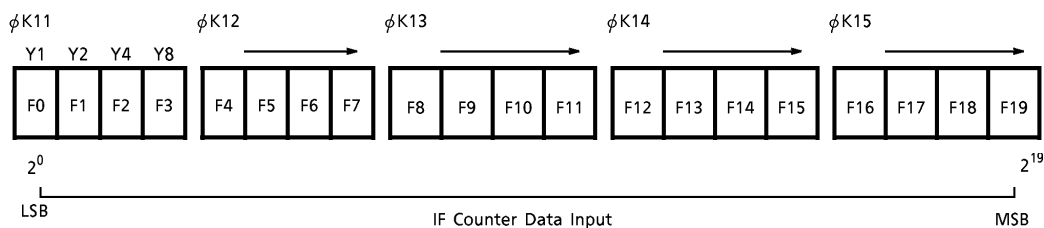
○ General purpose IF counter

This is a 20bit general purpose IF counter that is used to count FM or AM intermediate frequency (IF) and is usable for detection of auto stop signal, etc.

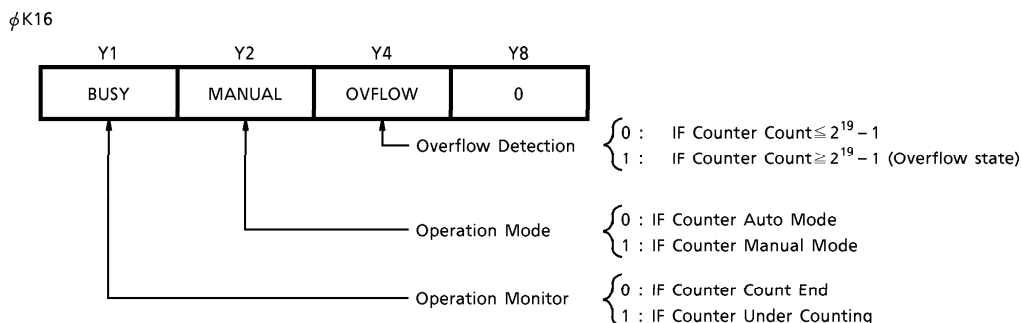
The IF counter consists of a 20bit binary counter and IF counter control ports.

1. IF counter data ports ($\phi K11 \sim \phi K16$)

These are the data input ports for reading count data and operating state of the IF counter. Data are read in the data memory by the PLL input instruction designated [$C_N = 1 \sim 5$] in the operand.



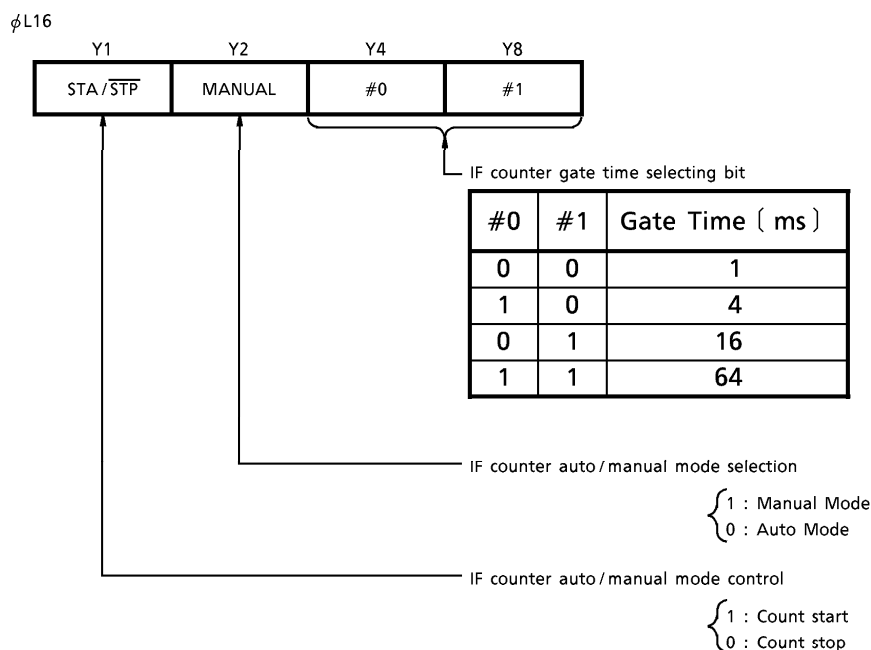
Date counted by the IF counter can be input in binary number through the input ports F0~F19.



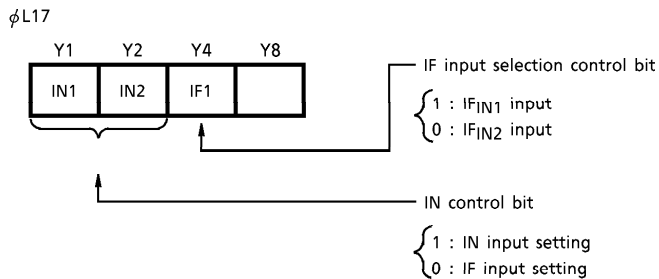
This is an input port (ϕ K16) to detect the operating state of the IF Counter. When using the IF counter, count data (F0~F19) shall be processed after confirming that BUSY bit is "0" (Count end) and OVFLOW bit is "0" (no overflow).

2. IF counter control ports (ϕ L16, ϕ L17)

These are ports to output data for control of IF counter operation, and are accessible by the PLL output instruction designated [C_N = 6 or 7] in the operand.



In the auto mode (MANUAL bit is set to "0"), IF count starts whenever STA/ $\overline{\text{STP}}$ bit set to "1". IF count ends automatically after passing a gate time selected by #0 or #1 bit. Further, in the manual mode, when STA/ $\overline{\text{STP}}$ is set to "1", IF count starts and continues till STA/ $\overline{\text{STP}}$ bit is set to "0".



(Note) Input ports and IF input are selectable in 1bit unit.

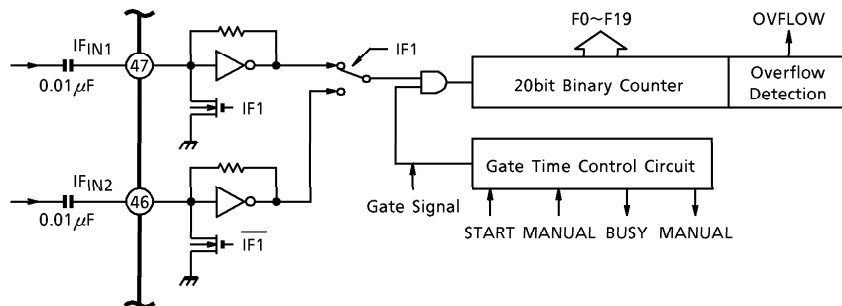
In case that IF counter is used, IN control bit that corresponds to an input terminal to be used shall be set to "0" and IF input selection control bit shall be designated.

(Note) In the PLL OFF mode, IF counter is reset by force and IF counter input is pulled down. Further, the input that is not selected by IF input selection control bit (IF 1bit) at the IF counter is pulled down.

(Note) After system reset, IN control bit is set to "0" and IF input selection control bit is set to "1".

3. IF counter circuit configuration

The IF counter consists of input amplifiers, gate time control circuit, and 20bit binary counter.



(Note) IF_{IN} terminals have built-in amplifiers and are capable of operating at small amplitude with coupled capacitors.

○ I/O ports

1. I/O ports -1, -2, -3, -4, -5, -6, -7, -8

I/O Ports -1, -2, -4, -5, -6, -7 are 4bit ports where input/output are selectable in a unit of each bit, I/O Port-3 is 3bit port and I/O Port-8 is 2bit port where input/output are selectable in a unit of each bit. Input/output are set in I/O ports according to the contents of I/O control inner port. To set input in I/O port, set "0" in I/O control port bit corresponding to that I/O port and to set output in I/O port, set "1".

In case of setting input port, data that have been currently input to I/O ports are read in the data memory when IO input instructions corresponding to respective I/O ports are executed. At this time, the contents of the output side latch gives no effect on input data.

In case of setting output port, the I/O port output state is controlled by executing IO output instructions corresponding to respective I/O ports. Further, the contents of data currently being output are read in the data memory when IO input instruction is executed.

Further, I/O Port-3 is also used as the analog input/output of 6bit A/D and D/A converters, and I/O Port-2 is also used as the serial interface. Therefore, when I/O Port-2 and -3 are used, the contents of A/D ON bit and SIO ON bit should be set to "0".

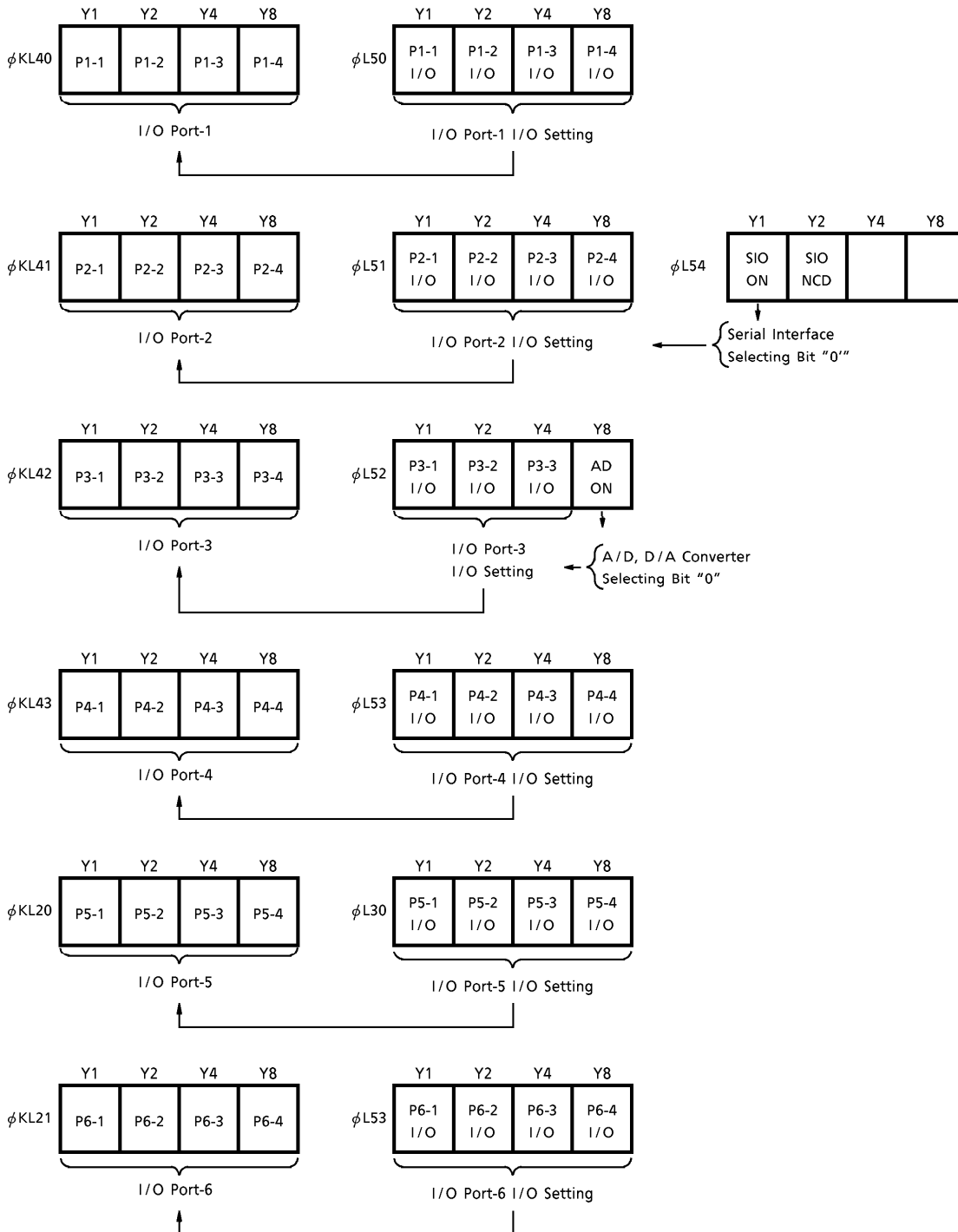
(Refer to items of A/D and D/A Converters and Serial Interface.)

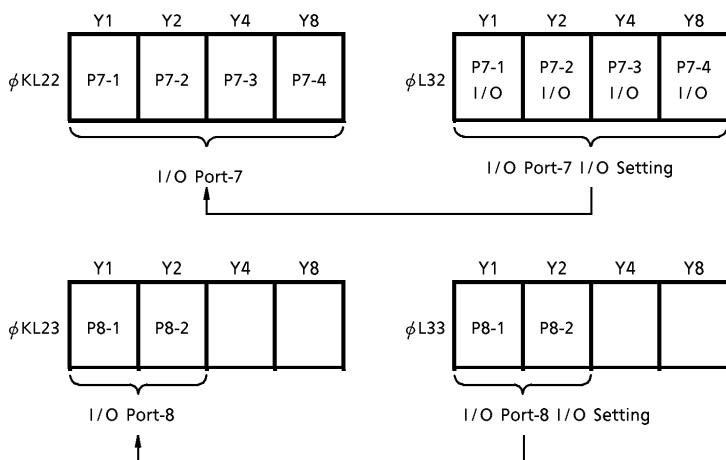
(Note) Output side latch P3-4 data are input from Input Port P3-4.

(Note) Output side latch P3-4 data are normally unconcerned, and when A/D converter is in operation it becomes effective. Further, after system reset, the contents of AD ON bit and SIO ON bit are reset to "0", and D/A converter and serial interface terminal becomes I/O port.

(Note) After system reset, the contents of I/O control ports are all reset to "0" and all I/O ports are set in the input mode.

(Note) During the clock stop mode, the output state of all I/O ports that have been set in the output mode is automatically fixed at "L" level but the contents of all output latches are kept at the preceding data.



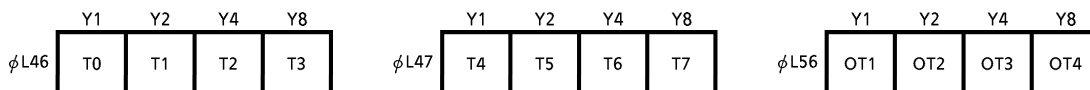


2. Key timing output (T0~T7), general purpose output ports (OT1~OT4)

T0~T7 are CMOS 8bit output and OT1~OT4 are CMOS 4bit output ports. Normally T0~T7 are used for output of key return timing signal of the key matrix and OT1~OT4 are used for control of mute signal, linear circuit, etc.

T0~T7 are accessed by the IO output instruction designated [CN=6 or 7] in the operand, and OT1~OT4 are accessed by the KEY output instruction designated [CN=6] in the operand. (phiL46 or phiL47 or phiL56)

(Note) During the clock stop mode, T0~T7 and OT1~OT4 outputs are automatically fixed at "L" level but the contents of the ports are kept at the preceding data.

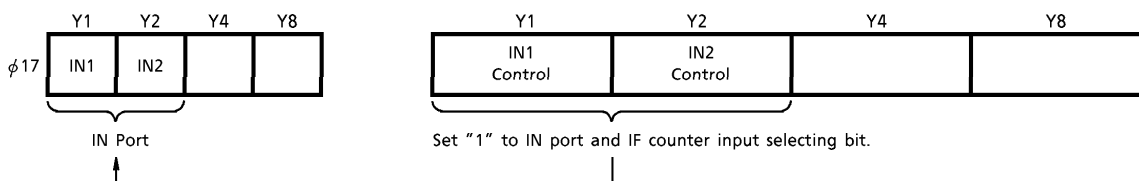


3. General purpose input ports (IN1, IN2)

IN1 and IN2 are CMOS 2bit input ports. These ports are also used as the IF counter input and they are selected according to the contents of IN control port.

(Refer to Item of General Purpose IF Counter.)

In case of setting the input ports, IN control port bit shall be set to "1" by the PLL output instruction designated [CN=7] in the operand and data of the input terminals are read in the data memory by executing the PLL input instruction designated [CN=7] in the operand.



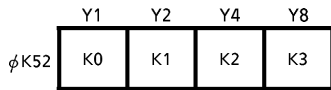
(Note) When IF counter is used, the contents of IN Port becomes "0".

(Note) After system reset, the contents of IN control port are reset to "0".

4. Key input ports (K0~K3)

K0~K3 are the 4bit exclusive key input terminals for key matrix input. Each of these 4 terminals has a built-in pull-down resistor.

Data is read in the data memory from the key input terminal when the key input instruction designated [C_N=2] in the operand is executed.



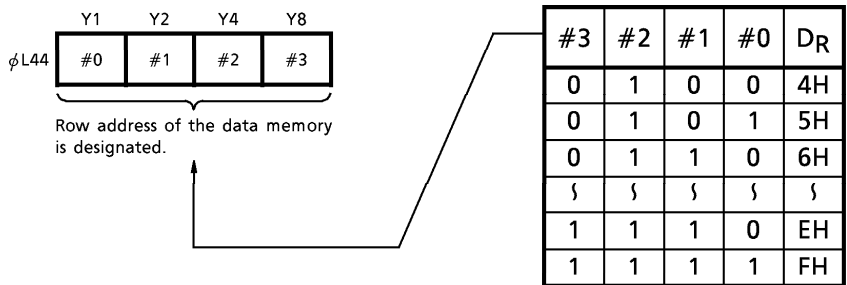
○ Register ports

G-Register and Data Registers described in the explanation of CPU are also treated as the inner ports.

1. G-Register (φL44)

This is a register for addressing row addresses (D_R=4H~FH) of the data memory when MVGD / MVGS instruction are executed. This register is accessed by IO output instruction designated [C_N=4] in the operand.

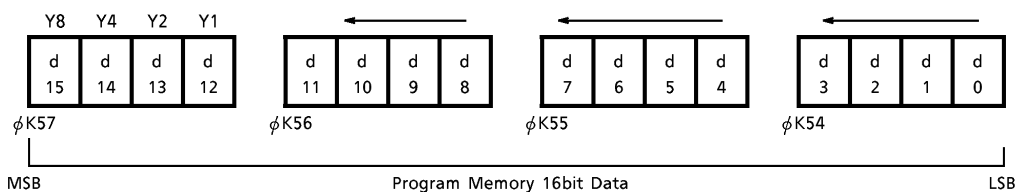
(Note) The contents of this register becomes valid only when MVGD / MVGS instruction are executed, and are not concerned with other instructions.



(Note) All row address of the data memory also can be designated indirectly by setting data 0H~FH in the G-register. (D_R=0H~FH)

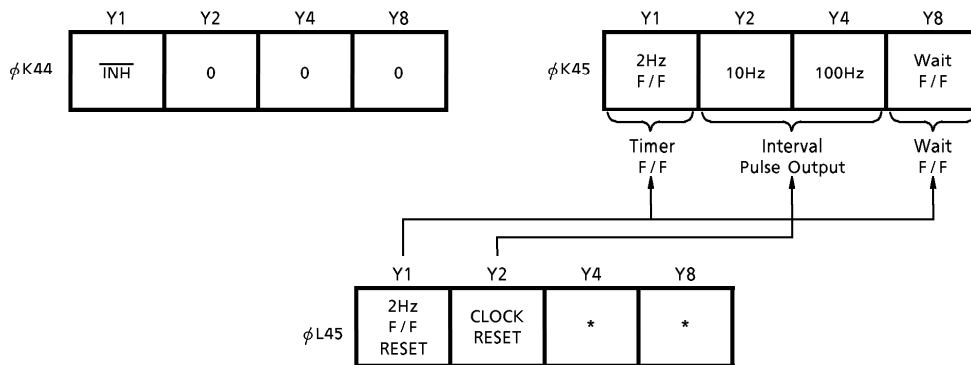
2. Data register (φK54~φK57)

This register is a 16bit register into which the program memory data are loaded. The contents of this register are read in the data memory in a unit of 4 bits when KEY input instruction designated [C_N=4~7] in the operand are executed. This register can be used for LCD segment decoding operation and taking radio band edge data, coefficient data of Binary to BCD conversion, etc.



○ Internal control ports

The internal control ports are used for reading the internal state of a device into the data memory, that is needed to know for program execution, and for resetting the internal state of a device.



1. \overline{INH} input port ($\phi K44$)

This is a single bit input port for input the \overline{INH} terminal data. The contents of this port are read in the data memory by executing IO input instruction designated [$C_N=4$] in the operand. When CKSTP instruction is executed during "L" level being applied to this terminal, the device is put in the clock stop mode.

(Note) In executing the CKSTP instruction, make sure that the contents of the \overline{INH} input port is "0" and set the PLL OFF mode (set the contents of the reference port to all "1".) before executing the CKSTP instruction.

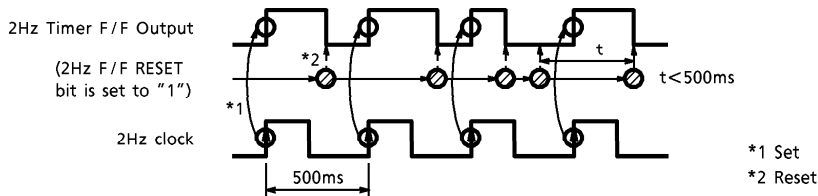
2. 2Hz timer F/F ($\phi K45$)

The 2Hz timer F/F is set by 2Hz (500ms) signal, and is reset when data "1" is set to 2Hz F/F RESET bit by executing the IO output instruction designated [$C_N=5$] in the operand. This F/F output is read in the data memory when the IO input instruction designated [$C_N=5$] in the operand is executed.

Since the 2Hz timer F/F is automatically set at intervals of 500ms, it can be used for ordinary clock count.

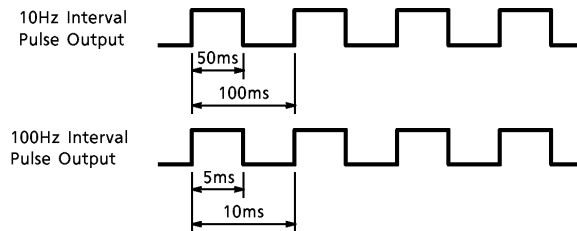
The 2Hz timer F/F can be reset only by 2Hz F/F RESET bit, therefore, if data "1" can not be set to the 2Hz RESET bit within the 500ms period, a count error is caused and a correct time may not be obtained.

(Note) When the power source is applied or after the CKSTP instruction was executed, the state of 2Hz timer F/F output becomes uncertain.



3. 10Hz/100Hz interval pulses (ϕ K45)

10Hz interval pulse is a 100ms period, 50% duty pulse, and 100Hz interval pulse is a 10ms period, 50% duty pulse and both are output to 10Hz and 100Hz bits. These pulses are read in the data memory when the IO input instruction designated [$C_N = 5$] in the operand is executed. These outputs have no flip-flop and are available for counting of muting time, and scanning time of tuning, etc.



4. CLOCK RESET bit (ϕ L45)

Whenever data "1" is set to this bit, time base below 50Hz is reset. (10Hz interval pulse is also reset but 100Hz interval pulse is not reset.)

This bit is used for adjustment of clock time. Accuracy of clock at the time is +0.02 / -0s.

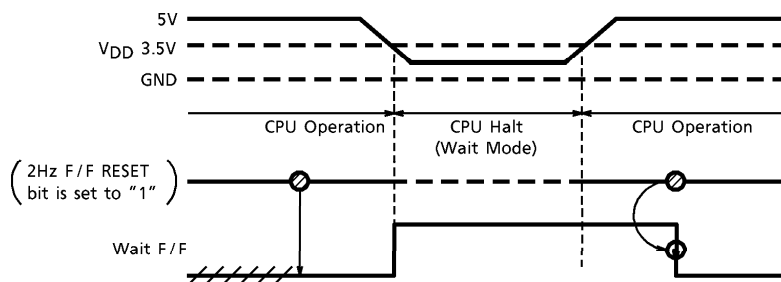
5. Wait F/F bit (ϕ K45)

IF the power supply voltage at the V_{DD} terminal dropped below 2.5~3.5V during CPU operation, CPU comes to halt to prevent its malfunction at a timing when voltage drops below 2.5~3.5V (Wait Mode).

The Wait F/F is set under this state, and when voltage at the V_{DD} terminal rises above 3.5V, CPU restarts to run.

Therefore, if Wait F/F bit data was read in the data memory by executing the KEY input instruction designated [$C_N = 5$] in the operand and Wait F/F bit was set to "1", the initialization, clock correction, etc. shall be performed when necessary.

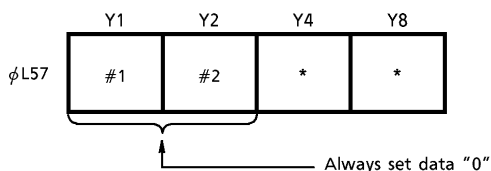
Wait F/F bit is also reset when "1" is set to 2Hz F/F RESET bit.



(Note) In the Wait mode, the inner data just before the Wait Mode are retained and no instruction can be executed.

6. TEST port (ϕ L57)

This TEST Port is an internal port for testing function of device. This port is accessed by executing the KEY output instruction designated [$C_N=7$] in the operand. In case of ordinary Program, data "0" shall be always set.



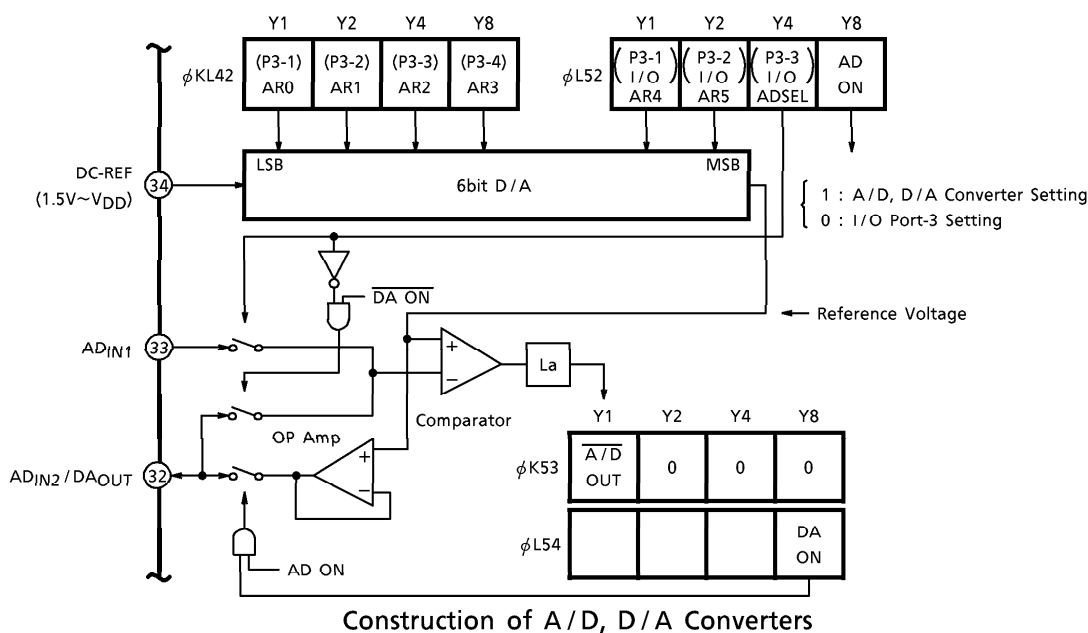
○ A/D and D/A converters

The TC9321F has built-in programmatic sequential comparison type 6bit A/D and D/A converters. 3 I/O port terminals are used for the A/D and D/A converters, which are selected by AD ON bit.

When data "1" is set to AD ON bit, P3-1 is switched to the reference voltage input (DC-REF), P3-2 to the analog voltage input (AD_{IN1}), and P3-3 to the analog voltage input/output (AD_{IN2}/DA_{OUT}).

In this case, 4 bits of I/O port-3 output side latch, (ϕ L42) and 3 bits of I/O Control Port-3 output side latch (ϕ L52) become A/D and D/A converter control data ports.

The A/D, D/A converter consists of 2 6bit D/A converter, comparator, operational amplifier, and control circuit.



(Note) After system reset, AD ON bit, DA ON bit, ADSEL bit, AR5 bit are all reset to "0".

(Note) The 6bit D/A circuit for generating reference voltage is commonly used for the A/D converter and D/A converter.

1. A/D converter

The A/D converter is of 2 channel multiplex type and can be used for field strength measurement, analog voltage level detection, etc.

When AR0~AR3 bits data (ϕ L42) are set after setting of AD ON bit, ADSEL bit, and AR4/AR5 bits (ϕ L52) data, comparison voltage corresponding to AR0~AR5 data is compared with input voltage (AD input) in the A/D converter, and the result of this comparison is stored in the comparator output latch.

This comparison result is output to the $\overline{\text{AD OUT}}$ Port (ϕ K53), and this data is read in the data memory when the KEY input instruction designated [$C_N=3$] in the operand is executed.

The relation between input voltage and comparison voltage, and the result of comparison to be output is as follows :

$\overline{\text{AD OUT}} = "0"$ when input voltage > comparison voltage

$\overline{\text{AD OUT}} = "1"$ when input voltage < comparison voltage

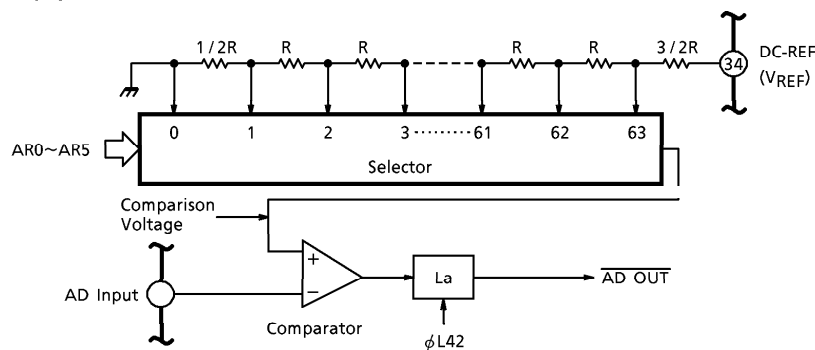
Further, comparison voltage is calculated according to the following equation :

$$\text{Comparison Voltage} = V_{\text{REF}} \times \frac{n - 0.5}{64} \left(n \text{ is AR0~AR5 data value [decimal number]} \right)$$

$63 \geq n \geq 1$

AD input of AD_{IN1} or AD_{IN2} is selected according to the contents of ADSEL bit.

That is, AD_{IN2} input is selected when ADSEL bit is "0" and AD_{IN1} input is selected when ADSEL bit is "1".



Construction of A/D Converter

AD ON	DA ON	AD SEL	AD INPUT
1	0	0	AD _{IN2}
1	0	1	AD _{IN1}
1	1	※	Invalid

(Note) Whenever AR0~AR3 data are set, comparison carried out.

(Note) ※ : don't care.

(Note) In case of A/D converter used, DA ON bit shall be set to "0".

Even if DA ON bit is set to "1" and the comparing operation is carried out (data is set to AR0~AR3 bit), the contents of $\overline{\text{AD OUT}}$ become indefinite.

(Note) String resistor of A/D converter is set at values lower by 1/2 LSB.

2. D/A converter

The D/A converter is available for control of electronic volume which is controlled by analog voltage, etc.

In case of D/A converter used, when "1" is set to both AD ON bit and DA ON bit, D/A output corresponding to AR0~AR5 data is output from the DA output terminal.

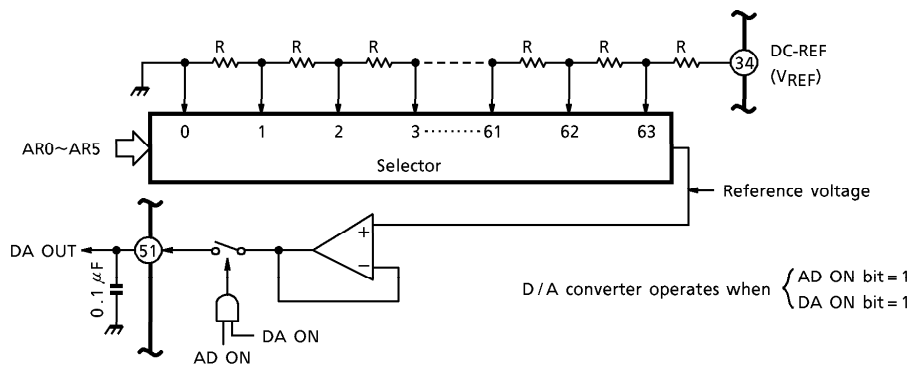
When AR0~AR5 data is changed successively, output ripple is generated at time of carry to AR4 because I/O memory layout differs between AR0~AR3 data and AR4~AR5 data.

Therefore, at time of carry to AR4, the carry shall be performed after making output to high impedance by setting DA ON bit to "0". In this case, a voltage holding capacitor is connected to the output because of being high impedance.

Further, D/A output voltage is calculated according to the following equation :

$$D/A \text{ output voltage} = V_{REF} \times \frac{n}{64} \quad (n \text{ is AR0~AR5 data [decimal number] } 63 \geq n \geq 1)$$

When the A/D converter and the D/A converter are simultaneously used, perform A/D conversion with D/A ON bit set at "0" and thereafter, output D/A analog voltage by setting DA ON bit at "1".



Construction of D/A Converter

(Note) Add an external buffer circuit to the D/A output if necessary, although it has a built-in buffer.

(Note) D/A output range is 0V~V_{DD} - 1.0V and so, be careful when V_{REF} = V_{DD}.

(Note) DA ON bit becomes invalid when AD ON bit is "0".

(Note) Voltage value of string resistor of D/A converter is a 64 divided V_{REF} value.

○ Serial interface

I/O Port-2 can be programmatically switched to the serial interface. The serial interface is a serial I/O dedicated for powerful control of a group of peripheral optional ICs.

When switched to the serial interface, 4 terminals of I/O port-2 are switched to SI, SO, CK and STB terminals. These terminals are connected to external device with 4 serial bus lines for data transfer.

By connecting peripheral optional ICs on these bus lines according to system, functions can be expanded.

Various external devices such as I/O port extension IC, static display driver, etc. are available.

Serial data transfer is carried out by executing the SIO instruction and during this instruction execution time (55.5μs), all data transfer is completed.

It is possible to handle all ports of external devices simply as inner ports that are handled through execution of other I/O instructions. Further, two kinds of serial transfer are programmatically selectable.

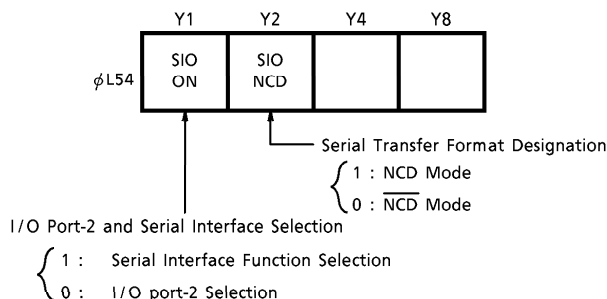
1. Serial transfer control port (φKL53)

I/O Port-2 and the serial interface are selected and controlled by the KEY output instruction designated [C_N=4] in the operand (φL54).

When SIO ON bit is set to "0", I/O port-2 is selected and when "1" is set, the serial interface is selected. Further, two kinds of the serial transfer formats are selectable by SIO NCD bit.

When SIO NCD bit is set to "0", NCD mode serial transfer format is selected.

In the NCD Mode, Port Code No. designated in the operand of SIO is serially transferred together with data. When "1" is set, the NCD Mode results. In the NCD mode, Code No. is not transferred and data only are exchanged. (C_N value in the operand of SIO instruction become don't care.)



(Note) After system reset, the contents of SIO ON bit and SIO NCD bit are automatically cleared to "0". (I/O Port-2 has been selected.)

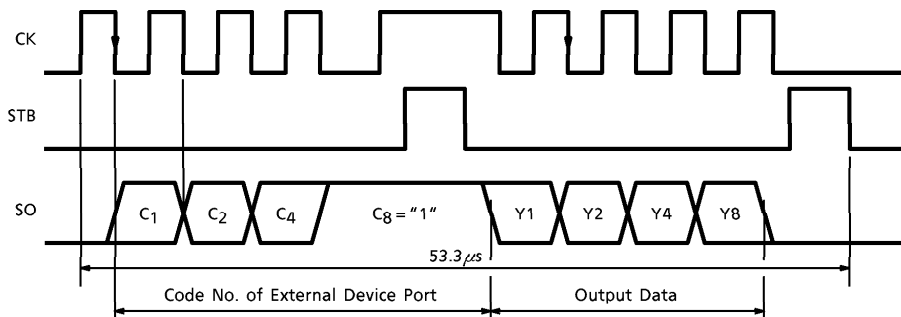
(Note) In the NCD mode, P2-1/SI and P2-4/STB terminal is selected P2-1 and P2-4. It can uses as normal I/O port.

(Note) In the NCD mode, SO terminal becomes data I/O structure. It must select input/output of SO terminal by PORT2-2 I/O CONTROL bit (φL51) before executing SIO instruction.

(Note) It is inhibited to program by executing SIO input instruction next to SIO output instruction. If in case of programming to SIO input instruction after SIO output instruction, NOOP instruction (etc.) is inserted between SIO output and SIO input instruction.

2. Serial I / O timing chart

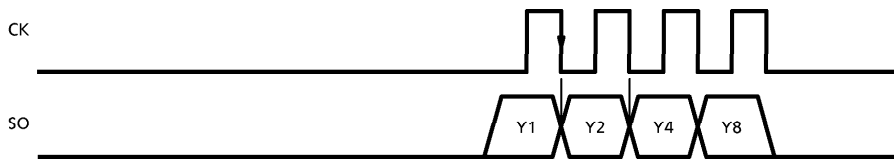
- $\overline{\text{NCD}}$ mode output timing



At the timing shown in the above chart, Code No. ($C_1 \sim C_8$: 4 bits) of the output port of destination device to which data is sent and data ($Y_1 \sim Y_8$: 4 bits) are output serially from LSB synchronizing with the fall timing of CK signal.

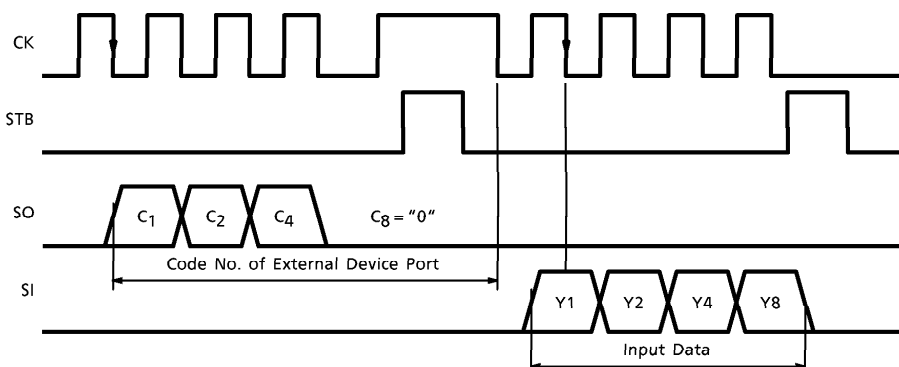
(Note) When executing the SIO output instruction ($\overline{\text{NCD}}$ Mode), C_8 bit of Code No. becomes "1".

- NCD mode output timing



Serial output in the NCD Mode will be 4bit data only. Further, STB output is always fixed at "L" level.

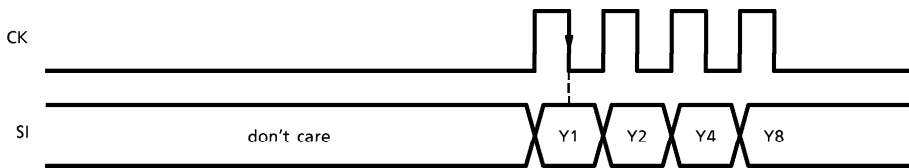
- $\overline{\text{NCD}}$ mode input timing



When Code No. ($C_1 \sim C_8$: 4 bits) of the input port of destination device is output from the SO terminal at the timing shown in the above timing chart, the contents ($Y_1 \sim Y_8$: 4 bits) of that input port are serially input into the SI terminal from LSB. SO data is output synchronizing with the fall timing of CK signal and similarly, SI data is input synchronizing with the fall timing of CK signal.

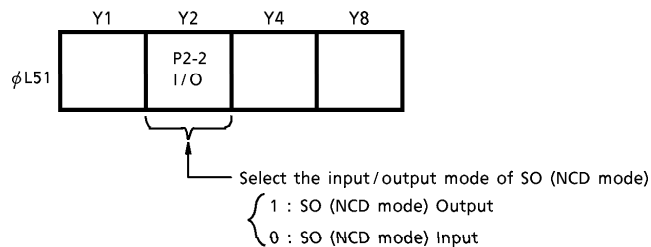
(Note) When executing the SIO input instruction (\overline{NCD} Mode), C_8 bit Code No. becomes "0".

● NCD mode input timing



At time of serial input in the NCD Mode, STB output and SO output are always fixed at "L" level. SI data is input synchronizing with the all timing of CK signal.

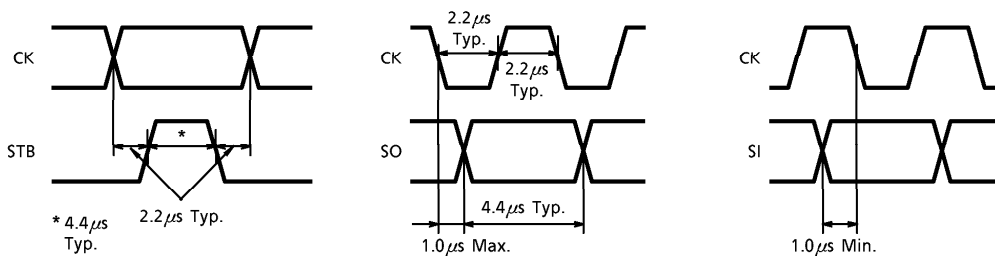
(Note) In NCD mode, SO terminal becomes data I/O structure. It must be set the data "0" to PORT2-2 I/O CONTROL bit before executing SIO input instruction (NCD mode) and SO terminal is set to input mode.



At SIO (NCD mode) input mode, set to the data "0" in advance.

3. Serial timing pulse width

Pulse width of each timing signal is shown below.



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	-0.3~6.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	400	mW
Operation Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = -40~85°C, V_{DD} = 4.5~5.5V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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CPU operation / PLL stop

Operating Power Supply Voltage Range	V _{DD1}	—	PLL Stop / CPU Operation	3.5	5.0	5.5	V
Memory Holding Voltage Range	V _{HD}	—	Cristal oscillation stop	2.0	~	5.5	V
Operating Power Supply Current	I _{DD1}	—	PLL Stop / CPU Operation V _{DD} = 5V, Ta = 25°C	—	0.7	1.5	mA
Memory Holding Power Supply Circuit	I _{HD1}	—	V _{DD} = 5V, Cristal oscillation stop	—	0.1	10	μA
	I _{HD2}	—	V _{DD} = 2V, Cristal oscillation stop	—	—	5	
Crystal Oscillation Frequency	f _{XT}	—	—	—	7.2	—	MHz

CPU / PLL operation

Operating Power Supply Voltage Range	V _{DD2}	—	CPU / PLL Operation	4.5	5.0	5.5	V
Operating Power Supply Current	I _{DD2}	—	CPU / PLL Operation (FM _{IN} = 140MHz), V _{DD} = 5V Ta = 25°C	—	10	25	mA

PLL operating frequency range

FM _{IN} (FM _H Mode)	f _{FMH}	—	V _{IN} = 0.5V _{p-p}	30	~	185	MHz
FM _{IN} (FM _L Mode)	f _{FML}	—	V _{IN} = 0.3V _{p-p}	30	~	140	MHz
AM _{IN} (HF Mode)	f _{HF}	—	V _{IN} = 0.3V _{p-p}	1	~	40	MHz
AM _{IN} (LF Mode)	f _{LF}	—	V _{IN} = 0.3V _{p-p}	0.5	~	20	MHz
IF _{IN1}	f _{IF1}	—	V _{IN} = 0.3V _{p-p}	0.1	~	20	MHz
IF _{IN2}	f _{IF2}	—	V _{IN} = 0.3V _{p-p}	0.1	~	20	MHz

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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PLL operating input amplitude range

FM _{IN} (FM _H Mode)	V _{IN} (FM _H)	—	f _{IN} = 30~185MHz	0.5	~	V _{DD} - 0.5	V _{p-p}
FM _{IN} (FM _L Mode)	V _{IN} (FM _L)	—	f _{IN} = 30~140MHz	0.3	~	V _{DD} - 0.5	V _{p-p}
AM _{IN} (HF Mode)	V _{IN} (HF)	—	f _{IN} = 1~40MHz	0.3	~	V _{DD} - 0.5	V _{p-p}
AM _{IN} (LF Mode)	V _{IN} (LF)	—	f _{IN} = 0.5~20MHz	0.3	~	V _{DD} - 0.5	V _{p-p}
IF _{IN1}	V _{IN} (IF _{IN1})	—	f _{IN} = 0.1~20MHz	0.3	~	V _{DD} - 0.5	V _{p-p}
IF _{IN2}	V _{IN} (IF _{IN2})	—	f _{IN} = 0.1~20MHz	0.3	~	V _{DD} - 0.5	V _{p-p}

P1-1~P1-4, P2-1~P2-4 (SO, CK, STB), P3-1~P3-3, P4-1~P4-4, T0~T7, OT1~OT4 output port

Output Current	"H" Level	I _{OH1}	—	V _{OH} = 4.5V, V _{DD} = 5V	-1.0	-3.0	—	mA
	"L" Level	I _{OL1}	—	V _{OL} = 0.5V, V _{DD} = 5V	1.0	3.0	—	

P5-1~P5-4, P6-1~P6-4, P7-1~P7-4, P8-1~P8-2 port

Output Current	"H" Level	I _{OH2}	—	V _{OH} = 4.5V, V _{DD} = 5V	-0.1	-3.0	—	mA
	"L" Level	I _{OL2}	—	V _{OL} = 0.5V, V _{DD} = 5V	2.5	7.5	—	

INH input port

INH Input Voltage	"H" Level	V _{IH2}	—	—	V _{DD} × 0.85	~	V _{DD}	V
	"L" Level	V _{IL2}	—	—	0	~	V _{DD} × 0.4	
Input Leak Current	"H" Level	I _{IH1}	—	V _{IH} = V _{DD} = 5.5V	—	—	2	μA
	"L" Level	I _{IL1}	—	V _{IL} = 0V, V _{DD} = 5.5V	—	—	2	

Key input port (K0~K3)

Input Voltage	"H" Level	V _{IH1}	—	—	V _{DD} × 0.7	~	V _{DD}	V
	"L" Level	V _{IL1}	—	—	0	~	V _{DD} × 0.3	
Pull-down Resistance	R _{IN1}	—	—	V _{IH} = V _{DD} = 5V Ta = 25°C	50	100	200	kΩ

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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\overline{IN} , IN1, IN2, P1-1~P1-4, P2-1~P2-4 (SI, SO), P3-1~P3-3, P4-1~P4-4 port

Input Voltage	"H" Level	V _{IH1}	—	—	V _{DD} × 0.7	~	V _{DD}	V
	"L" Level	V _{IL1}	—	—	0	~	V _{DD} × 0.3	
Input Leak Current	"H" Level	I _{IH1}	—	V _{IH} = V _{DD} = 5.5V	—	—	2	μA
	"L" Level	I _{IL1}	—	V _{IL} = 0V, V _{DD} = 5.5V	—	—	2	

P5-1~P5-4, P6-1~P6-4, P7-1~P7-4, P8-1~P8-2 port

Input Voltage	"H" Level	V _{IH3}	—	—	V _{DD} × 0.7	~	V _{DD}	V
	"L" Level	V _{IL3}	—	—	0	~	V _{DD} × 0.12	
Input Leak Current	"H" Level	I _{IH1}	—	V _{IH} = V _{DD} = 5.5V	—	—	2	μA
	"L" Level	I _{IL1}	—	V _{IL} = 0V, V _{DD} = 5.5V	—	—	2	

DO1, DO2 outputs

Output Current	"H" Level	I _{OH1}	—	V _{OH} = 4.5V, V _{DD} = 5V	-1.0	-3.0	—	mA
	"L" Level	I _{OL1}	—	V _{OL} = 0.5V, V _{DD} = 5V	1.0	3.0	—	
Tri-State Leak Current		I _{TL}	—	V _{TLH} = V _{DD} = 5.5V V _{TLL} = 0V	—	—	±1	μA

A/D, D/A converter (DC-REF, A/D_{IN1}, A/D_{IN2}, D/A_{OUT})

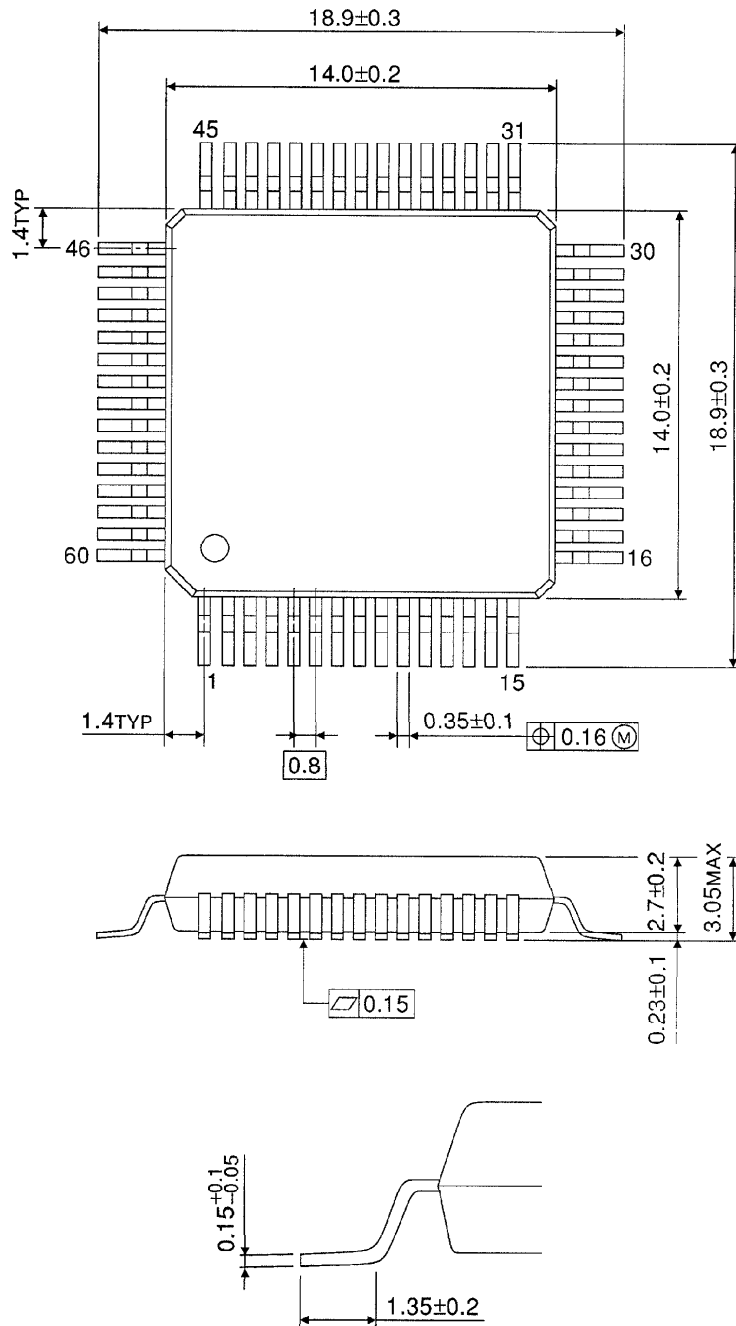
Analogue Input Voltage Range	V _{ADI}	—	AD _{IN1} , AD _{IN2}	0	~	V _{DD}	V
Analogue Reference Voltage Range	V _{REF}	—	DC-REF	1.5	~	V _{DD}	V
Resolution	V _{RES}	—	—	—	—	6	bit
Analogue Reference Voltage Input Current	I _{REF}	—	DC-REF, T _a = 25°C V _{IH} = V _{DD} = 5V	—	0.5	1.0	mA
Analogue Output Voltage Range	V _{DAO}	—	DA _{OUT}	0	~	V _{DD} - 1.0	V
Analogue Output Voltage Deviation	ΔV _{DA}	—	I _{DA} = ±100 μA V _{DD} = 5V, T _a = 25°C	—	±50	±150	mV
Conversion total Error	—	—	—	—	±0.5	±1.5	LSB

Other

FM _{IN} , AM _{IN} , IF _{IN} Input Feedback Resistance	R _{f1}	—	V _{DD} = 5V, T _a = 25°C	250	500	1000	kΩ
X _T Input Feedback Resistance	R _{f2}	—	V _{DD} = 5V, T _a = 25°C	500	1000	2000	kΩ
TEST Input Pull-down Resistance	R _{IN2}	—	V _{IH} = V _{DD} = 5V T _a = 25°C	15	30	60	kΩ

OUTLINE DRAWING
QFP60-P-1414-0.80D

Unit : mm



Weight : 1.10g (Typ.)