

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9322FA, TC9322FB

SINGLE CHIP DTS MICROCONTROLLER (DTS-21)

The TC9322FA and TC9322FB are a 4bit CMOS microcontroller for signal chip digital tuning systems. It is capable of functioning at a low voltage of 3V and features a built-in prescaler of operating 230MHz, PLL and LCD drivers.

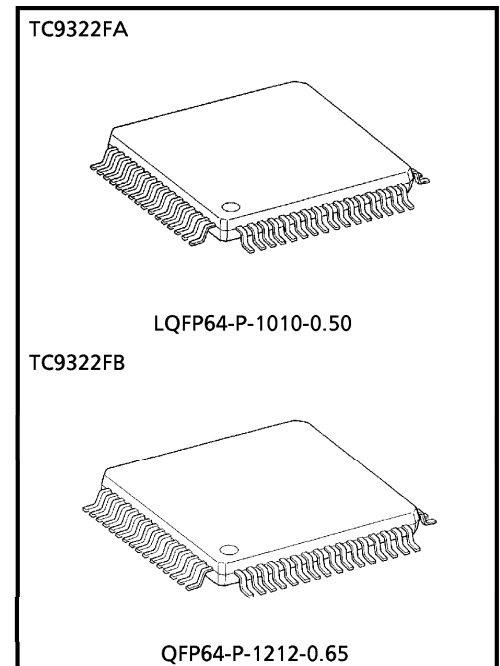
The CPU has 4bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AND), composite judging and compare instructions (e.g., TM, SL), and time-base functions.

The package is an pin 64, 0.5/0.65-mm-pitch quad flat pack package. In addition to various input/output ports and a dedicated key-input port, which are controlled by powerful input/output instructions (IN 1, 2, OUT 1, 2), there are many dedicated LCD pins, a buzzer port, a 6bit A/D converter, an IF counter, and other pins.

Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.

FEATURES

- 4bit microcontroller for digital tuning systems.
- Operating voltage $V_{DD}=1.8\sim 3.6V$, with low current consumption because of CMOS circuitry (with only CPU operating, when $V_{DD}=3V$, $I_{DD}=80\mu A$ Max.)
- Built-in prescaler (1/2 fixed divider +2 modulus prescaler : $f_{max}\geq 230MHz$)
- Features built-in 1/3-duty, 1/2-bias LCD drivers and a built-in 3V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM) : 16bit \times 3072 steps
- Data memory (RAM) : 4bit \times 192 words
- 62-instruction set (all one-word instructions)

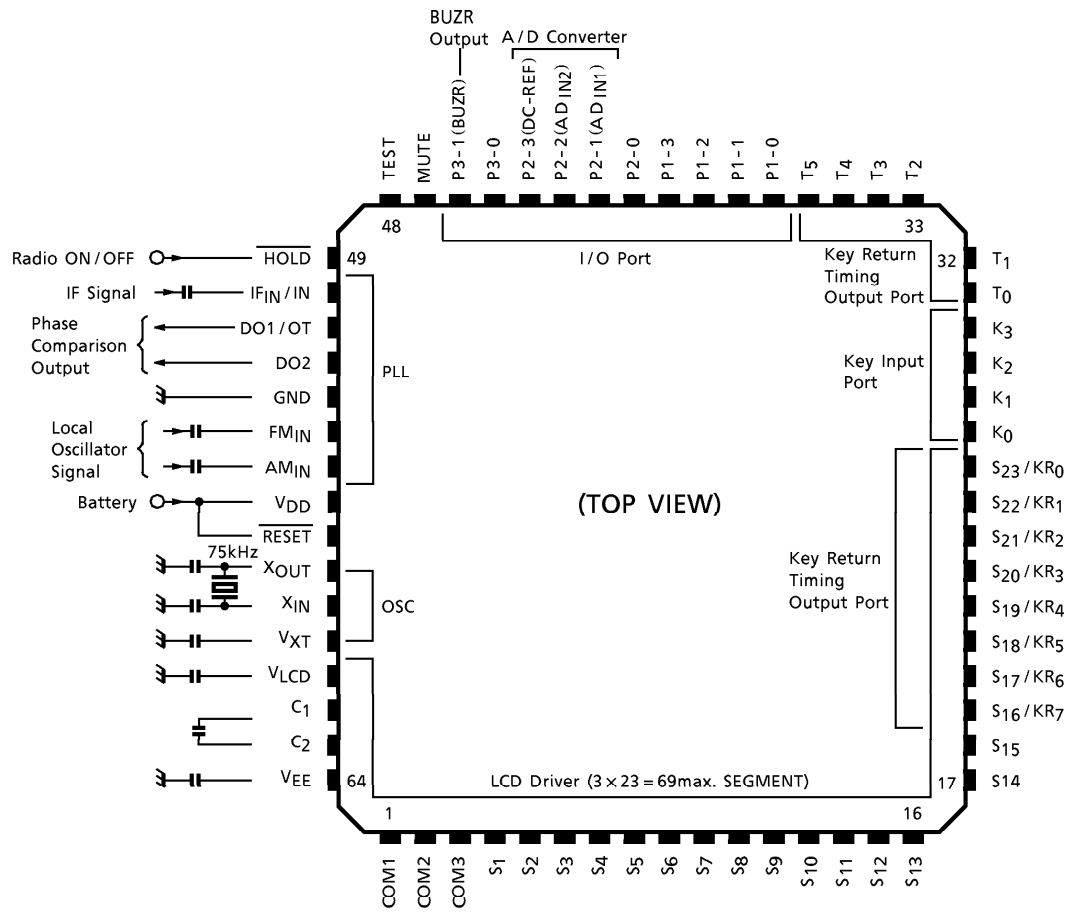


Weight

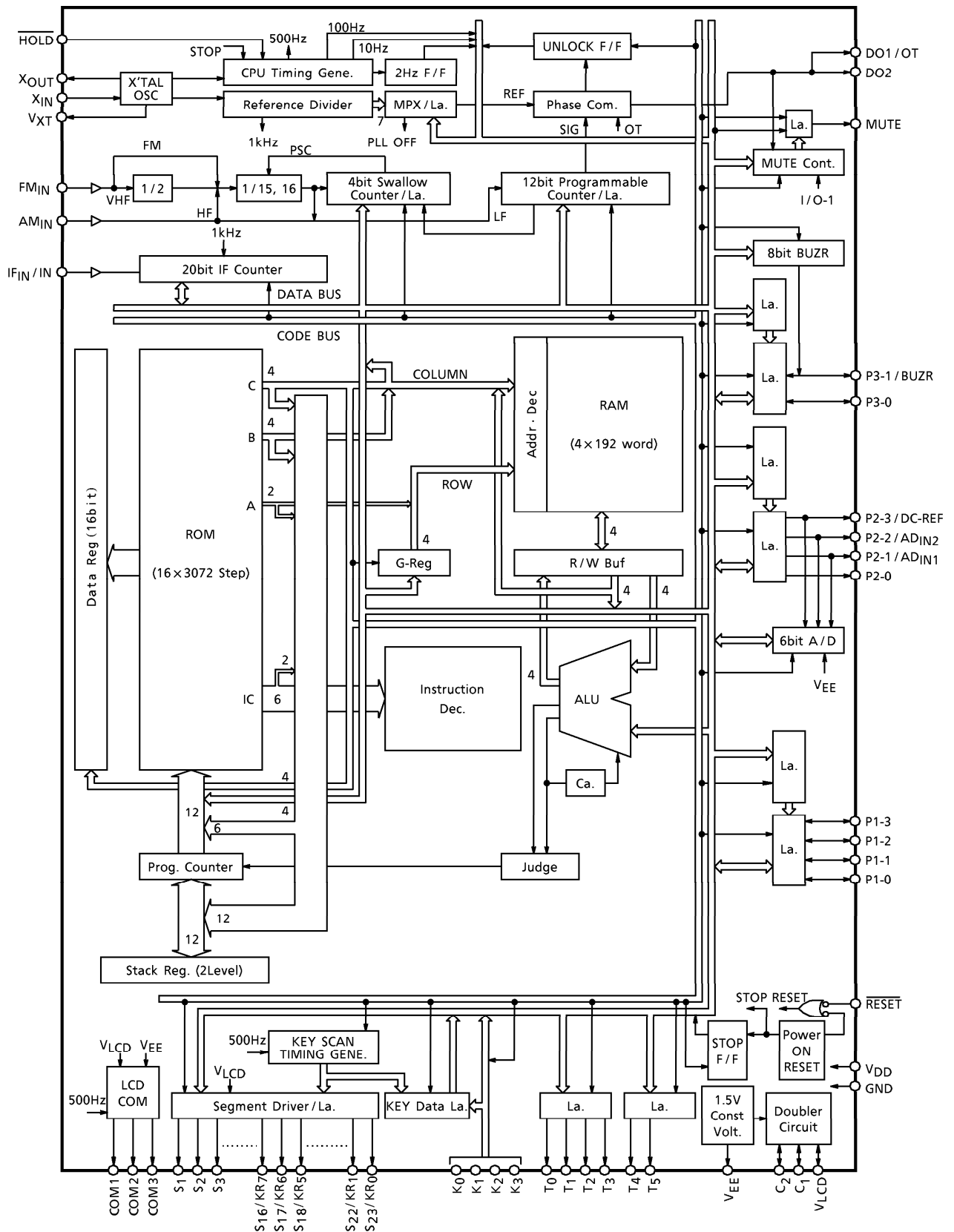
LQFP64-P-1010-0.50 : 0.32g (Typ.)
 QFP64-P-1212-0.65 : 0.45g (Typ.)

- Instruction execution time : 40 μ s (with 75kHz crystal) (MVGS, DAL instructions : 80 μ s)
- Many addition and subtraction instructions (12 types addition, 12 types subtraction)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row. (MVSR instruction)
- Register indirect transfer available (MVG D, MVGS instruction).
- 16 powerful general registers (located in RAM)
- Stack levels : 2
- JUMP or CAL instruction can be used anywhere in the 3072 steps of program memory (ROM) as there are no pages or fields.
- 16bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Features independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparison outputs for FM/VHF and AM.
- Seven reference frequencies can be selected by program.
- Powerful input/output instructions (IN 1, 2, OUT 1, 2)
- Dedicated input ports (K₀~K₃) for key input. 26 LCD drive pins (69 segments maximum) available.
- 17 I/O ports : 10 with input/output programmable in 1bit units, and 7 output-only port. The 2 IF_{IN}, and DO1 pins can be switched by instruction to IN (input-only) or OT (output-only).
- Three back-up modes available by instruction : only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2Hz timer F/F and a built-in 10/100Hz interval pulse output (internal port for time base).
- Allows PLL lock status detection.
- 8 of the LCD segment outputs (S₁₆~S₂₃) can also operate as key return timing outputs (KR₀~KR₇). The I/O ports are not dedicated key return timing outputs but can have other uses as well.
- Built-in 20bit, general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8bit buzzer output circuit can produce 254 different tone signals.
- Features a built-in 2-channel, 6bit A/D converter.
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5V.

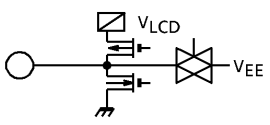
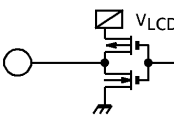
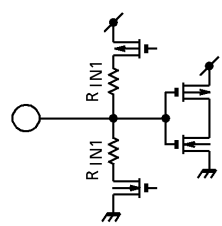
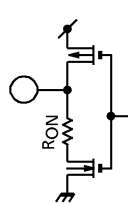
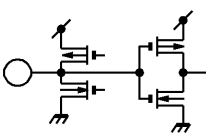
PIN CONNECTION

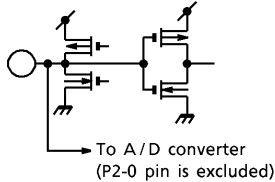
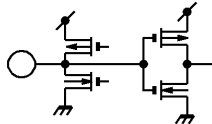
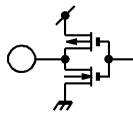
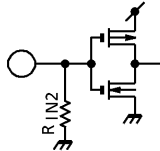


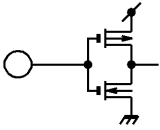
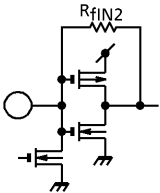
BLOCK DIAGRAM

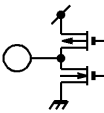
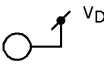


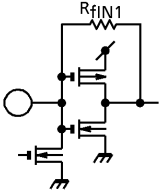
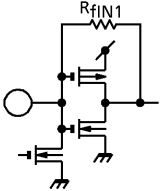
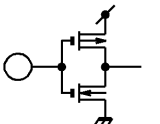
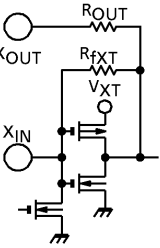
EXPLANATION OF FUNCTION

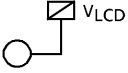
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	COM1	LCD common output	Output common signals to the LCD panel. Through a matrix with pins S ₁ ~S ₂₃ , a maximum of 69 segments can be displayed.	
2	COM2		Three levels, V _{LCD} , V _{EE} , and GND, are output at 83Hz every 2ms.	
3	COM3		V _{EE} is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0".	
4~18	S ₁ ~S ₁₅	LCD segment output	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 69 segments.	
19~26	S ₁₆ /KR ₇ S ₂₃ /KR ₀	LCD segment output/Key return timing output	The signals for the key matrix and the segment signals from pins S ₁₆ /KR ₇ ~S ₂₃ /KR ₀ are output on a time division basis. 4×8=32 key matrix can be created in conjunction with key input ports K ₀ ~K ₃ .	
27~30	K ₀ ~K ₃	Key input ports	4bit input ports for key matrix input. Combined in a matrix with key return timing outputs of the LCD segment pins, data from a maximum of 4×8=32 keys can be input and pins are pulled up. On the key setetuning output pins, data from 4×6=24 keys can be input and pins are pulled down. The WAIT mode is released when high level is applied to key input ports set to pull-down.	
31~36	T ₀ ~T ₅	Key return timing output port	These ports output the timing signal for key matrix. To form the key matrix, load resistance has been built-in the N-channel side. When the key matrix combined with push-key, that does not need a key matrix diode.	
37~40	P1-0 P1-3	I/O port 1	The input and output of these 4bit I/O ports can be programmed in 1bit units. By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1".	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
41~44	P2-0 P2-1/ ADIN1 P2-2/ ADIN2 P2-3/ DC-REF	I/O port 2 /AD analog voltage input /AD analog voltage input /Reference voltage input	4bit I/O ports. Input and output may be programmed in 1bit units. Pins P2-1 through P2-2 can also be used for analog input to the built-in 6bit, 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280 μ s. The necessary pin can be programmed to AD analog input in 1bit units, and P2-3 can be set to the reference voltage input. Internal power supply (V _{DD}) or constant voltage (V _{EE}) can be used as the reference voltage. In addition, constant voltage (V _{EE}) can be input to the AD analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance. The A/D converter, and their control are all executed by program.	
45~46	P3-0 P3-1/ BUZR	I/O port 3 /Buzzer output	2bit I/O ports, whose input/output can be programmed in 1bit units. The P3-1 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75kHz and 147Hz, and at a duty of 50%. The buzzer output, and all associated controls can be programmed.	
47	MUTE	Muting output port	1bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed ; PLL phase difference can also be output using this pin.	
48	TEST	TEST mode control input	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (A pull-down resistor is built-in).	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
49	$\overline{\text{HOLD}}$	HOLD mode control input	<p>Input pin for request/release HOLD mode.</p> <p>Normally, this pin is used to input radio mode selection signals or battery detection signals.</p> <p>HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the HOLD pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the level of the $\overline{\text{HOLD}}$ pin level in MODE-1.</p> <p>When memory back-up mode is entered by executing a WAIT instruction, any change in the HOLD pin input releases the mode.</p> <p>In memory back-up mode, current consumption is low (below $10\mu\text{A}$), and all the output pins (e.g., display output, output ports) are automatically set to low level.</p>	
50	IF _{IN} /IN	IF signal input / Input port	<p>IF counter's IF signal input pin for counting the IF signals of the FM and AM bands and detecting the automatic stop position.</p> <p>The input frequency is between 0.35~12MHz (0.2V_{p-p} (Min)). A built-in input amp and C coupling allow operation at low-level input.</p> <p>The IF counter is a 20bit counter with optional gate times of 1, 4, 16, and 64ms. 20 bits of data can be readily stored in memory.</p> <p>This input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port.</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
51	DO1/OT	Phase comparison output / Output port	PLL's phase comparison tri-state output pins. When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus, the pins can be used to improve lock-up time or used as output ports.	
52	DO2			
56	VDD	Power-supply pins	Pins to which power is applied. Normally, $V_{DD} = 1.8\sim 3.6V$ (3.0V Typ.) is applied. In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0V. If voltage falls below 1.5V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5V, the CPU restarts. STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (Power on reset) (Note) To operate the power on reset, the power supply should start up in 10~100ms.	
53	GND			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
54	FM _{IN}	FM programmable counter input	<p>Programmable counter input pin for FM, VHF band.</p> <p>The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are selectable freely by program.</p> <p>At the VHF mode, local oscillation output (VCO output) of 50~230MHz (0.2V_{p-p} (Min)) is input and FM mode, 40~130MHz (0.2V_{p-p} (Min)) is input.</p> <p>A built-in input amp and C coupling allow operation at low-level input.</p> <p>(Note) When in the PLL OFF mode or when set to AM_{IN} input, the input is pulled down.</p>	
55	AM _{IN}	AM local oscillator signal input	<p>Programmable counter input pin for AM band.</p> <p>The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1~45MHz (0.2V_{p-p} (Min)) is input and LF mode, 0.5~12MHz (0.2V_{p-p} (Min)) is input.</p> <p>Built-in input amp operates with low-level input using a C coupling.</p> <p>(Note) When in PLL OFF mode or when set to FM_{IN} input, the input is pulled down.</p>	
57	RESET	Reset input	<p>Input pin for system reset signals.</p> <p>RESET takes place while at low level ; at high level, the program starts from address "0".</p> <p>Normally, if more than 1.8V is supplied to V_{DD} when the voltage is 0, the system is reset (Power on reset).</p> <p>Accordingly, this pin should be set to high level during operation.</p>	
58	X _{OUT}	Crystal oscillator pins	<p>Crystal oscillator pins.</p> <p>A reference 75kHz crystal oscillator is connected to the X_{IN} and X_{OUT} pins.</p> <p>The oscillator stops oscillating during CKSTP instruction execution.</p> <p>The V_{X_T} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47μF Typ.) is connected.</p>	
59	X _{IN}			
60	V _{X_T}			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
61	V _{LCD}	Voltage doubler boosting pin	Voltage doubler boosting pin for driving the LCD. A capacitor (0.1 μ F Typ.) is connected to boost the voltage. The V _{LCD} pin outputs voltage (3.0V), which has been doubled from the constant voltage (V _{EE} : 1.5V) using the capacitors connected between C ₁ and C ₂ . That potential is supplied to the LCD drivers. If the internal V _{LCD} OFF bit is set to "1" by program, an external power supply can be input through the V _{LCD} pin to drive the LCD. At this time, the V _{LCD} /2 potential, whose V _{LCD} voltage is divided using registers, is output from the C ₂ pin.	
62	C ₁			
63	C ₂			
64	V _{EE}	Constant voltage supply pin	1.5V constant voltage supply pin for driving the LCD. A stabilizing capacitor (0.1 μ F Typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.	—

- (Note 1) When the device is reset (voltage higher than 1.8V, or when $\overline{\text{RESET}} = \text{low} \rightarrow \text{high}$) I/O ports are set to input, the pins for I/O ports and additional functions (e.g., A/D converter) are set to I/O port input pins, while the IF_{IN}/IN pins become IF input pins.
- (Note 2) When in PLL OFF mode (when the three bits in the internal reference ports all show "1"), the IF_{IN} and FM_{IN}, AM_{IN} pins are pulled down, and DO1 and DO2 are at high impedance.
- (Note 3) When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports and the LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{X_T}) are all off.
- (Note 4) When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~4.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	100	mW
Operating Temperature	T _{opr}	-10~60	°C
Storage Temperature	T _{stg}	-55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Range Of Operating Supply Voltage	V _{DD}	—	*	1.8	3.0	3.6	V
Range Of Memory Retention Voltage	V _{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) *	1.0	~	3.6	
Operating Current	I _{DD1}	—	Under ordinary operation and PLL on operation, no output load V _{DD} = 3.0V FM _{IN} = 230MHz input	—	7.0	12	mA
			Under ordinary operation and PLL on operation, no output load V _{DD} = 3.0V FM _{IN} = 130MHz input	—	6.0	10	
	I _{DD2}	—	Under CPU operation only (PLL off, display turned on) V _{DD} = 3.0V	—	40	80	μA
	I _{DD3}	—	Soft Wait mode (Crystal oscillator, display circuit operating, CPU stopped, PLL off)	—	25	50	
	I _{DD4}	—	Hard Wait mode (Crystal oscillator operating only)	—	15	30	
Memory Retention Current	I _{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	10	
Crystal Oscillation Frequency	f _{XT}	—	*	—	75	—	kHz
Crystal Oscillation Startup Time	t _{ST}	—	Crystal oscillation f _{XT} = 75kHz	—	—	1.0	s

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6V, Ta = -10~60°C.

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Voltage doubler circuit

Voltage Doubler Reference Voltage	V_{EE}	—	GND reference (V_{EE})	1.3	1.5	1.7	V
Constant Voltage Temperature Characteristics	D_V	—	GND reference (V_{EE})	—	-5	—	mV/°C
Voltage Doubler Boosting Voltage	V_{LCD}	—	GND reference (V_{LCD})	2.6	3.0	3.4	V

Operating frequency ranges for programmable counter and IF counter

FM_{IN} (VHF Mode)	f_{VHF}	—	Sine wave input when $V_{IN} = 0.2V_{p-p}$ *	50	~	230	MHz
FM_{IN} (FM Mode)	f_{FM}	—	Sine wave input when $V_{IN} = 0.2V_{p-p}$ *	40	~	130	
AM_{IN} (HF Mode)	f_{HL}	—	Sine wave input when $V_{IN} = 0.2V_{p-p}$ *	1	~	45	
AM_{IN} (LF Mode)	f_{LF}	—	Sine wave input when $V_{IN} = 0.2V_{p-p}$ *	0.5	~	12	
IF_{IN}	f_{IF}	—	Sine wave input when $V_{IN} = 0.2V_{p-p}$ *	0.35	~	12	
Input Amplitude	V_{IN}	—	FM_{IN} , AM_{IN} , IF_{IN} input *	0.2	~	$V_{DD} - 0.8$	V_{p-p}

LCD common output / segment output (COM1~COM3, S1~S23)

Output Current	"H" Level	I_{OH1}	—	$V_{LCD} = 3V$, $V_{OH} = 2.7V$	-0.5	-1.0	—	mA
	"L" Level	I_{OL1}	—	$V_{LCD} = 3V$, $V_{OL} = 0.3V$	0.5	1.0	—	
Output Voltage 1/2 Level	V_{BS}	—	No load	1.3	1.5	1.7	V	

HOLD input port

Input Leak Current	I_{LI}	—	$V_{IH} = 3.0V$, $V_{IL} = 0V$	—	—	± 1.0	μA	
Input Voltage	"H" Level	V_{IH1}	—	—	2.4	~	3.0	V
	"L" Level	V_{IL1}	—	—	0	~	1.2	

A/D converter (A/D_{IN1} , A/D_{IN2} , DC-REF)

Analog Input Voltage Range	V_{AD}	—	AD_{IN1} , AD_{IN2}	0	~	V_{DD}	V
Analog Reference Voltage Range	V_{REF}	—	DC-REF, $V_{DD} = 2.0 \sim 3.6V$	1.0	~	$V_{DD} \times 0.9$	V
Resolution	V_{RES}	—	—	—	6.0	—	bit
Conversion Total Error	—	—	$V_{DD} = 2.0 \sim 3.6V$	—	± 1.0	± 4.0	LSB
Analog Input Leak	I_{LI}	—	$V_{IH} = 3.0V$, $V_{IL} = 0V$ (AD_{IN1} , AD_{IN2} , DC-REF)	—	—	± 1.0	μA

For conditions marked by an asterisk (*), guaranteed when $V_{DD} = 1.8 \sim 3.6V$, $T_a = -10 \sim 60^\circ C$.

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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KEY input port (K₀~K₃)

N-ch / P-ch Input Resistance	R _{IN1}	—	—	75	150	300	kΩ	
Input Voltage	"H" Level	V _{IH2}	—	When input with pull-down resistance	1.8	~	3.0	V
	"L" Level	V _{IL2}	—	When input with pull-down resistance	0	~	0.3	
Input Voltage	"H" Level	V _{IH3}	—	When input with pull-up resistance	2.7	~	3.0	V
	"L" Level	V _{IL3}	—	When input with pull-up resistance	0	~	1.2	
Input Leak Current	I _{LI}	—	When input resistance off, V _{IH} = 3.0V, V _{IL} = 0V	—	—	± 1.0	μA	

Timing output port (T₀~T₅)

Output Current	"H" Level	I _{OH1}	—	V _{OH} = 2.7V	-0.5	-1.0	—	mA
	"L" Level	I _{OL1}	—	V _{OL} = 0.3V, Use LCD key-return mode	0.5	1.0	—	
N-ch Load Resistance	R _{ON}	—	No used LCD key-return mode	75	150	300	kΩ	

DO1 / OT, DO2 output ; MUTE output

Output Current	"H" Level	I _{OH1}	—	V _{OH} = 2.7V	-0.5	-1.0	—	mA
	"L" Level	I _{OL1}	—	V _{OL} = 0.3V	0.5	1.0	—	
Output Off Leak Current	I _{TL}	—	V _{TLH} = 3.0V, V _{TLL} = 0V (DO1, DO2)	—	—	± 100	nA	

General-purpose I/O ports (P1-0~P3-1)

Output Current	"H" Level	I _{OH1}	—	V _{OH} = 2.7V	-0.5	-1.0	—	mA
	"L" Level	I _{OL1}	—	V _{OL} = 0.3V	0.5	1.0	—	
Input Leak Current	I _{LI}	—	V _{IH} = 3.0V, V _{IL} = 0V	—	—	± 1.0	μA	
Input Voltage	"H" Level	V _{IH4}	—	—	2.4	~	3.0	V
	"L" Level	V _{IL4}	—	—	0	~	0.6	

IN, RESET input port

Input Leak Current	I _{LI}	—	V _{IH} = 3.0V, V _{IL} = 0V	—	—	± 1.0	μA	
Input Voltage	"H" Level	V _{IH4}	—	—	2.4	~	3.0	V
	"L" Level	V _{IL4}	—	—	0	~	0.6	

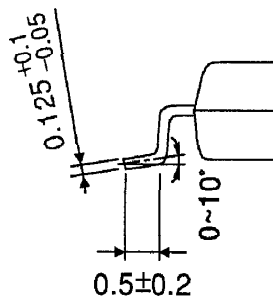
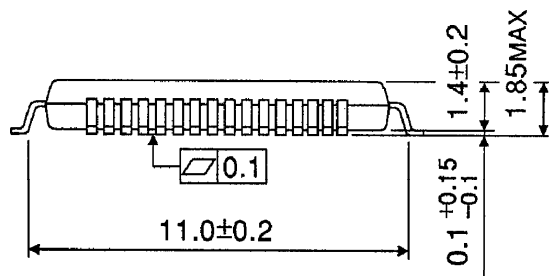
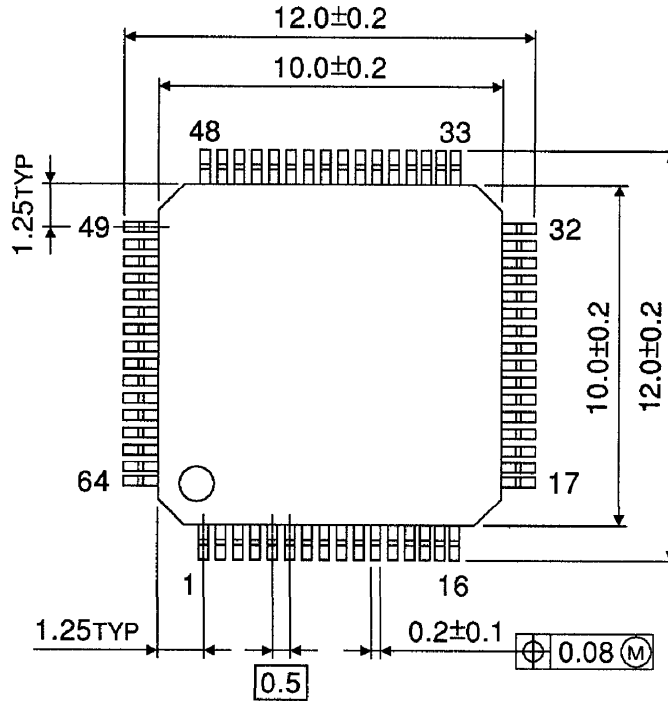
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Others

Input Pull-Down Resistance	R_{IN2}	—	(TEST)	25	50	100	$k\Omega$
X_{IN} Amp Feedback Resistance	R_{fXT}	—	(X_{IN} - X_{OUT})	—	20	—	$M\Omega$
X_{OUT} Output Resistance	R_{OUT}	—	(X_{OUT})	—	3	—	$k\Omega$
Input Amp Feedback Resistance	R_{fIN1}	—	(FM_{IN} , AM_{IN})	150	300	600	$k\Omega$
	R_{fIN2}	—	(IF_{IN})	500	1000	2000	
Voltage Used To Detect Supply Voltage Drop	V_{STP}	—	(V_{DD})	1.3	1.5	1.6	V
Supply Voltage Drop Detection Temperature Characteristics	D_S	—	(V_{DD})	—	-2	—	$mV/^\circ C$

PACKAGE DIMENSIONS
LQFP64-P-1010-0.50

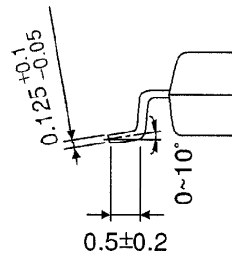
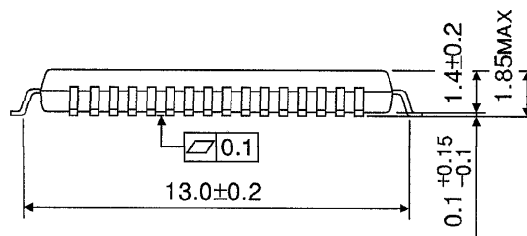
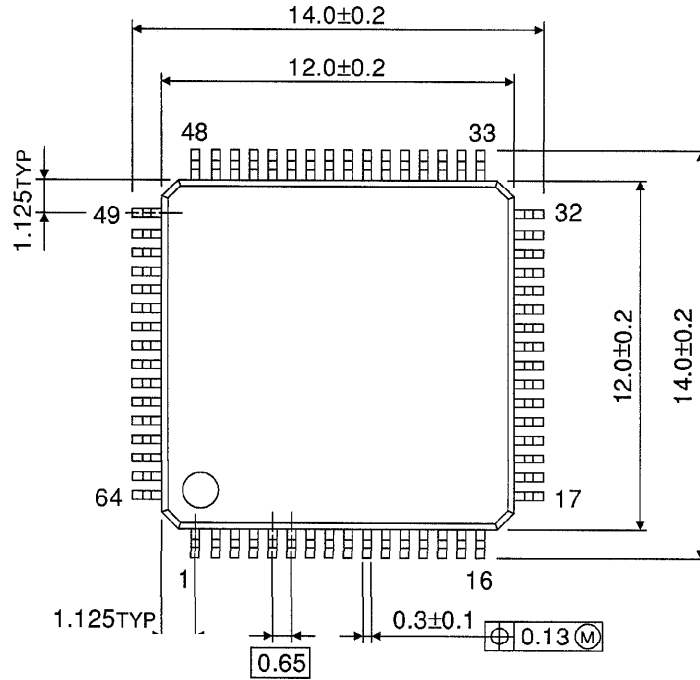
Unit : mm



Weight : 0.32g (Typ.)

PACKAGE DIMENSIONS
QFP64-P-1212-0.65

Unit : mm



Weight : 0.45g (Typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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