

# TC9337F

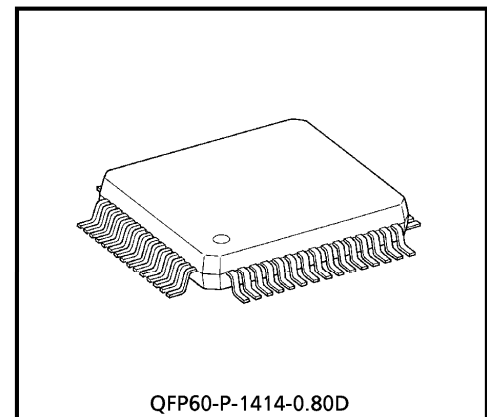
## AUDIO DIGITAL SIGNAL PROCESSOR

The TC9337F has a ROM area that holds application programs for digital filters such as equalizers, for dynamic range control of compressors, and for acoustic field control concert hall simulation. These application programs allow real-time digital processing of audio signals.

Thanks to 64Kbit of built-in data delay (audio field control) RAM, no external RAM is necessary and the built-in voltage-controlled oscillator (VCO) allows easy phase-locked loop configuration.

### FEATURES

- 24bit main bus
- The arithmetic operations block is as follows :
  - Multiplier / adder : 24bit × 16bit + 43bit → 43bit
  - Accumulator : 43bit (code extension 4bit)
  - Logic operator : 24bit (AND, OR, XOR, NOT)
  - Work register : 32bit, 39bit
  - Temporary register : 32bit
  - Shifter : +4bit, +1bit shift
- The structure of the program and internal data memory areas are as follows :
  - Program ROM : 1024 word × 32bit
  - Data RAM : 128 word × 24bit
  - Coefficient RAM : 320 word × 16bit
  - Coefficient ROM : 256 word × 16bit
  - Offset address RAM : 64 word × 16bit
- The following five serial data ports are provided :
  - Serial data input ports : 2 ports (SDI0, SDI1)
  - Serial data output ports : 3 ports (SDO0, SDO1, SDO2)
  - Data word length : 24bit and 16bit
  - Data format : First MSB / LSB (input)  
First MSB (output)
- Built-in RAM for data delay
  - Delay RAM : 64Kbit (4096word × 16bit)
- Built-in VCO circuit.
- Coefficient data and offset data can be set or changed via a I<sup>2</sup>C-bus interface.
- CMOS silicon technology for higher speed.
- 60 pin flat package.



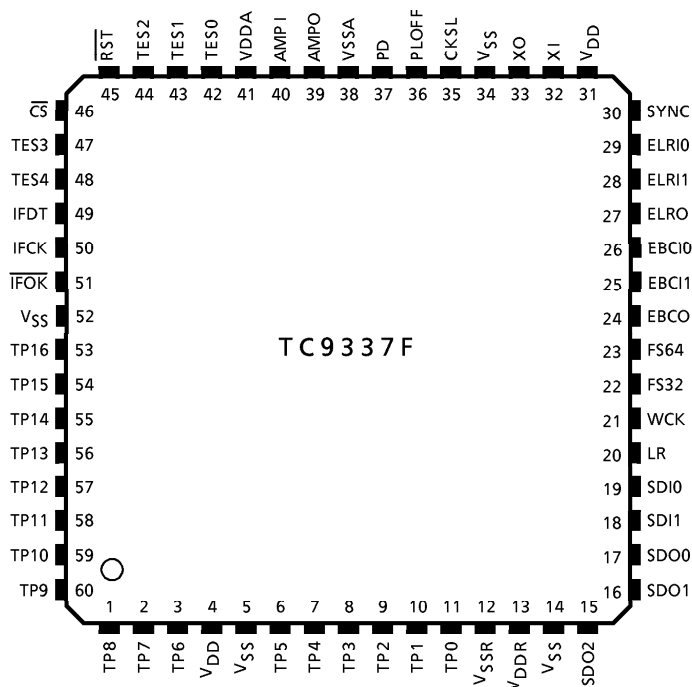
QFP60-P-1414-0.80D

Weight : 1.08g (Typ.)

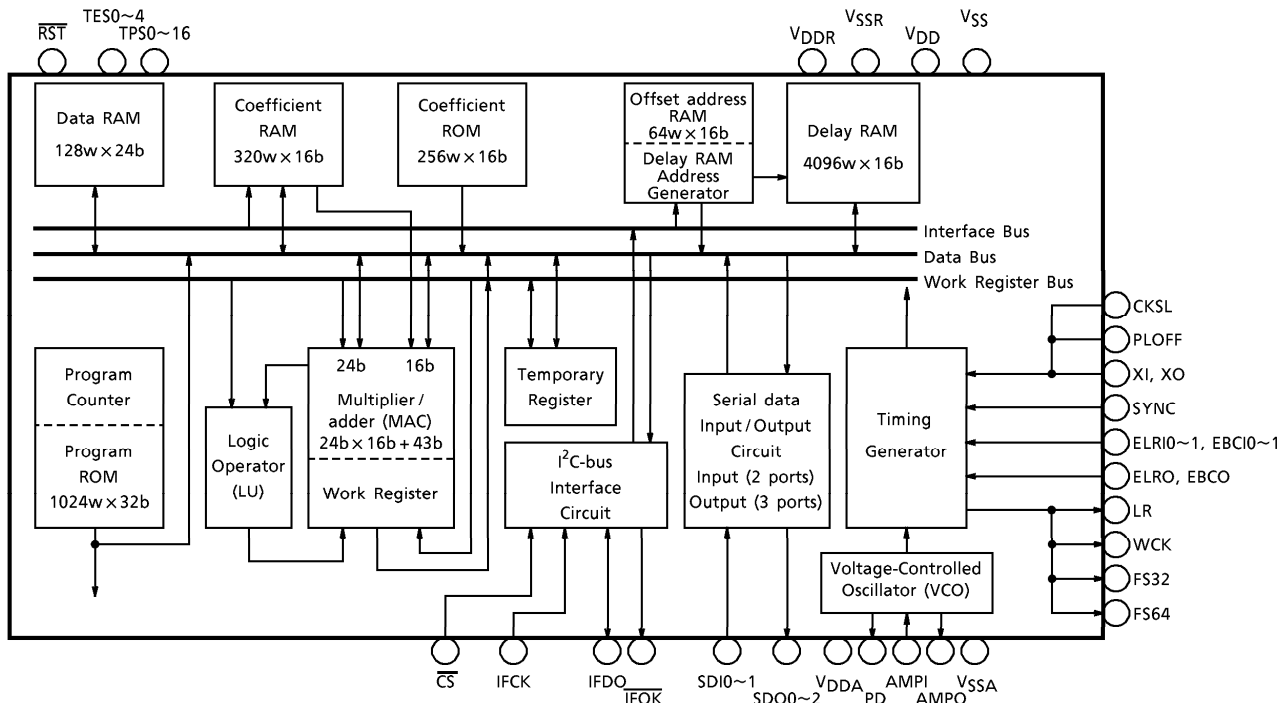
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PIN CONNECTION



BLOCK DIAGRAM



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**PIN FUNCTION**

PIN No.	SYMBOL	I/O	DESCRIPTION OF PIN FUNCTIONS	REMARKS
1 5 3	TP8 5 TP6	O	Test data output terminal, normally open.	—
4	V <sub>DD</sub>	—	Power supply terminal.	—
5	V <sub>SS</sub>	—	Ground terminal.	—
6 5 11	TP5 5 TP0	O	Test data output terminal, normally open.	—
12	V <sub>SSR</sub>	—	Ground terminal for internal delay RAM (DLRAM).	—
13	V <sub>DDR</sub>	—	Power supply terminal for internal delay RAM (DLRAM).	—
14	V <sub>SS</sub>	—	Ground terminal.	—
15	SDO2	O	Serial data output terminal.	—
16	SDO1		Output data length 24bit or 16bit, selectable by microcontroller.	
17	SDO0			
18	SDI1	I	Serial data input terminal.	—
19	SDI0		Input data length 24bit or 16bit, selectable by microcontroller.	
20	LR	O	LR clock output terminal (1fs).	—
21	WCK	O	Word clock output terminal (2fs).	—
22	FS32	O	Bit clock output terminal (32fs).	—
23	FS64	O	Bit clock output terminal (64fs).	—
24	EBC0	I	Bit clock input terminals. Inputs shift clock for SDO0 / 1 / 2 data output.	Schmitt input
25	EBC11	I	Bit clock input terminals. Inputs shift clock for SDI0 / 1 data input.	For SDI1 data input
26	EBC10			For SDI0 data input
27	ELRO	I	LR clock input terminal. Inputs LR clock for SDO0 / 1 / 2 data output.	Schmitt input
28	ELR11	I	LR clock input terminals. Inputs LR clock for SDI0 / 1 data input.	For SDI1 data input
29	ELR10			For SDI0 data input
30	SYNC	I	Synchronous signal input terminal. The synchronous signal forcibly reset the program counter to "zero", and the polarity is set by microcontroller.	Schmitt input
31	V <sub>DD</sub>	—	Power supply terminal.	—
32	XI	I	Crystal oscillator connection terminal / External clock input terminal.	—
33	XO	O	Crystal oscillator connection terminal.	—
34	V <sub>SS</sub>	—	Ground terminal.	—

PIN No.	SYMBOL	I/O	DESCRIPTION OF PIN FUNCTIONS	REMARKS
35	CKSL	I	Clock select terminal. "L" : 384fs "H" : 512fs	Pull-up resistor, Schmitt input
36	PLOFF	I	External oscillation / built-in VCO mode select terminal. "L" : VCO mode "H" : External oscillation mode	Pull-down resistor
37	PD	O	Phase-difference output terminal.	Tri-state output
38	VSSA	—	Analog ground terminal.	—
39	AMPO	O	LPF amplifier output.	—
40	AMPI	I	LPF amplifier input.	—
41	VDDA	—	Analog power supply terminal.	—
42 43 44	TES0 43 TES2	I	Test terminal, normally high or open.	Pull-up resistor, Schmitt input
45	$\overline{RST}$	I	Reset signal input terminal.	Pull-up resistor
46	$\overline{CS}$	I	Chip select signal input terminal : when $\overline{CS}$ is at low active, data can be sent from the microcontroller.	Schmitt input
47	TES3	I	Test terminal, normally high.	Schmitt input
48	TES4	I	Test terminal, normally high or open.	Pull-up resistor, Schmitt input
49	IFDT	I/O	I <sup>2</sup> C-bus data input/output terminal.	Open-drain input / output
50	IFCK	I	I <sup>2</sup> C-bus clock input terminal.	Schmitt input
51	$\overline{IFOK}$	O	Bus monitor permission signal output terminal.	Open-drain output, Pull-up resistor
52	VSS	—	Ground terminal.	—
53 54 60	TP16 54 TP9	O	Test data output terminal, normally open.	—

**DESCRIPTION OF OPERATION**

1. Timing generator

(1) Crystal oscillator

As Figure 1 shows, the clocks required for internal operations can be generated by connecting a crystal oscillator and capacitor. (PLOFF = "H")

As Figure 2 shows, clocks can also be externally input to the XI terminal.

For external clock purposes, a crystal with a good starting potential and low CI value is recommended.

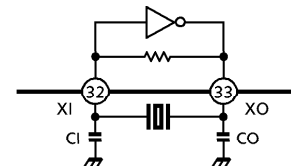


Fig.1 Self-exciting Crystal Oscillation

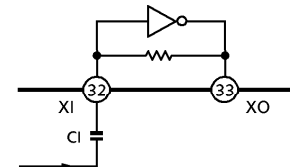


Fig.2 External Clock Input

(2) Voltage-controlled oscillator (VCO)

The clocks required for internal operations are generated by an built-in VCO. The signal input from the SYNC pin is used as a reference. Configure the phase-locked loop as shown in Figure 3. A phase-difference (PD) signal is output from the PD terminal.

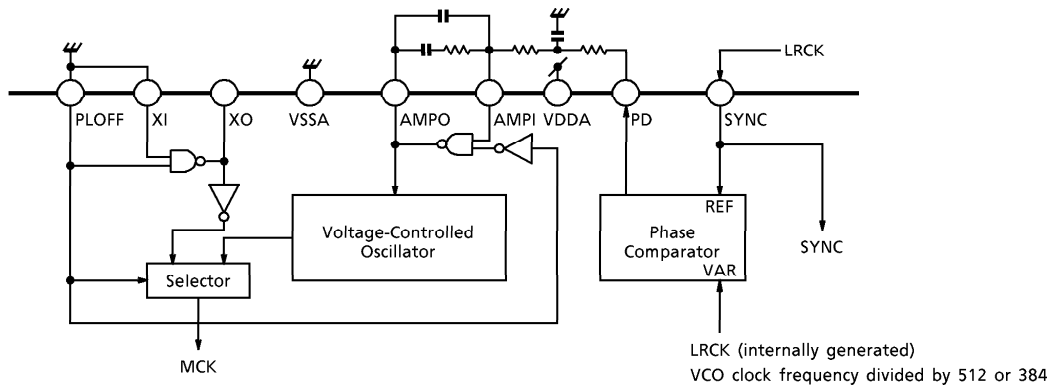


Fig.3 Example of Configuration of a Basic PLL Circuit

(2-1) Phase-difference output

A phase-difference (PD) signal between the REF and VAR signals are output from the PD terminal the PD signal as shown in Figure 4 below.

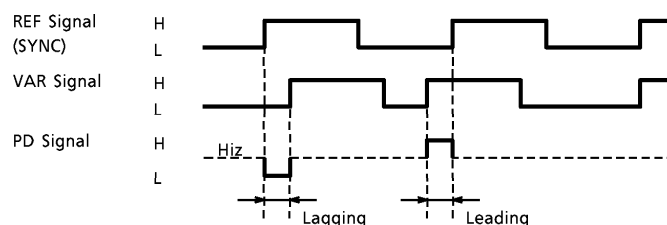


Fig.4 Example of Phase-Difference Output Timing

2. Setting audio data input/output format (data, channel clock, and bit clock)

The 16bit/24bit serial data input/output channel clocks (LR, ELRI0~1 and ELRO0~2) and bit clocks (FS64, FS32, EBCI0~1 and EBCO) can be either internally generated or externally input. The mode setting is effected by the microcontroller interface (control register). Figure 4 shows the data input/output clock pulse selector.

- (1) The channel clock, bit clock and data format for data inputs SDI0~1 are selected by LRIS0~1, BCIS0~1 and SIFMT0~1 of control register 2 (CNT-R2). Table 1 (a) and (b) show setting modes for data inputs SDI0~1.

Table 1 (a) Setting Modes for Data Input SDI0

CONTROL REGISTER 2 (CNT-R2)			FORMAT FOR DATA INPUT SDI0			
LRIS0	BCIS0	SIFMT0	DATA	BIT CLOCK	CHANNEL CLOCK	DATA FORMAT
0	0	0	16bit	32fs (FS32 terminal) Internally generated	LR terminal Internally generated	MSB first
0	0	1				LSB first
0	1	0	24bit	64fs (FS64 terminal) Internally generated	LR terminal Internally generated	MSB first, effective data before the change point of LRCK
0	1	1				LSB first, effective data before the change point of LRCK
1	0	0	16bit	32fs (EBCI0 terminal) Externally input terminal	ELRI0 terminal Externally input terminal	MSB first
1	0	1				LSB first
1	1	0	24bit	48 / 64fs (EBCI0 terminal) Externally input terminal	ELRI0 terminal Externally input terminal	MSB first, effective data before the change point of LRCK
1	1	1				LSB first, effective data before the change point of LRCK

Table 1 (b) Setting Modes for Data Input SDI1

CONTROL REGISTER 2 (CNT-R2)			FORMAT FOR DATA INPUT SDI1			
LRIS1	BCIS1	SIFMT1	DATA	BIT CLOCK	CHANNEL CLOCK	DATA FORMAT
0	0	0	16bit	32fs (FS32 terminal) Internally generated	LR terminal Internally generated	MSB first
0	0	1				LSB first
0	1	0	24bit	64fs (FS64 terminal) Internally generated	LR terminal Internally generated	MSB first, effective data before the change point of LRCK
0	1	1				LSB first, effective data before the change point of LRCK
1	0	0	16bit	32fs (EBCI1 terminal) Externally input terminal	ELRI1 terminal Externally input terminal	MSB first
1	0	1				LSB first
1	1	0	24bit	48 / 64fs (EBCI1 terminal) Externally input terminal	ELRI1 terminal Externally input terminal	MSB first, effective data before the change point of LRCK
1	1	1				LSB first, effective data before the change point of LRCK

- (2) The channel clock, bit clock and data format for data outputs SDO0~2 are selected by LROS0~2, BCOS02 and SOFMT0~1 of control register 2 (CNT-R2).  
 Table 2 (a), (b), and (c) show setting modes for data outputs SDO0-2.

Table 2 (a) Setting Modes for Data Output SDO0

CONTROL REGISTER					FORMATS FOR DATA OUTPUT SDO0				
CNT-R2				CNT-R1	DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS0	BCOS0	SOFMT0	LROS2	EBCS					
0	0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCIO (64fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24bit	48fs			MSB first, effective data after the change point of LRCK
						64fs			
1	*	1	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24bit	64fs			

\* : Don't care

(Note) Clock output from LR terminal is input to ELRO terminal.

Table 2 (b) Setting Modes for Data Output SDO1

CONTROL REGISTER					FORMATS FOR DATA OUTPUT SDO1				
CNT-R2			CNT-R1		DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS1	BCOS1	SOFMT1	LROS2	EBCS					
0	0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCI0 (64fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24bit	48fs			MSB first, effective data after the change point of LRCK
						64fs			
1	*	1	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24bit	64fs			

Table 2 (c) Setting Modes for Data Output SDO2

CONTROL REGISTER				FORMATS FOR DATA OUTPUT SDO2				
CNT-R2			CNT-R1	DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS2	BCOS2	LROS2	EBCS					
0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCI0 (64fs)		ELRO terminal Internally generated	MSB first
*	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated (Note)	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
				24bit	48fs			MSB first, effective data after the change point of LRCK
					64fs			
1	*	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
				24bit	64fs			

\* : Don't care

(Note) Clock output from LR terminal is input to ELRO terminal.



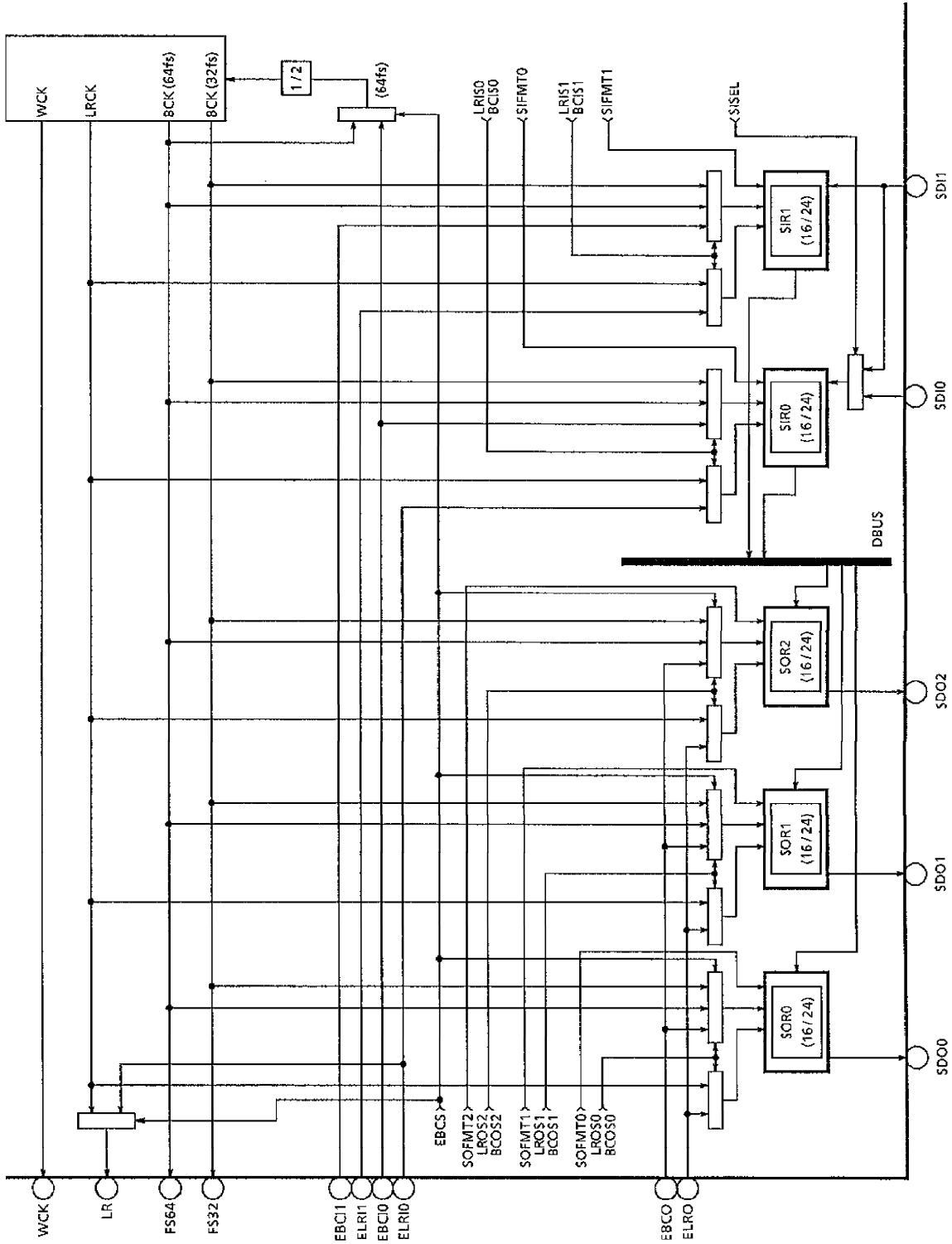


Fig.5 Data Input/Output Clock Selector

## 2. Data input and output circuits

### (1) Data input circuits

#### (1-1) Data input

Data are input in twos complement form, MSB first or LSB first, effective data before the change point of LRCK.

Input registers SIR0 and SIR1 are selectable for either 16bit or 24bit data length. The channel clock (LRCK) and bit clock (BCK) signals can be externally input independently as the timing signals for the data input to registers SIR0 and SIR1.

Mode using internally generated LRCK and BCK signals is also provided.

Input data are fetched by sensing the rise and fall of LRCK.

Input register SIR0 can select between input data SDI0 and SDI1 using the control registers of the microcontroller interface.

#### (1-2) Data input formats

- When input data are 16bit/channel, see Figure 6 (a).  
When BCK is 32fs, input is MSB first or LSB first.
- When input data is 24bit/channel, see Figures 6 (b) and 6 (c).  
When BCK is 48fs (external input), input is MSB first or LSB first.  
When BCK is 64fs, input is MSB first or LSB first, with effective data before the change point of LRCK.

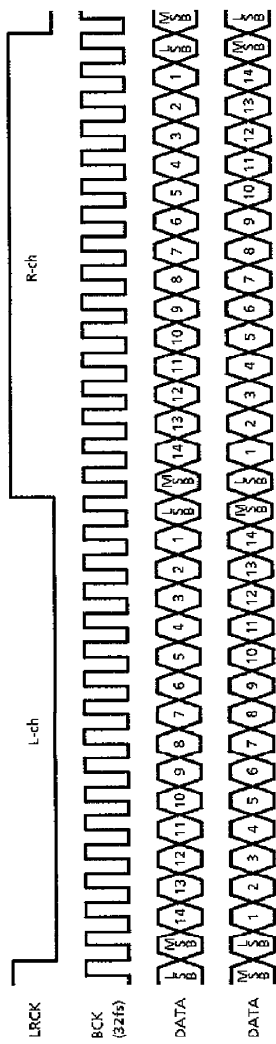


Fig.6 (a) 16bit Data Input Format

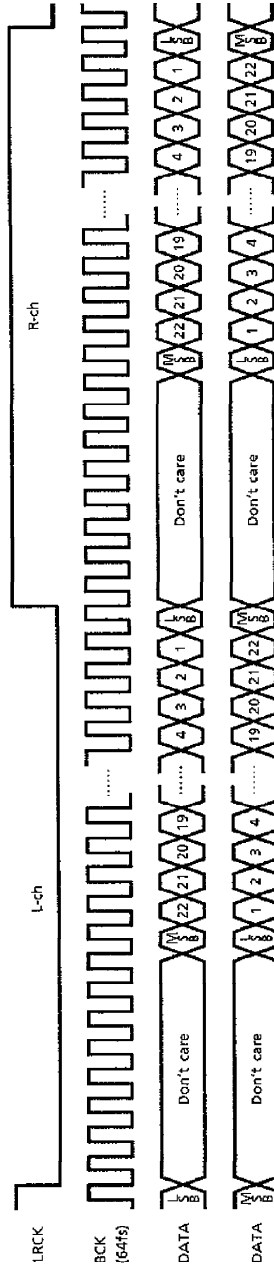


Fig.6 (b) 24bit Data Input Format

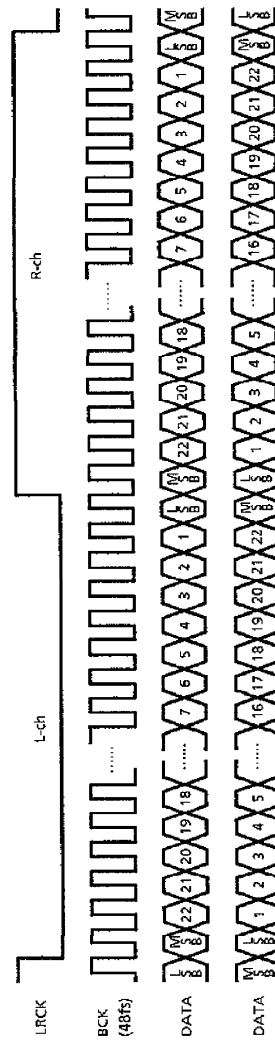


Fig.6 (c) 24bit Data Input Format

## (2) Data output circuits

### (2-1) Data output

Data are output in twos complement form, MSB first, with effective data after the change point of LRCK or 8 clock shift with effective data before the change point of LRCK.

Output registers SOR0, SOR1 and SOR2 are selectable for either 16bit or 24bit data.

The channel clock (LRCK) and bit clock (BCK) signals can be externally input independently as the timing signals for the data output to registers SOR0, SOR1 and SOR2.

Mode using internally generated LRCK and BCK signals is also provided.

Input data are output to registers SOR0, SOR1 and SOR2 by sensing the rise and fall of LRCK.

Output register SIR0 can select between output data SDI0 and SDI1 using the control registers of the microcontroller interface.

### (2-2) Data output formats

16bit or 24bit data are output from the data bus starting from the MSB.

- When output data are 16bit/channel, see Figure 7 (a).  
When BCK is 32fs, output is MSB first.
- When output data are 24bit/channel, see Figures 7 (b) and 7 (c).  
When BCK is 48fs (external output), output is MSB first or the 8 clock shifted highest 16bit data with effective data before the change point of LRCK.  
When BCK is 64fs, output is MSB first with effective data after the change point of LRCK or 8 clock shift with effective data before the change point of LRCK.

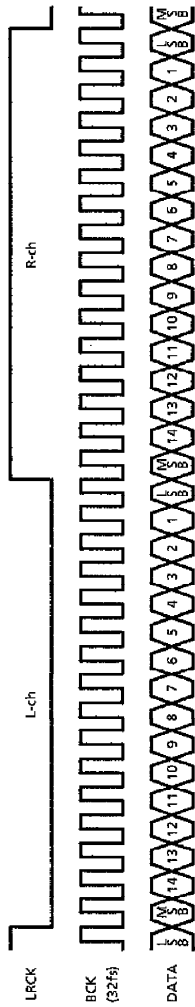


Fig. 7 (a) 16bit Data Output Format

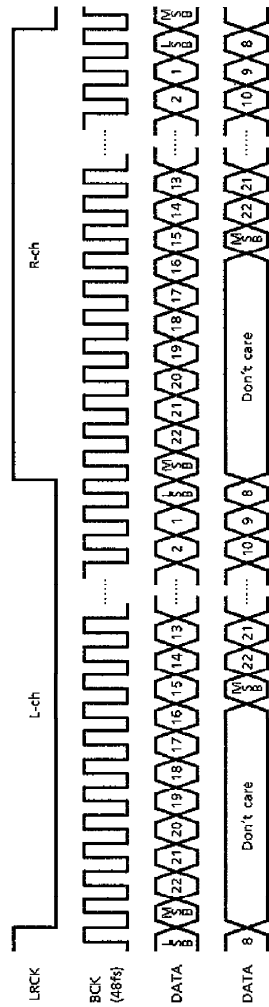


Fig. 7 (b) 24bit Data Output Format

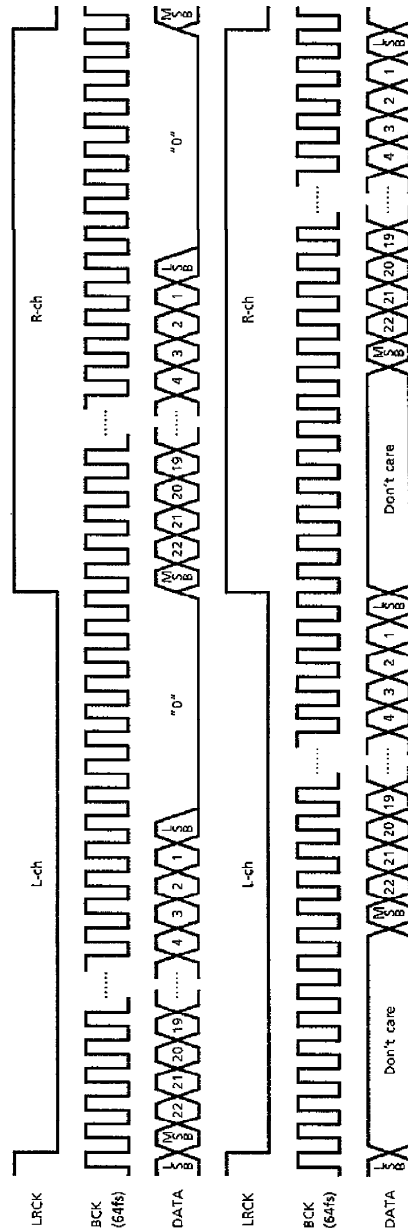


Fig. 7 (c) 24bit Data Output Format

3. I<sup>2</sup>C BUS interface circuit

The TC9337F transfers serial data to the host microcontroller using  $\overline{CS}$ ,  $\overline{IFOK}$  terminal and IFCK, IFDT terminal for I<sup>2</sup>C BUS. The microcontroller is used to set data modes, set data in the coefficient RAM (CRAM) and offset RAM (OFRAM), set the module sequencer (MSEQ), and read data from the internal data bus (DBUS). TC9337F operation mode are slave mode and fast mode of I<sup>2</sup>C BUS, and there isn't data shift clock output.

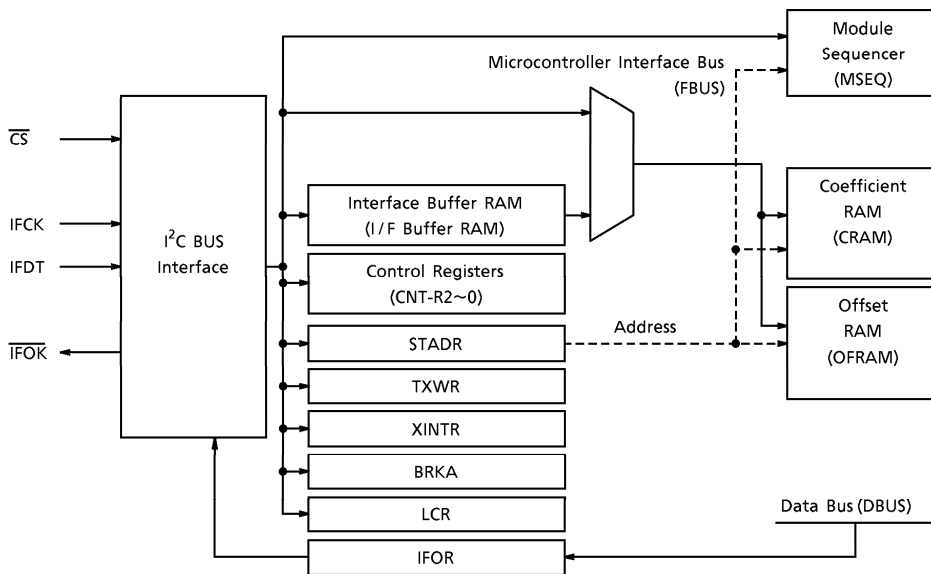


Fig.8 Structure of Microcontroller Interface Block

An example of a connection with the host microcontroller is shown below in Figure 9.

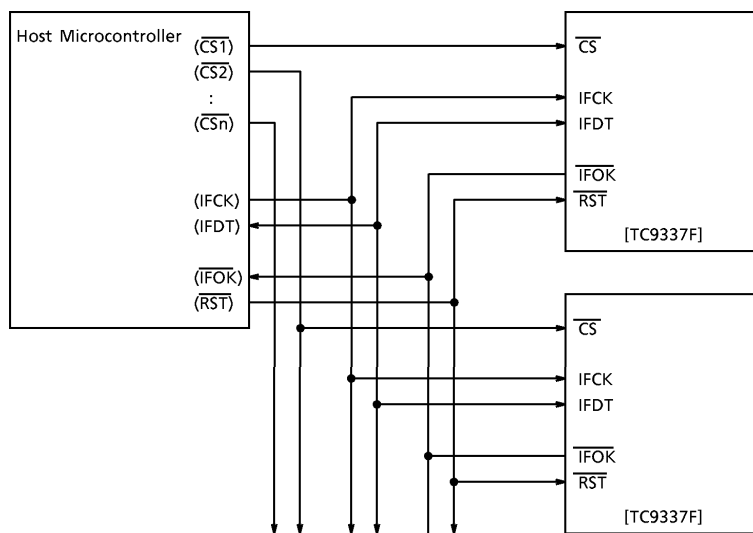


Fig.9 Relationship between Host Microcontroller and TC9337F

The functions of the signals on the microcontroller interface pins are as shown below.

- IFCK signal (input) : Data signal shift clock for I<sup>2</sup>C BUS
- IFDT signal (input/output) : Data input/output signal for I<sup>2</sup>C BUS
- $\overline{CS}$  signal (input) : Sets TC9337F data receive and transmit to active.
- $\overline{F\!O\!K}$  signal (output) : Handshake signal for microcontroller, as monitor to the data bus (DBUS)

The TC9337F receive and transmit synchronous serial data to IFCK signal (Shift clock) from the host microcontroller for I<sup>2</sup>C BUS interface.

In case of receiver operation, transfer slave address (write register) from microcontroller, continue transfer sub address and necessary data.

Slave address 32h (write register)

MSB							LSB
0	0	1	1	0	0	1	0

In case of transmitter operation, transfer slave address (write register) from microcontroller, continue transfer necessary data.

Slave address 33h (read register)

MSB							LSB
0	0	1	1	0	0	1	1

## (1) Data transmission format

## (1-1) Receiver operation

In case of microcontroller don't handshake another TC9337F chip,  $\overline{CS}$  terminal is low-level fixed. When microcontroller handshake another TC9337F chip, it have to be every access to the TC9337F's  $\overline{CS}$  terminal at low-level.

At idle, the IFCK and IFDT signals are high-level. After the microcontroller is to be a start condition of transmission (When IFCK clock is high-level, microcontroller control to IFDT signal at low-level) and TC9337F become condition the receiver mode at received slave address 32h. After the TC9337F is appreciated salve address 32h, IFDT transmit to microcontroller at low-level.

After the microcontroller transfer sub address (1byte), continue transfer necessary data (2byte). There are 12 sub address (0Fh-04h) used to control TC9337F from microcontroller. The end of the microcontroller transmitted end condition is to be finished. (When IFCK clock is high-level, microcontroller control to IFDT signal at high-level).

- Ex1. Figure 10-1 shows examples of set to register data 1234h at control register 1 (sub address 0Eh).
- Ex2. Figure 10-2 to 10-4 shows examples of set to coefficient data at coefficient RAM (sub address 09h). After microcontroller set to coefficient address 080h at start address register and transfer coefficient data FFFh, 7FFFh, C000h and 4000H at coefficient RAM.

## (1-2) Transmitter operation

At idle, the IFCK and IFDT signals are high-level. After the microcontroller is to be a start condition of transmission (when IFCK clock is high-level, microcontroller control to IFDT signal at low-level) and TC9337F become condition the transmitter mode at received slave address 33h. After the TC9337F is appreciated slave address 33h, IFDT transmit to microcontroller at low-level.

As TC9337F output data synchronous IFCK signal, microcontroller able to read out value of the data bus data. Further  $\overline{IFOK}$  signal able to handshake signal for microcontroller, as monitor to the data bus (DBUS).

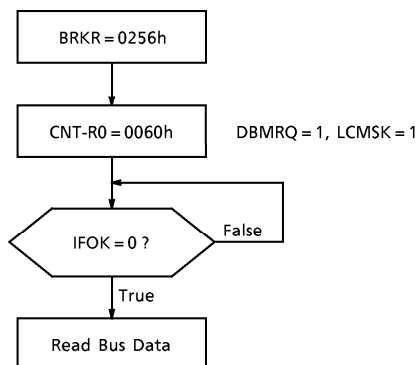
Normally IFOK terminal output high-level, if DBUS data is latched to internal data output register (IFOR),  $\overline{IFOK}$  terminal output low-level. At DBUS data is read out finished,  $\overline{IFOK}$  terminal output high-level.

The end of the microcontroller transmitted end condition is to be finished. (when IFCK clock is high-level, microcontroller control to IFDT signal at high-level).

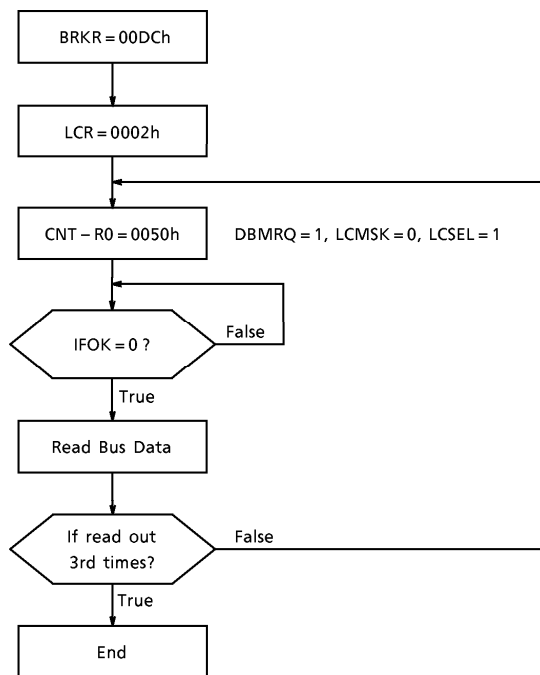
- Ex1. Figure 11 shows examples of read out 3byte data of DBUS.
- Ex2. Figure 12-1 to 12-3 shows examples of read out data of DBUS as using only program counter (PC) value. Otherwise how to read out data of DBUS as using program counter (PC) value and loop counter value.



① In case of read out DBUS data at program counter value is PC = 256h.



② In case of read out DBUS data at program counter value is PC = 0DCh when loop counter value is each of LC1 = 02h, LC1 = 01h, and LC1 = 00h.



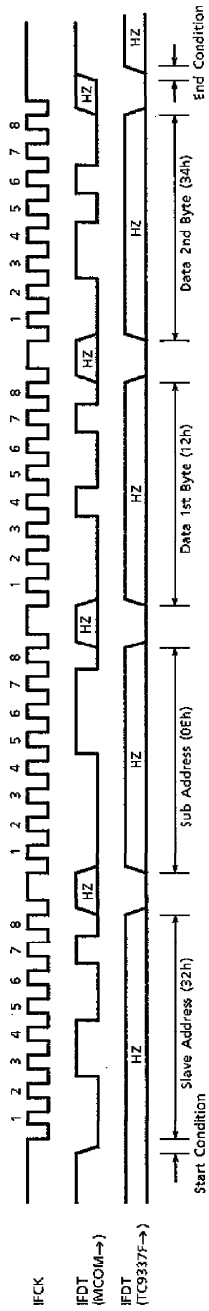


Fig. 10-1

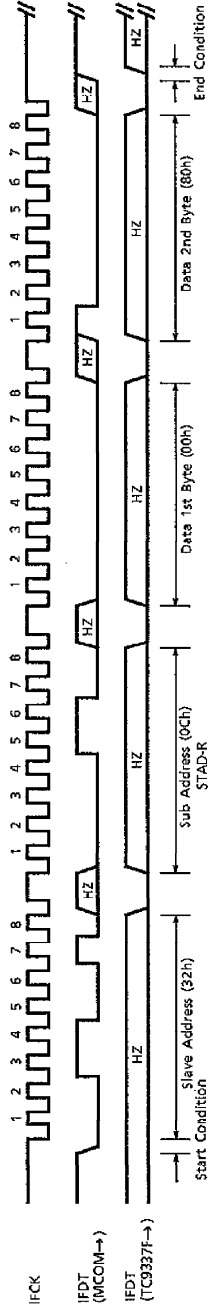


Fig. 10-2

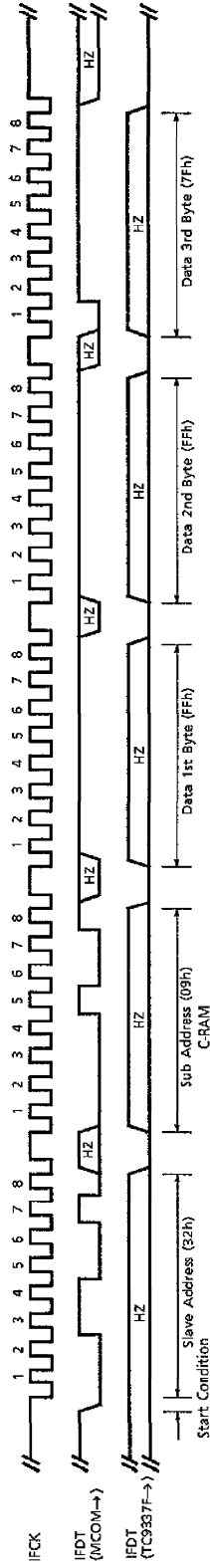


Fig. 10-3

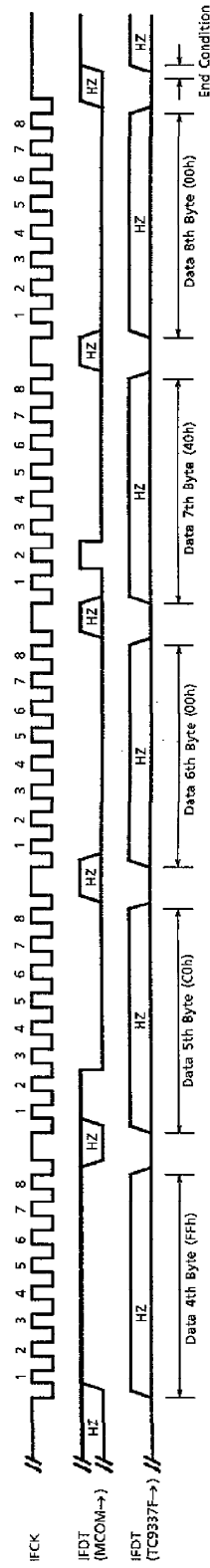


Fig. 10-4

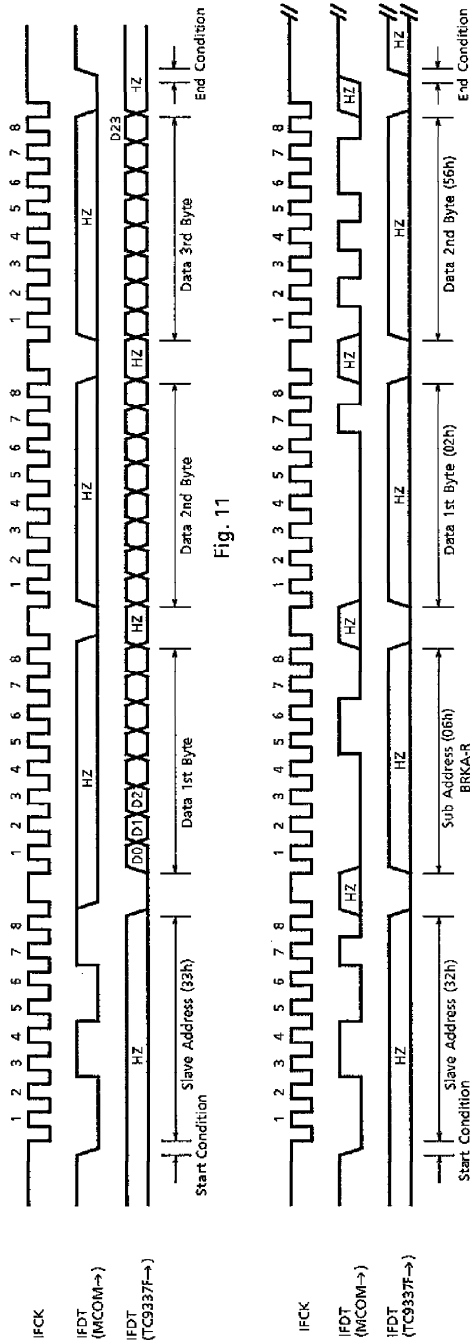


Fig. 11

Fig. 12-1

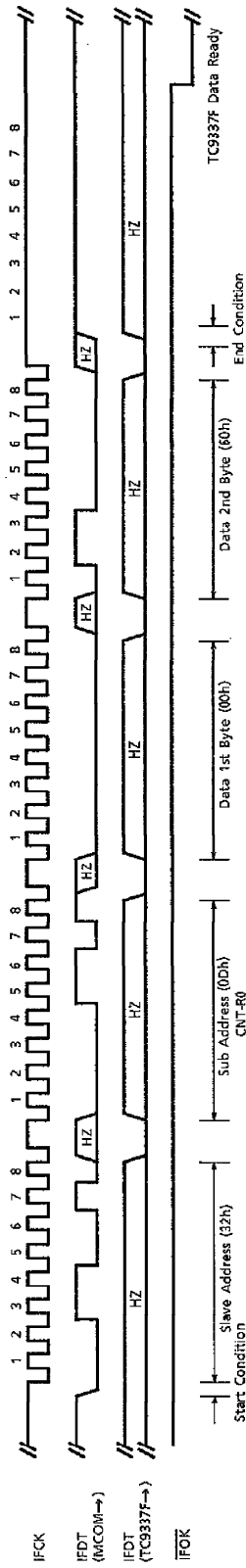


Fig. 12-2

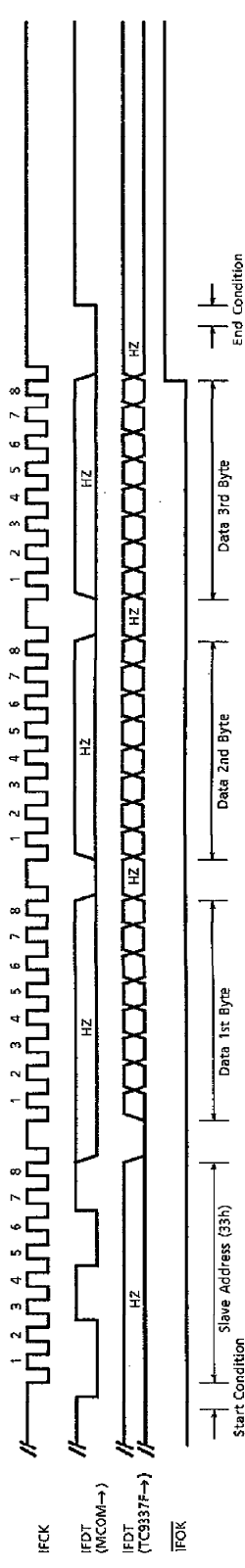


Fig. 12-3

## (2) Sub address

Sub address is 1byte data after transferred slave address (write register). There are 12 sub address (0Fh – 04h) used to control TC9337F from microcontroller. It is effective at receiver mode only.

Table 3 Sub address

REGISTER / MEMORY OF WRITE DESTINATION		FETCH SYNC	SUB ADDRESS	
			(HEX)	(BIN)
CNT-R2	CONTROL REGISTER 2	Async	0Fh	00001111b
CNT-R1	CONTROL REGISTER 1	Async	0Eh	00001110b
CNT-R0	CONTROL REGISTER 0	Sync	0Dh	00001101b
STAD-R	START ADDRESS REGISTER	Async	0Ch	00001100b
TXW-R	TRANSFER EXCHANGE WRITE ADDRESS REGISTER	Async	0Bh	00001011b
MSEQRAM	MODULE SEQUENCER RAM	Sync	0Ah	00001010b
CRAM	COEFFICIENT RAM	Async	09h	00001001b
OFRAM	OFFSET RAM	Async	08h	00001000b
XINT-R	EXTERNAL INTERRUPT REGISTER	Sync	07h	00000111b
BRKA-R	BREAK ADDRESS REGISTER	Async	06h	00000110b
LC-R	LOOP COUNTER COMPARE REFERENCE REGISTER	Async	05h	00000101b
TEST-R	TEST REGISTER for test mode	Async	—	—

In case of fetch sync is sync in Table 3, data is latched at edge of SYNC signal next after internal circuit received. Edge of SYNC signal is able to change at control register 1 (CNT-R1). Normally, TEST register is not used.

## (4) Control registers and dedicated interface registers

## (4-1) Control register 2 (CNT-R2)

(\* : default value)

BIT	SYMBOL	DESCRIPTION OF FINCTION	DESCRIPTION OF FINCTION	
			0*	1
15	LRIS1	Selects channel clock or bit clock for audio serial data input from the SDI1 terminal.	0*	Generates internally
			1	ELRI1 / EBCI1
14	BCIS1	Selects bit length of audio serial data input from the SDI1 terminal.	0*	16bit
			1	24bit
13	SIFMT1	Selects format of audio serial data input from the SDI1 terminal.	0*	MSB first
			1	LSB first
12	LRIS0	Selects a channel clock or bit clock for audio serial data input from the SDI0 terminal.	0*	Generates internally
			1	ELRIO / EBCIO
11	BCIS0	Selects bit length of audio serial data input from the SDI0 terminal.	0*	16bit
			1	24bit
10	SIFMT0	Selects format of audio serial data input from the SDI0 terminal.	0*	MSB first
			1	LSB first
9	SISEL	Selects input terminal for input register SDI0.	0*	SDI0
			1	SDI1
8	LROS2	Selects a channel clock or bit clock for audio serial data output to the SDO2 terminal. (Note 2)	0*	Generates internally
			1	ELRO / EBCO
7	BCOS2	Selects an internally generated bit clock for audio serial data output to the SDO2 terminal.	0*	FS32 (16bit / ch)
			1	FS64 (32bit / ch)
6	SOFMT2	Selects whether audio serial data output to the SDO2 pin are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted
5	LROS1	Selects a channel clock or bit clock for audio serial data output to the SDO1 terminal. (Note 2)	0*	Generates internally
			1	ELRO / EBCO
4	BCOS1	Selects an internally generated bit clock for audio serial data output to the SDO1 terminal.	0*	FS32 (16bit / ch)
			1	FS64 (32bit / ch)
3	SOFMT1	Selects whether audio serial data output to the SDO1 terminal are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted
2	LROS0	Selects a channel clock or bit clock for audio serial data output to the SDO0 terminal. (Note 2)	0*	Generates internally
			1	ELRO / EBCO terminal input
1	BCOS0	Selects an internally generated bit clock for audio serial data output to the SDO0 terminal.	0*	FS32 (16bit / ch)
			1	FS64 (32bit / ch)
0	SOFMT0	Selects whether audio serial data output to the SDO0 terminal are to be effective data after the change point of LRCK or 8 clock shifted.	0*	Effective data after the change point of LRCK
			1	8 clock shifted

(Note 1) Normally set only once at initialization.

Data can be set in CNT-R2 asynchronously with the SYNC signal.

(Note 2) When a channel clock or bit clock is externally input, (LROS bits 2~0 set to "1"), the data can be output to pins SDO2~0 with 8 clock shifted by setting SOFMT~0. Data can also be output with 8 clock shifted by program (operation) without the above setting.

## (4-2) Control register 1 (CNT-R1)

(\* : default value)

BIT	SYMBOL	DESCRIPTION OF FUNCTIONS	
15 ⋮ 11	—	Unused	0* fixed 0 data
10	ZST	Switches coefficient ROM mode (for dis logarithm table).	0 2-cycle
			1* 1-cycle
9	EMU	Test emulator mode	0* Normal
			1 SYNC = ELRI1
8	SYNCS	Selects internal generation or external input (from SYNC terminal) of SYNC signal.	0* Generates internally
			1 Inputs externally
7	SYNCP	Switches SYNC signal polarity.	0* Fall
			1 Rise
6	SYRC	Resets the coefficient pointer (CP) for each SYNC signal.	0* Enable
			1 Disable
5	SYRO	Resets the offset address pointer (OFP) for each SYNC signal.	0* Enable
			1 Disable
4	EBCS	Modifies LROS2-0, BCOS2-0 and LR terminal output signals.	0* Disable (normal)
			1 Enable
3	—	Unused	0* fixed 0 data
2	IFOS	Selects output format for data (24bit) read from IFOR (DBUS).	0* Upper 16bit
			1 24bit
1	DLSEP	Divides the delay RAM (DLRAM) into a delay area and a data table area.	0* Divides.
			1 Does not divide.
0	ACMP RQ	Overwrites when the value of the CRAM or OFRAM pointer matches the overwrite counter address (automatically set to "0" after executing batch overwrite of the interface buffer RAM.)	0* Disable
			1 Enable

(Note) Normally set only once at initialization.  
Data can be set in CNT-R1 asynchronously with the SYNC signal.

(4-3) Control register 0 (CNT-R0)

(\* : default value)

BIT	SYMBOL	DESCRIPTION OF FUNCTIONS	
15 ⋮ 9	—	Unused	0* fixed 0 data
8	SQALL	Renders instruction non-operative and clears the flag.	0 Off (RUN)
			1* On (NOP)
7	BRKRQ	Setting this bit to "1" after the break address (BRKA) of the program counter is set executes a break.	0* Break off
			1 Break on
6	DBMRQ	Requests data read from DBUS.	0* Does not request.
			1 Requests.
5	LCMSK	Compares the loop counter value during data read from DBUS.	0* Compares.
			1 Does not compare.
4	LCSEL	Selects the counter (LC0 or LC1) to be compared when comparing the loop counter value during data read from DBUS.	0* LC0
			1 LC1
3	INMT	Mutes input from the SDI0 and SDI1 terminals.	0 Mute off
			1* Mute on
2	OUTMT2	Mutes output to the SDO2 terminal.	0 Mute off
			1* Mute on
1	OUTMT1	Mutes output to the SDO1 terminal.	0 Mute off
			1* Mute on
0	OUTMT0	Mutes output to the SDO0 terminal.	0 Mute off
			1* Mute on

(Note) Data are read from CNT-R0 synchronously with the SYNC signal.

(4-4) Dedicated interface registers

Start address register (STADR)

This register sets the address to start writing data to CRAM, OFRAM and MSEQ. It consists of a presettable up-counter. (9bit)

	15	...	9	8	7	6	5	4	3	2	1	0
CRAM	0	0	0	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
OFRAM	0	0	0	0	0	0	RA5	RA4	RA3	RA2	RA1	RA0
MSEQ	0	0	0	0	0	0	0	0	RA3	RA2	RA1	RA0

When data are set in MSEQ, data are sent 1 byte at a time.

(Note) Data are set in STADR asynchronously with the SYNC signal.

**Transfer exchange write address register (TXWR)**

When ACMPRQ in control register 1 (CNT-R1) is set to "1", this register sets the length of data to be overwritten to CRAM or OFRAM using interface buffer RAM.

Overwrites up to 16word are supported. (4bit)

NUMBER OF WORDS OVERWRITTEN	TXWR						
	TXW15	...	TXW4	TXW3	TXW2	TXW1	TXW0
1	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1
⋮	⋮						
15	0	0	0	1	1	1	0
16	0	0	0	1	1	1	1

(Note) Data can be set in TXWR asynchronously with the SYNC signal.

**Module sequencer (MSEQ)**

The module sequencer sets the sequence in which the subroutines grouped in program ROM are called.

It has a 16word × 10bit structure, and data are set by the microcontroller one word at a time at the program ROM sequence start address. Set the 4bit address of the sequencer, which sets the data store sequence, in STADR.

Data cannot be transferred to the MSEQ using the interface buffer RAM.,

(Note 1) Bit 15~10 are fixed 0 data.

(Note 2) MSEQ data is read in synchronously with the SYNC signal.

**Coefficient RAM (CRAM)**

The coefficient RAM has a 320word × 16bit structure, and data can be changed one word at a time during each sampling period by the microcontroller communication procedure. Using the interface buffer RAM, 16word can be overwritten during each sampling period.

(Note) Data can be set in CRAM asynchronously with the SYNC signal.  
(during continuous setting)

**Offset RAM (OFRAM)**

The offset RAM has a 64word × 16bit structure, and the overwriting procedure is similar to that of the CRAM.

(Note) Data can be set in OFRAM asynchronously with the SYNC signal.  
(during continuous setting)

**External interrupt register (XINTR)**

The external interrupt register sets data in IFF2-0, which are allocated to the conditional jump flag (F) field. (3bit)

FLAG FIELD			D15	...	D3	D2	D1	D0
IFF2	IFF1	IFF0						
Off	Off	Off	0	0	0	0	0	0
Off	Off	On	0	0	0	0	0	1
Off	On	Off	0	0	0	0	1	0
⋮			⋮					
On	On	On	0	0	0	1	1	1

(Note) XINTR data are read synchronously with the SYNC signal.



**Break address (BRKAR) register**

This register sets the break address. Continuous comparison is made with the program counter (PC) and when BRKRQ of the control register is on, program execution is stopped. Since DBUS data are fetched to IFDOR when the value of the PC matches, it is possible to turn BRKRQ off and read the internal data while program execution is in progress. (10bit)

(Note 1) Bit 15~10 are fixed 0 data.

(Note 2) Data can be set in BRKAR asynchronously with the SYNC signal.

**Loop counter compare reference register (LCR)**

When reading break or DBUS data, either of loop counters LC0 or LC1 is being compared along with the PC value, this register stores the value of the loop counter to be compared. (8bit)

Which of the loop counters is being compared is set by LCSEL of control register 0 (CNT-R0). When break or DBUS data have been read, LCR is automatically decremented by 1.

(Note 1) Bit 15~8 are fixed 0 data.

(Note 2) Data can be set in LCR asynchronously with the SYNC signal.

**Interface data output register (IFDOR)**

This is a buffer register that can read DBUS data. (24bit)

The microcontroller can read data from IFDOR serially.

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>DD</sub>	-0.3~6.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	1250	mW
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

**ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V<sub>DD</sub> = 5V)****DC CHARACTERISTICS**

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V <sub>DD</sub>	—	Ta = -40~85°C	4.75	5.0	5.25	V
Power Supply Current-1 (no load, external oscillation)	I <sub>DD1</sub>	—	f <sub>opr</sub> = 24.576MHz	—	75	100	mA
			f <sub>opr</sub> = 18.432MHz	—	55	75	
Power Supply Current-2 (no load, VCO oscillation)	I <sub>DD2</sub>	—	f <sub>opr</sub> = 24.576MHz	—	80	100	
			f <sub>opr</sub> = 18.432MHz	—	65	85	

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Clock terminals (XI, XO)

Input Voltage	"H" Level	V <sub>IH1</sub>	—	XI terminal	3.5	—	—	V
	"L" Level	V <sub>IL1</sub>	—		—	—	1.5	
Output Voltage	"H" Level	V <sub>OH1</sub>	—	I <sub>OH</sub> = -3.0mA XO terminal	4.5	—	—	
	"L" Level	V <sub>OL1</sub>	—		I <sub>OL</sub> = 6.0mA	—	—	
Feedback Resistor	R <sub>fb</sub>	—	—	—	100	500	kΩ	

Input terminals

Input Voltage	"H" Level	V <sub>IH2</sub>	—	(*1)	4.2	—	—	V	
	"L" Level	V <sub>IL2</sub>	—		—	—	0.8		
Input Leakage Current	"H" Level	I <sub>IH2</sub>	—	V <sub>IN</sub> = V <sub>DD</sub> V <sub>IN</sub> = 0V	(*1)	—	—	10	μA
	"L" Level	I <sub>IL2</sub>	—			-10	—	—	
Threshold Voltage	"H" Level	V <sub>p</sub>	—	(*2)	—	3.2	—	V	
	"L" Level	V <sub>N</sub>	—		—	1.8	—		
Hysteresis Voltage		V <sub>H</sub>	—	(*2)	—	0.6	—	V	
Input Leakage Current	"H" Level	I <sub>IH3</sub>	—	V <sub>IN</sub> = V <sub>DD</sub> V <sub>IN</sub> = 0V	(*2)	—	—	10	μA
	"L" Level	I <sub>IIL3</sub>	—			-10	—	—	

(\*1) SDI0~1, PLOFF,  $\overline{RST}$  : CKSL, TEST0~2, TEST4 (Schmitt input terminals with pull-up resistor)

(\*2) SYNC, ELRI0~1, ELRO, EBCI0~1, EBCO,  $\overline{CS}$ , TES3, IFCK (Schmitt input terminals)

Output terminals

Output Voltage	"H" Level	V <sub>OH2</sub>	—	I <sub>OH</sub> = -1.0mA I <sub>OL</sub> = 1.0mA	(*3)	4.5	—	—	V
	"L" Level	V <sub>OL2</sub>	—			—	—	0.5	
Output Voltage	"H" Level	V <sub>OH3</sub>	—	I <sub>OH</sub> = -3.0mA I <sub>OL</sub> = 5.0mA	(*4)	4.5	—	—	
	"L" Level	V <sub>OL3</sub>	—			—	—	0.5	
Output Voltage	"H" Level	V <sub>OH4</sub>	—	I <sub>OH</sub> = -0.6mA I <sub>OL</sub> = 0.6mA	(*5)	4.5	—	—	
	"L" Level	V <sub>OL4</sub>	—			—	—	0.5	

(\*3) SDO0~2

(\*4) FS64, FS32, WCK, LR

(\*5) AMPO

Three state output terminals (PD)

Output Voltage	"H" Level	V <sub>OH5</sub>	—	I <sub>OH</sub> = -3.0mA I <sub>OL</sub> = 5.0mA	—	4.5	—	—	V
	"L" Level	V <sub>OL5</sub>	—			—	—	0.5	
Output Off-leakage Current		IOZ5	—	V <sub>OH</sub> = V <sub>DD</sub> , V <sub>OL</sub> = 0V		—	—	± 10	μA

Open-drain output terminals (IFDT,  $\overline{IFOK}$ )

"L" Level Output Voltage	V <sub>OL7</sub>	—	I <sub>OL</sub> = 5.0mA	—	—	0.5	V
Output Open Leakage Current	IOZ7	—	V <sub>OH</sub> = V <sub>DD</sub>	—	—	± 10	μA

CHARACTERISTIC	SYMBOL	TEST CIR-UCIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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## Pull-up and pull-down resistor terminals

Pull-up Resistor	RUP	—	(*6)	—	35	200	k $\Omega$
Pull-down Resistor-1	Rdwn1	—	(*7)	—	25	200	
Pull-down Resistor-2	Rdwn2	—	(*8)	—	0.25	80	

(\*6) TES4,  $\overline{RST}$ ,  $\overline{IFOK}$ , CKSL, TES0~2

(\*7) PLOFF

(\*8) XI

## AC CHARACTERISTICS

## External clock input terminal (XI)

XI Clock Cycle	t <sub>XI</sub>	—	—	40	—	—	ns
XI Clock "H" Duration	t <sub>XIH</sub>	—	—	—	20	—	
XI Clock "L" Duration	t <sub>XIL</sub>	—	—	—	20	—	

Reset terminal ( $\overline{RST}$ )

Stand-by Time	t <sub>ST</sub>	—	—	250	—	—	$\mu$ s
Reset Pulse Width	t <sub>RST</sub>	—	—	0.15	—	—	

## Audio serial interface (fs = 48kHz)

ELRI Holding Time	t <sub>LIH</sub>	—	C <sub>L</sub> = 30pF	-75	—	75	ns
SDI Data Setup Time	t <sub>DIS</sub>	—	C <sub>L</sub> = 30pF	50	—	—	
SDI Data Hold Time	t <sub>DIH</sub>	—	C <sub>L</sub> = 30pF	50	—	—	
EBCI Clock Cycle	t <sub>EBCI</sub>	—	C <sub>L</sub> = 30pF	325	—	—	
EBCI Clock "H" Duration	t <sub>EBIH</sub>	—	C <sub>L</sub> = 30pF	162	—	—	
EBCI Clock "L" Duration	t <sub>EBIL</sub>	—	C <sub>L</sub> = 30pF	162	—	—	
ELRO Hold Time	t <sub>LOH</sub>	—	C <sub>L</sub> = 30pF	-75	—	75	
SDO Data Output Delay Time (1)	t <sub>DO1</sub>	—	C <sub>L</sub> = 30pF	—	—	65	
SDO Data Output Delay Time (2)	t <sub>DO2</sub>	—	C <sub>L</sub> = 30pF	—	—	65	
EBCO Clock Cycle	t <sub>EBCO</sub>	—	C <sub>L</sub> = 30pF	325	—	—	
EBCO Clock "H" Duration	t <sub>EBOH</sub>	—	C <sub>L</sub> = 30pF	162	—	—	
EBCO Clock "L" Duration	t <sub>EBOL</sub>	—	C <sub>L</sub> = 30pF	162	—	—	
WCK Output Delay Time (1)	t <sub>DHL1</sub>	—	C <sub>L</sub> = 30pF	—	—	13	
LR Output Delay Time (1)	t <sub>DHL2</sub>	—	C <sub>L</sub> = 30pF	—	—	17	
FS32 Output Delay Time (1)	t <sub>DHL3</sub>	—	C <sub>L</sub> = 30pF	—	—	6	
WCK Output Delay Time (2)	t <sub>DLH1</sub>	—	C <sub>L</sub> = 30pF	—	—	23	
LR Output Delay Time (2)	t <sub>DLH2</sub>	—	C <sub>L</sub> = 30pF	—	—	27	

CHARACTERISTIC	SYMBOL	TEST CIR-UCIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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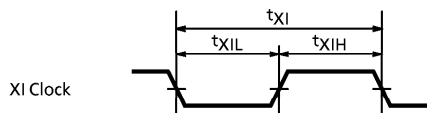
FS32 Output Delay Time (2)	$t_{DLH3}$	—	$C_L = 30\text{pF}$	—	—	17	ns
BCK Clock Cycle	$t_{BCK}$	—	$C_L = 30\text{pF}$	650	—	—	
BCK Clock "H" Duration	$t_{BCH}$	—	$C_L = 30\text{pF}$	325	—	—	
BCK Clock "L" Duration	$t_{BCL}$	—	$C_L = 30\text{pF}$	325	—	—	

I<sup>2</sup>C bus interface

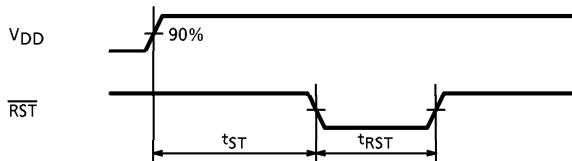
IFCK Clock Frequency	$f_{IFCK}$	—	$f_{IFCK} = 1 / T_{IFCK}$	0	—	400	kHz
IFCK Clock "H" Duration	$t_H$	—	$C_L = 400\text{pF}$	0.60	—	—	
IFCK Clock "L" Duration	$t_L$	—	$C_L = 400\text{pF}$	1.30	—	—	
Data Setup Time	$t_{DS}$	—	$C_L = 400\text{pF}$	0.10	—	—	
Data Hold Time	$t_{DH}$	—	$C_L = 400\text{pF}$	0.00	—	0.90	
Transmission Start Condition Hold Time	$t_{SCH}$	—	$C_L = 400\text{pF}$	0.60	—	—	
Transmission Start Condition Setup Time For a Repeated Start Condition	$t_{SCS}$	—	$C_L = 400\text{pF}$	0.60	—	—	
Transmission End Condition Setup Time	$t_{ECS}$	—	$C_L = 400\text{pF}$	0.60	—	—	
Data Transmission Interval	$t_{BUF}$	—	$C_L = 400\text{pF}$	1.30	—	—	
I <sup>2</sup> C Rise Time	$t_R$	—	$C_L = 400\text{pF}$	—	—	0.30	
I <sup>2</sup> C Fall Time	$t_F$	—	$C_L = 400\text{pF}$	—	—	0.30	

AC CHARACTERISTICS MEASUREMENT POINTS

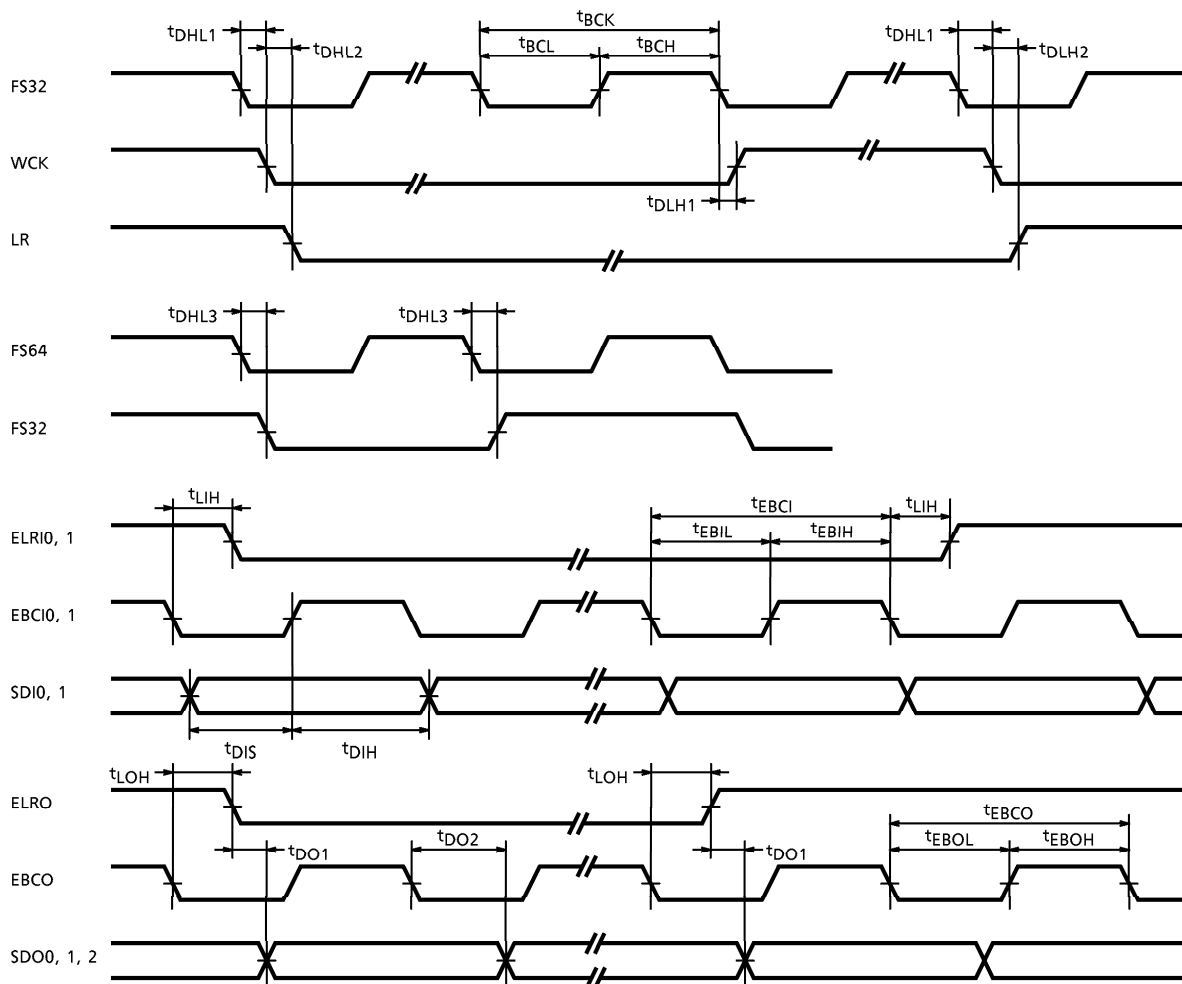
(1) External clock input terminal



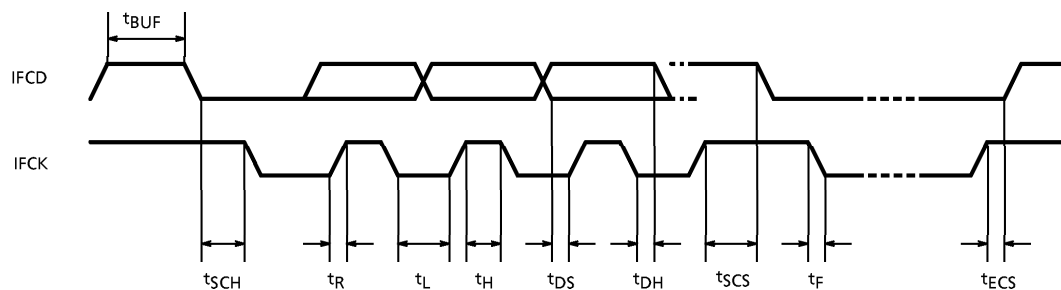
(2) Reset terminal



(3) Audio serial interface



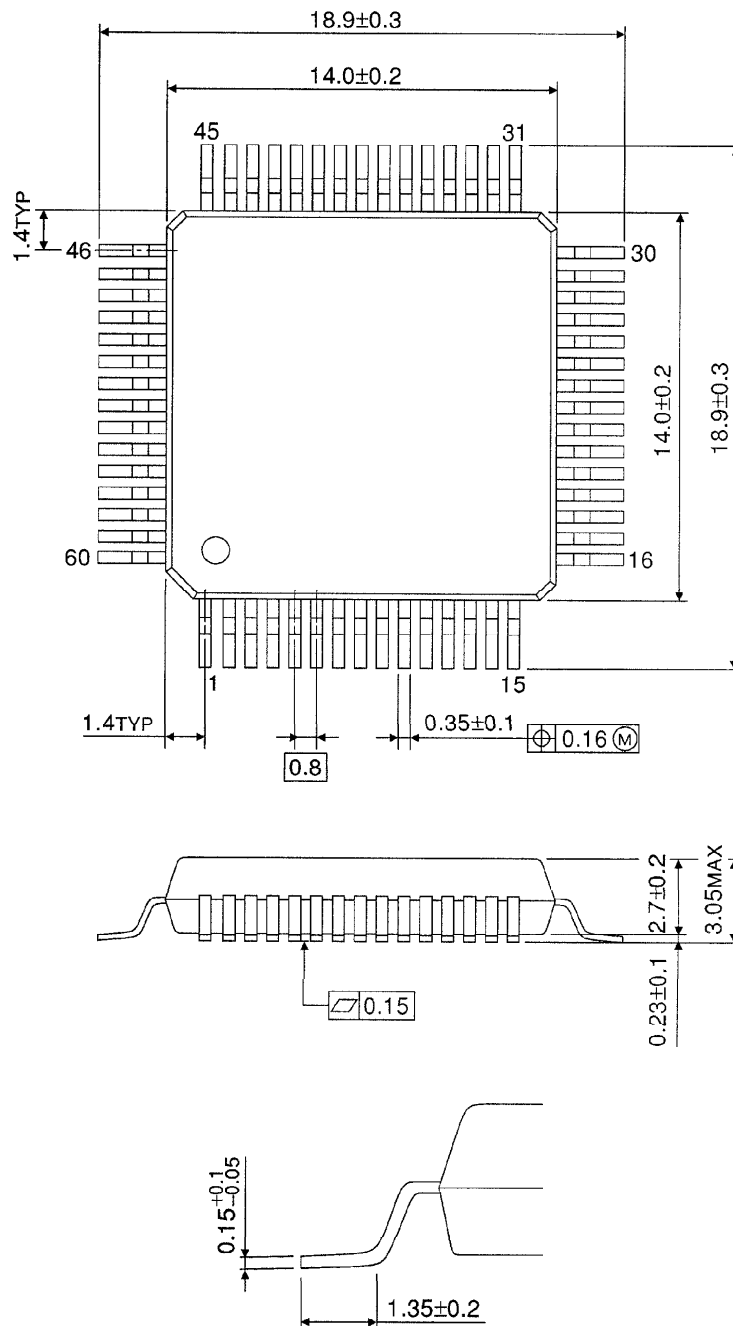
(4) I<sup>2</sup>C BUS timing chart



Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Right to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

**OUTLINE DRAWING**  
QFP60-P-1414-0.80D

Unit : mm



Weight : 1.08g (Typ.)