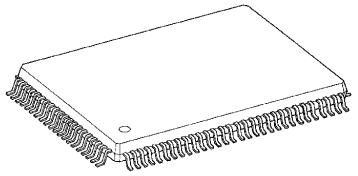
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9432AF

DIGITAL SERVO SINGLE CHIP PROCESSOR BUILT IN 1 BIT DA CONVERTER

The TC9432AF is a single chip processor which incorporates the following function : synchronous separation protection and interpolation, EFM demodulation, Error correction, microcontroller interface, digital equalizer for use in servo LSI and servo control circuit.
In addition, the TC9432AF incorporates a 1 bit DA converter. In combination with the head amplifier TA2109F, TA2122FN for digital servo, the TC9432AF allow simplified, adjustment-free structuring of CD player system.



QFP100-P-1420-0.65A

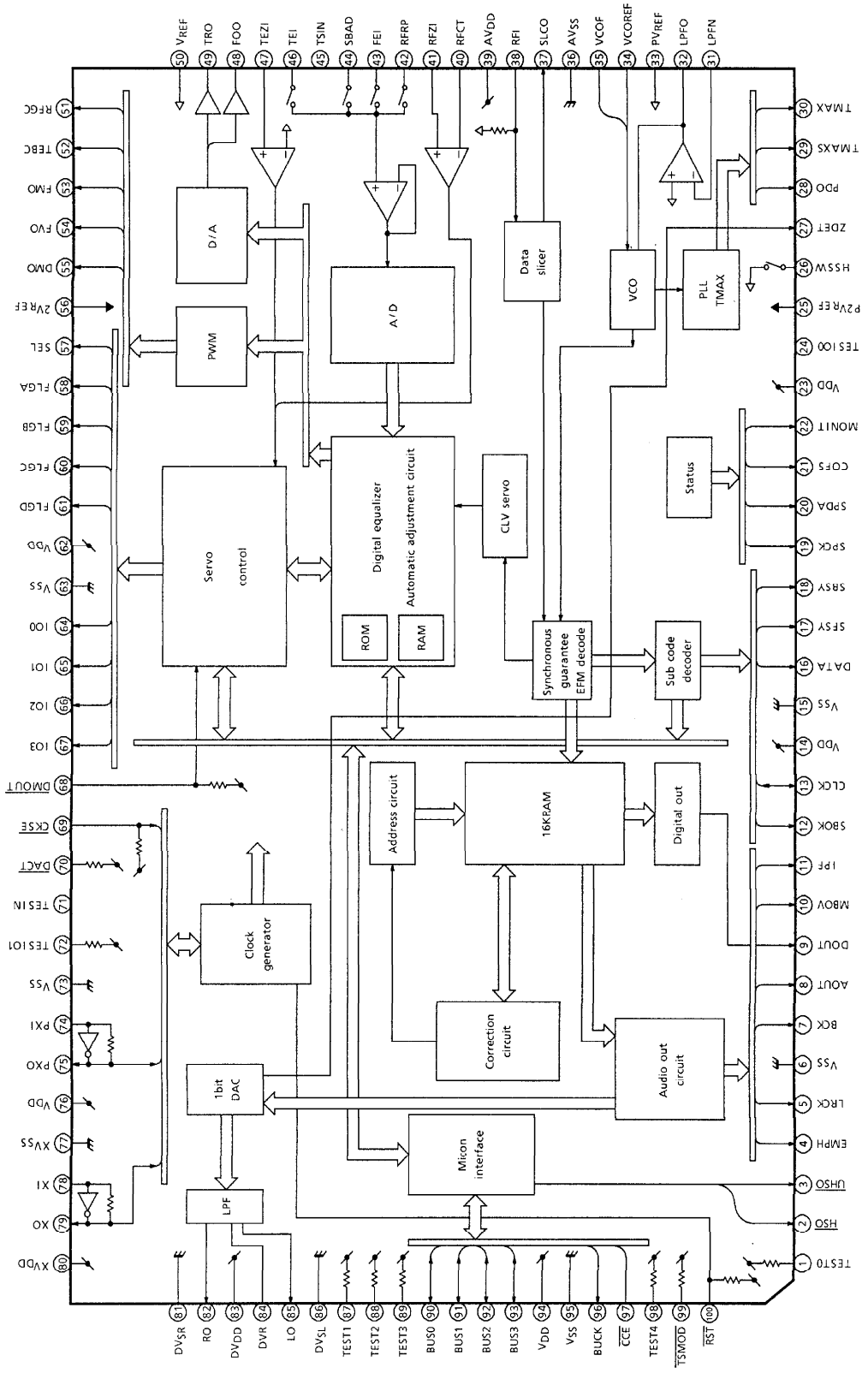
Weight : 1.6 g (Typ.)

FEATURES

- Sync pattern detection, sync signal protection and synchronization can be made correctly.
- Built in EFM demodulation circuit, subcode demodulation circuit.
- Capable of correcting dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- The TC9432AF respond to variable playback system.
- Jitter absorbing capacity of ±6 frames.
- Built in 16KRAM.
- Built in digital out circuit.
- Built in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Reed timing free subcode Q data and capable of synchronous output with audio data.

- Built in data slicer and analog PLL (free-adjustment VCO).
- Capable of automatic adjustment function of focus servo and tracking servo, for loop gain, offset and balance.
- Built in RF gain automatic adjustment circuit.
- Built in digital equalizer for phase compensation.
- Built in RAM for digital equalizer for coefficient, and capable of variable pickup.
- Built in focus, tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Lens-kick are using speed controlled form.
- Built in AFC circuit and APC circuit for CLV servo of disc motor.
- Built in anti-defect and anti-shock circuit.
- Built in 8 times oversampling 1 bit DA converter.
- Built in analog filter for 1 bit DA converter.
- Built in zero data detect output circuit.
- The TC9432AF capable of 4 times speed operation.
- Built in microcontroller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 100 pin flat package.

BLOCK DIAGRAM (Top view)



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PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	TEST0	I	Test mode terminal. Normally, keep at open.	With pull-up resistor.
2	$\overline{HSO}$	O	Playback speed mode flag output terminal. $\overline{UHSO}$ / $\overline{HSO}$ / PLAYBACK SPEED H / H / Normal H / L / 2 times L / H / 4 times L / L / —	—
3	$\overline{UHSO}$	O		
4	EMPH	O	Subcode Q data emphasis flag output terminal. Emphasis ON at "H" level and OFF at "L" level. The output polarity can invert by command.	—
5	LRCK	O	Channel clock output terminal. (44.1 kHz) L-ch at "L" level and R-ch at "H" level. The output polarity can invert by command.	—
6	V_{SS}	—	Digital GND terminal.	—
7	BCK	O	Bit clock output terminal. (1.4112 MHz)	—
8	AOUT	O	Audio data output terminal.	—
9	DOUT	O	Digital data output terminal.	—
10	MBOV	O	Buffer memory over signal output terminal. Over at "H" level.	—
11	IPF	O	Correction flag output terminal. At "H" level, AOUT output is made to correction impossibility by C_2 correction processing.	—
12	SBOK	O	Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at "H" level.	—
13	CLCK	I/O	Subcode P~W data readout clock input/output terminal. This terminal can select by command bit.	—
14	V_{DD}	—	Digital power supply voltage terminal.	—
15	V_{SS}	—	Digital GND terminal.	—
16	DATA	O	Subcode P~W data output terminal.	—
17	SFSY	O	Play-back frame sync signal output terminal.	—
18	SBSY	O	Subcode block sync signal output terminal.	—
19	SPCK	O	Processor status signal readout clock output terminal.	—
20	SPDA	O	Processor status signal output terminal.	—
21	COFS	O	Correction frame clock output terminal. (7.35 kHz)	—
22	MONIT	O	Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command.	—
23	V_{DD}	—	Digital power supply voltage terminal.	—

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I/O</th><th>FUNCTIONAL DESCRIPTION</th><th>REMARKS</th></tr>
<tr><td>24</td><td>TESIO0</td><td>I</td><td>Test input/output terminal. Normally, keep at "L" level.</td><td>—</td></tr>
<tr><td>25</td><td>$P2V_{REF}$</td><td>—</td><td>PLL double reference voltage supply terminal.</td><td>—</td></tr>
<tr><td>26</td><td>HSSW</td><td>O</td><td>2/4 times speed at "V_{REF}" voltage.</td><td>2-state output.
(PV_{REF}, HiZ)</td></tr>
<tr><td>27</td><td>ZDET</td><td>O</td><td>1bit DA converter zero detect flag output terminal.</td><td>—</td></tr>
<tr><td>28</td><td>PDO</td><td>O</td><td>Phase difference signal output terminal of EFM signal and PLCK signal.</td><td>3-state output.
($P2V_{REF}$, PV_{REF}, V_{SS})</td></tr>
<tr><td>29</td><td>TMAXS</td><td>O</td><td>TMAX detection result output terminal. Selected by command bit (TMPS).</td><td>3-state output.
($P2V_{REF}$, PV_{REF}, V_{SS})</td></tr>
<tr><td>30</td><td>TMAX</td><td>O</td><td>TMAX detection result output terminal. Selected by command bit (TMPS).
<table>
<tr><th>DIFFERENCE RESULT</th><th>TMAX OUTPUT</th></tr>
<tr><td>Longer than fixed freq.</td><td>"$P2V_{REF}$"</td></tr>
<tr><td>Shorter than fixed freq.</td><td>"V_{SS}"</td></tr>
<tr><td>Within the fixed freq.</td><td>"HiZ"</td></tr>
</table></td><td>3-state output.
(P2VREF, HiZ, V_{SS})</td></tr>
<tr><td>31</td><td>LPFN</td><td>I</td><td>LPF amplifier inverting input terminal for PLL.</td><td>Analog input.</td></tr>
<tr><td>32</td><td>LPFO</td><td>O</td><td>LPF amplifier output terminal for PLL.</td><td>Analog output.</td></tr>
<tr><td>33</td><td>PV_{REF}</td><td>—</td><td>PLL reference voltage supply terminal.</td><td>—</td></tr>
<tr><td>34</td><td>VCOREF</td><td>I</td><td>VCO center frequency reference level terminal. Normally, keep at "PV_{REF}" level.</td><td>—</td></tr>
<tr><td>35</td><td>VCOF</td><td>O</td><td>VCO filter terminal.</td><td>Analog output.</td></tr>
<tr><td>36</td><td>AV_{SS}</td><td>—</td><td>Analog GND terminal.</td><td>—</td></tr>
<tr><td>37</td><td>SLCO</td><td>O</td><td>Data slice level output terminal.</td><td>Analog output.</td></tr>
<tr><td>38</td><td>RFI</td><td>I</td><td>RF signal input terminal.</td><td>Analog input. (Z_{in} : selected by command)</td></tr>
<tr><td>39</td><td>AV_{DD}</td><td>—</td><td>Analog power supply voltage terminal.</td><td>—</td></tr>
<tr><td>40</td><td>RFCT</td><td>I</td><td>RFRP signal center level input terminal.</td><td>Analog input.
(Z_{in} : 50 kΩ)</td></tr>
<tr><td>41</td><td>RFZI</td><td>I</td><td>RFRP zero cross input terminal.</td><td>Analog input.</td></tr>
<tr><td>42</td><td>RFRP</td><td>I</td><td>RF ripple signal input terminal.</td><td>Analog input.</td></tr>
<tr><td>43</td><td>FEI</td><td>I</td><td>Focus error signal input terminal.</td><td>Analog input.</td></tr>
<tr><td>44</td><td>SBAD</td><td>I</td><td>Sub-beam adder signal input terminal.</td><td>Analog input.</td></tr>
<tr><td>45</td><td>TSIN</td><td>I</td><td>Test input terminal. Normally, keep at "V_{REF}" level.</td><td>Analog input.</td></tr>
<tr><td>46</td><td>TEI</td><td>I</td><td>Tracking error signal input terminal.
Take in at tracking servo on.</td><td>Analog input.</td></tr>
<tr><td>47</td><td>TEZI</td><td>I</td><td>Tracking error zero cross input terminal.</td><td>Analog input.
(Z_{in} : 10 kΩ)</td></tr>
<tr><td>48</td><td>FOO</td><td>O</td><td>Focus servo equalizer output terminal.</td><td rowspan="2">Analog output.
($2V_{REF}$~AV_{SS})</td></tr>
<tr><td>49</td><td>TRO</td><td>O</td><td>Tracking servo equalizer output terminal.</td></tr>
<tr><td>50</td><td>V_{REF}</td><td>—</td><td>Analog reference voltage supply terminal.</td><td>—</td></tr>
</table>

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
51	RFGC	O	RF amplitude adjustment control signal output terminal.	3-state PWM signal output. ($2V_{REF}$, V_{REF}, V_{SS}) (PWM carrier = 88.2 kHz)
52	TEBC	O	Tracking balance control signal output terminal.	
53	TEBC	O	Feed equalizer output terminal.	
54	TEBC	O	Speed error signal or feed search equalizer output terminal.	
55	DMO	O	Disk equalizer output terminal. (PWM carrier = 88.2 kHz for DSP, Synchronize to PXO)	3-state output. ($2V_{REF}$, V_{REF}, V_{SS})
56	$2V_{REF}$	—	Analog double reference voltage supply terminal.	—
57	SEL	O	APC circuit ON/OFF indication signal output terminal. At the laser on time, UHF = L at "HiZ" level and UHF = H at "H" level.	—
58	FLGA	O	Extemal flag output terminal for internal signal. Can select signal from TEZC, $\overline{FOON}$, $\overline{FOK}$ and RFZC by command.	—
59	FLGB	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{DFCT}$, $\overline{FOON}$, $\overline{FMON}$ and RFZC by command.	—
60	FLGC	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{TRON}$, $\overline{TRSR}$, $\overline{FOK}$ and $\overline{SRCH}$ by command.	—
61	FLGD	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{TRON}$, $\overline{DMON}$, $\overline{HYS}$ and $\overline{SHC}$ by command.	—
62	V_{DD}	—	Digital power supply voltage terminal.	—
63	V_{SS}	—	Digital GND terminal.	—
64	IO0	I/O	General I/O terminal. Can change over input port or output port by command. At the input mode time can readout a state of terminal (H/L) by read command. At the output mode time can control a state of terminal (H/L/HiZ) by command.	—
65	IO1			
66	IO2			
67	IO3			
68	$\overline{DMOUT}$	I	This terminal controls IO0~IO3 terminal. At "L" level time, IO0, 1 out feed equalizer signal of 2-state PWM, IO2, 3 out disk equalizer signal of 2-state PWM.	With pull-up resistor.
69	$\overline{CKSE}$	I	Normally, keep at open.	With pull-up resistor.
70	$\overline{DACT}$	I	DAC test mode terminal. Normally, keep at open.	With pull-up resistor.
71	TESIN	I	Test input terminal. Normally, keep at "L" level.	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level.	Analog input.
73	V_{SS}	—	Digital GND terminal.	—

PIN No.	SYMBOL	I / O	FUNCTIONAL DESCRIPTION	REMARKS
74	PXI	I	Crystal oscillator connecting input terminal for DSP. Normally, keep at "L" level.	—
75	PXO	O	Crystal oscillator connecting output terminal for DSP.	
76	V_{DD}	—	Digital power supply voltage terminal.	—
77	XV_{SS}	—	Oscillator GND terminal for system clock.	—
78	XI	I	Crystal oscillator connecting input terminal for system clock.	—
79	XO	O	Crystal oscillator connecting output terminal for system clock.	—
80	XV_{DD}	—	Oscillator power supply voltage terminal for system clock.	—
81	DV_{SR}	—	Analog GND terminal for DA converter. (R-ch)	—
82	RO	O	R channel data forward output terminal.	—
83	DV_{DD}	—	Analog supply voltage terminal for DA converter.	—
84	DVR	—	Reference voltage terminal for DA converter.	—
85	LO	O	L channel data forward output terminal.	—
86	DV_{SL}	—	Analog GND terminal for DA converter. (L-ch)	—
87	TEST1	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
88	TEST2	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
89	TEST3	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
90	BUS0	I / O	Micon interface data input / output terminal.	Schmit input. With pull-up resistor.
91	BUS1	I / O		
92	BUS2	I / O		
93	BUS3	I / O		
94	V_{DD}	—	Digital power supply voltage terminal.	—
95	V_{SS}	—	Digital GND terminal.	—
96	BUCK	I	Micon interface clock input terminal.	Schmit input.
97	$\overline{CCE}$	I	Command and data sending / receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
99	$\overline{TSMOD}$	I	Local test mode selection terminal.	With pull-up resistor.
100	$\overline{RST}$	I	Reset signal input terminal. Reset at "L" level.	With pull-up resistor.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Power Dissipation	P_D	1420	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise specified, V_{DD} = AV_{DD} = DV_{DD} = XV_{DD} = 5 V, $2V_{REF}$ = $P2V_{REF}$ = 4.2 V, V_{REF} = PV_{REF} = 2.1 V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Assured Supply Voltage		V_{DD}	Ta = −40~85°C		4.5	5.0	5.5	V
Assured Supply Current		I_{DD}	Normal speed	XI = 16.9344 MHz	45	50	60	mA
			4 times speed		50	55	65	
Input Voltage	"H"Level	V_{IH}	CMOS Input Terminal (except Analog input)		3.5	—	—	V
	"L"Level	V_{IL}			—	—	1.5	
Input Current	"H"Level	I_{IH}	V_{IH} = 5 V	CMOS Input Terminal (except Analog input)	—	—	1.0	μA
	"L"Level	I_{IL}	V_{IL} = 0 V		−1.0	—	—	
Tri-State Leak Current	"H"Level	I_{TLH}	V_{IH} = 5 V	following (1)	—	—	0.1	μA
	"L"Level	I_{TLL}	V_{IL} = 0 V		−0.1	—	—	
Output Current	"H"Level	$I_{OH(1)}$	V_{OH} = 4.6 V	following (1) (except TMAXS, TMAX)	—	—	−1.0	mA
	"L"Level	$I_{OL(1)}$	V_{OL} = 0.4 V		2.0	—	—	
	"H"Level	$I_{OH(2)}$	V_{OH} = 4.6 V	following (2)	—	—	−1.0	
	"L"Level	$I_{OL(2)}$	V_{OH} = 0.4 V		2.0	—	—	
	"H"Level	$I_{OH(3)}$	V_{OH} = 4.6 V	following (3)	−1.4	—	−0.6	
	"L"Level	$I_{OL(3)}$	V_{OL} = 0.4 V		0.6	—	1.4	
	"H"Level	$I_{OH(4)}$	V_{OH} = 3.8 V	following (4)	—	—	−1.0	
	"L"Level	$I_{OL(4)}$	V_{OL} = 0.4 V		2.0	—	—	
V_{REF} Output ON Resistor		R_{ON}	following (4) (except TMAXS, TMAX)		—	—	500	Ω
Pull-up Resistor		R_{UP}	following (5)		25.0	50.0	75.0	kΩ
Osc. Amp. Feedback Resistor		R_N	between XI-XO and PXI-PXO terminal		1.0	2.0	3.0	MΩ

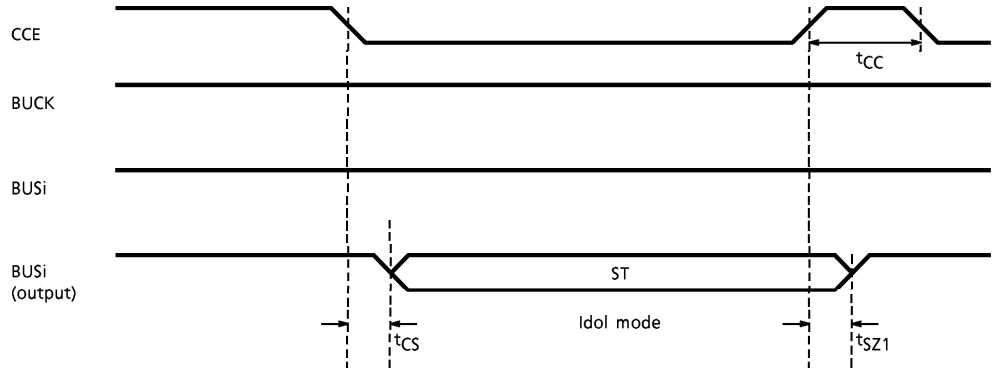
	TERMINAL NAME
(1) Terminal	$\overline{HSO}$, $\overline{UHSO}$, EMPH, DOUT, MBOV, IPF, SBOK, CLCK, TESIO1 DATA, SFSY, SBSY, SPCK, MONIT, TESIO0, TMAXS, TMAX, SEL FLGA, FLGB, FLGC, FLGD, IO0, IO1, IO2, IO3
(2) Terminal	LRCK, BCK, AOUT, SPDA, COFS, ZDET
(3) Terminal	BUS0~3
(4) Terminal	PDO, TMAXS, TMAX, RFGC, TEBC, FMO, FVO, DMO
(5) Terminal	$\overline{DMOUT}$, $\overline{CKSE}$, $\overline{DACT}$, TSMOD, $\overline{RST}$, TEST0~4

AC CHARACTERISTICS

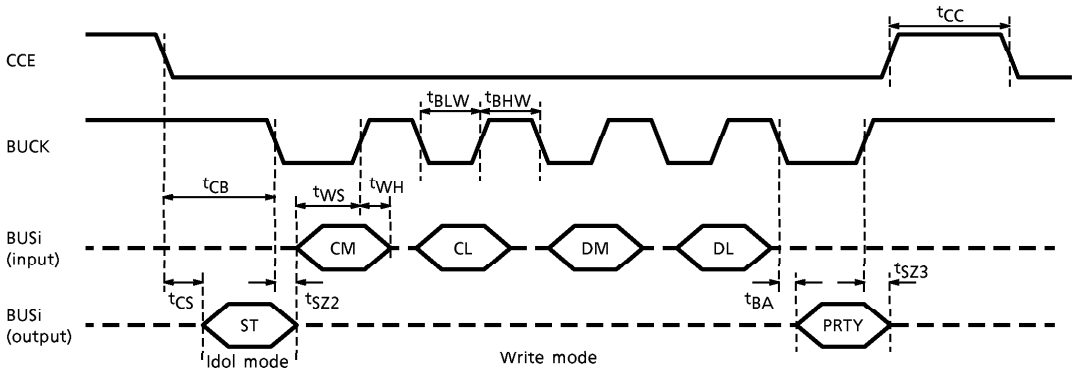
1. Microcomputer interface timing

CHARACTERISTIC	SIMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$\overline{CCE}$ "H" Clock Pulse Width	t_{CC}	—	120	—	—	ns
$\overline{CCE}$ Status Data Access Time	t_{CS}	$\overline{CCE}$ falling reference	0	—	—	
Status Data Disable Time	t_{SZ1}	$\overline{CCE}$ rising reference	0	—	—	
$\overline{CCE}$, BUCK Delay Pulse Width	t_{CB}	$\overline{CCE}$ falling reference	0	—	—	
BUCK "L" Clock Pulse Width	t_{BLW}	Write, SRC mode	120	—	—	
	t_{BLW}	QDRC mode	240	—	—	
BUCK "H" Clock Pulse Width (1)	t_{BHW}	Write, SRC mode	120	—	—	
BUCK "H" Clock Pulse Width (2)	t_{BHW}	QDRC mode (×1)	3000	—	—	
BUCK "H" Clock Pulse Width (3)	t_{BHW}	QDRC mode (×2)	1500	—	—	
BUCK "H" Clock Pulse Width (4)	t_{BHW}	QDRC mode (×4)	800	—	—	
Write Data Set-up Time	t_{WS}	BUCK rising reference	60	—	—	
Write Data Hold Time	t_{WH}	BUCK rising reference	20	—	—	
PRTY Data Access Time	t_{BA}	BUCK falling reference	0	—	—	
Data Disable Time	t_{SZ2}	BUCK falling reference	0	—	—	
Read Data Access Time	t_{RD}	BUCK falling reference	0	—	—	
Data Disable Time	t_{SZ3}	BUCK rising reference	0	—	—	

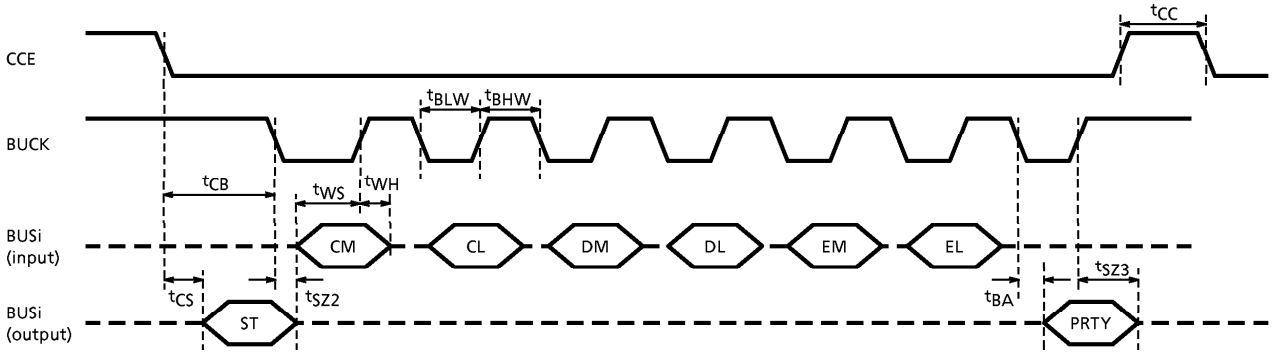
(a) Idle mode



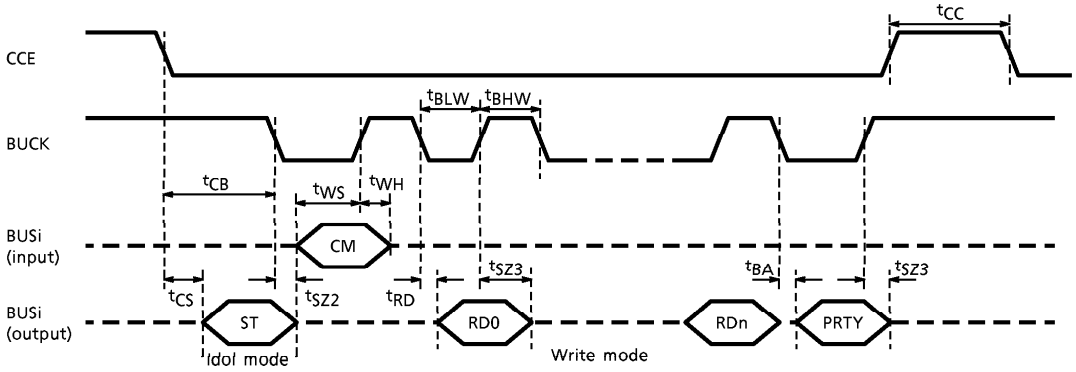
(b) Write command mode



BXXXXX, FXXXXX command at

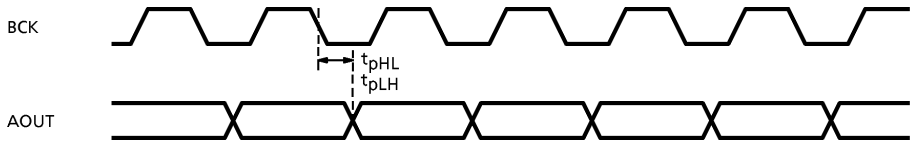


(c) Read command mode



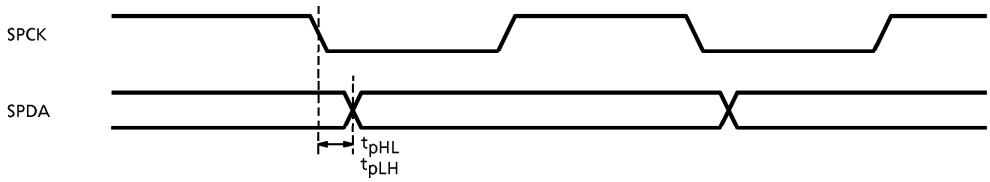
2. AOUT terminal output data timing

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time (1)	"H" Level	t_{pLH}	BCK→AOUT	—	—	5	ns
	"L" Level	t_{pHL}		—	—	5	



3. SPDA output timing

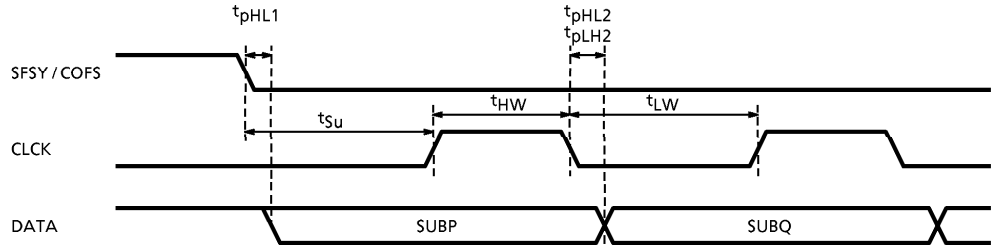
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pLH}	SPCK→SPDA	—	3	—	ns
	"L" Level	t_{pHL}		—	3	—	



4. DATA, CLCK input / output timing

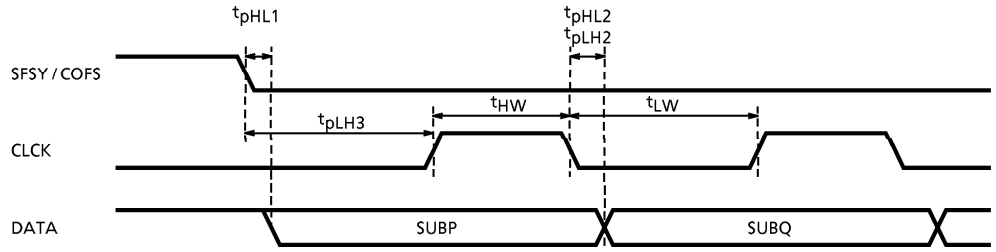
(a) CLCK input mode

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	CLCK input mode	200	—	—	ns
	"L" Level	t_{LW}		200	—	—	
Input Set-up Time		t_{Su}		200	—	—	
Transfer Time (1)	"L" Level	t_{pHL1}		—	—	5	
Transfer Time (2)	"H" Level	t_{pLH2}		—	—	20	
	"L" Level	t_{pHL2}		—	—	20	



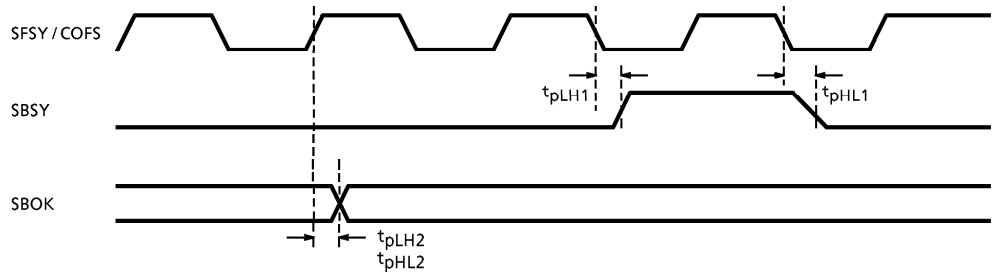
(b) CLCK output mode (t_{HW}, t_{LW}, t_{pLH3} ; 2 times speed = 1 / 2, 4 times speed = 1 / 4)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	CLCK output mode	—	—	1000	ns
	"L" Level	t_{LW}		—	—	1000	
Transfer Time (1)	"L" Level	t_{pHL1}		—	—	5	
Transfer Time (2)	"H" Level	t_{pLH2}		—	—	20	
	"L" Level	t_{pHL2}		—	—	20	
Transfer Time (3)	"H" Level	t_{pLH3}		—	—	900	



5. SBSY, SBOK input / output control

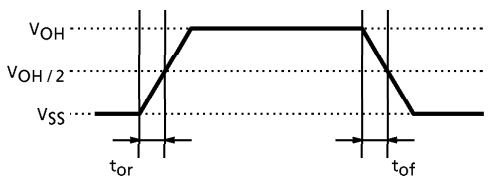
CHARACTERISTIC		SYNBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time (1)	"H" Level	t_{pLH1}	SBSY	—	—	5	ns
	"L" Level	t_{pHL1}		—	—	5	
Transfer Time (2)	"H" Level	t_{pLH2}	SBOK	—	—	15	
	"L" Level	t_{pHL2}		—	—	15	



6. Output terminal timing

CHARACTERISTIC	SYNBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Rising Time (1)	t_{or1}	Terminal (1)		—	—	20	ns
Output Falling Time (1)	t_{of1}			—	—	15	
Output Rising Time (2)	t_{or2}	Terminal (2)		—	—	20	
Output Falling Time (2)	t_{of2}			—	—	15	
Output Rising Time (3)	t_{or3}	Terminal (3)		—	—	20	
Output Falling Time (3)	t_{of3}			—	—	15	
Output Rising Time (4)	t_{or4}	Terminal (4)	$V_{REF} \rightarrow 2V_{REF}$	—	—	20	
			$V_{SS} \rightarrow V_{REF}$	—	—	10	
Output Falling Time (4)	t_{of4}		$2V_{REF} \rightarrow V_{REF}$	—	—	15	
			$V_{REF} \rightarrow V_{SS}$	—	—	10	

	TERMINAL NAME
(1) Terminal	AOUT, BCK, COFS, LRCK
(2) Terminal	BUS0, BUS1, BUS2, BUS3, CLCK
(3) Terminal	DATA, DOUT, EMPH, FLGA, FLGB, FLGC, FLGD, $\overline{HSO}$, IO0, IO1 IO2, IO3, IPF, MONIT, MBOV, SBOK, SBSY, SEL, SFSY, SPCK, $\overline{UHSO}$
(4) Terminal	PDO, TMAXS, TMAX, RFGC, TEBC, FMO, DMO, FVO



Analog circuit characteristics

1. A / D converter

CHARACTERISTIC		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution		—	—	8	—	bit
Sampling Frequency	FE	XI = 16.9344 MHz	—	176.4	—	kHz
	TE		—	176.4	—	kHz
	SBAD		—	88.2	—	kHz
	RFRP		—	176.4	—	kHz
Conversion Input Range		Ex. V_{SS} = 0 V, $2V_{REF}$ = 4.2 V	0.15 × $2V_{REF}$	—	0.85 × $2V_{REF}$	V

2. D / A converter (Focus, Tracking Equalizer output)

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Bit Number	—	—	5	—	bit
Sampling Frequency	—	—	2.8	—	MHz
Output Signal Range	—	AV_{SS}	—	$2V_{REF}$	V

3. PLL filter Amp.

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input / Output Signal Range	—	V_{SS}	—	$2V_{REF}$	V
Frequency Characteristics	– 3 dB point, RNF = 15 kΩ	2	4	—	MHz

4. VCO (PLL)

CHARACTERISTIC		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Center Oscillation Frequency		LPFO = V_{REF}, VCOREF = V_{REF}	—	34.6	—	MHz
Frequency Variation Range		VCOREF = V_{REF}, VCOGSL = "H"	± 40	± 50	—	%
		VCOREF = V_{REF}, VCOGSL = "L"	—	± 40	—	
VCOREF Terminal Input Voltage Range	upper limit	V_{REF} reference	—	—	1.0	V
	lower limit		– 0.5	—	—	

5. TEZI signal comparator

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Range	—	V_{SS}	—	$2V_{REF}$	V
Input Amplitude	—	1.0	—	3.5	V_{p-p}
Hysteresis Voltage	V_{REF} reference	—	100	—	mV

6. RFZI signal comparator

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Range	—	V_{SS}	—	$2V_{REF}$	V
Input Amplitude	—	1.0	—	3.5	V_{p-p}
Hysteresis Voltage	V_{REF} reference (no external register to RFCT terminal)	—	100	—	mV

7. Data slicer circuit

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
(Comparator)					
Input Amplitude	V_{REF} reference	—	1.2	2.0	V_{p-p}
Response Time	RFI = 0.6 V_{p-p}, f = 700 kHz	30	60	90	ns
(R-2R DAC)					
Output Conversion Range	—	1.58	—	2.59	V
Output Impedance	—	—	2.5	—	kΩ

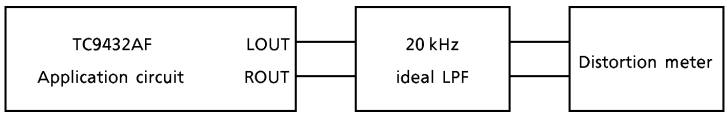
8. PWM converter output (RFGC, TEBC, FMO, FVO, DMO)

CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PWM Accuracy	—	—	8	—	bit
Sampling Frequency	—	—	88.2	—	kHz
Output Signal Range	—	AV_{SS}	—	$2V_{REF}$	V

DAC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Total Harmonic Distortion + Noise	THD + N	1	1 kHz sine wave, full scale input, PXI = "L"	—	− 85	− 80	dB
S / N Ratio	S / N	1	PXI = "L"	90	100	—	dB
Dynamic Range	DR	1	1 kHz sine wave, full scale input, PXI = "L"	85	90	—	dB
Cross Talk	CT	1	1 kHz sine wave, full scale input, PXI = "L"	—	− 90	− 85	dB
Analog Output Amplitude	DAC out	1	1 kHz sine wave, full scale input, PXI = "L"	1.12	1.20	1.28	V_{rms}

TEST CIRCUIT 1 : Application circuit is used.

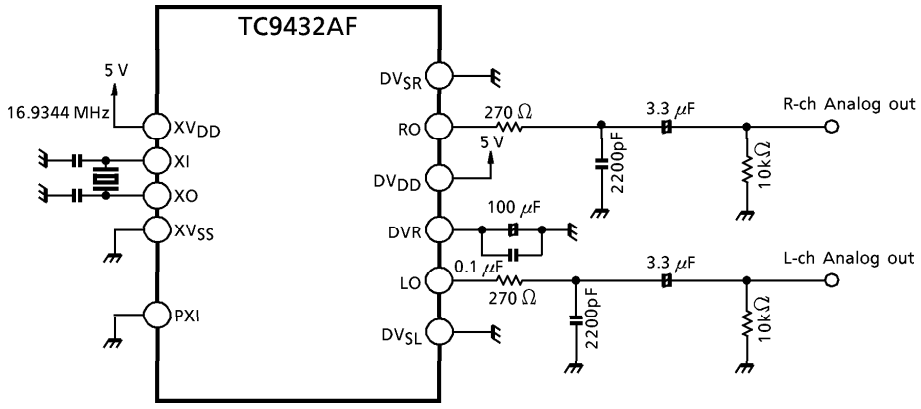


LPF : SHIBASOKU 725C
Distortion meter : SHIBASOKU 725C

CHARACTERISTICS	DISTORTION FILTER SETTING : A-WAIT
THD + N, CT	OFF
S / N, DR	ON

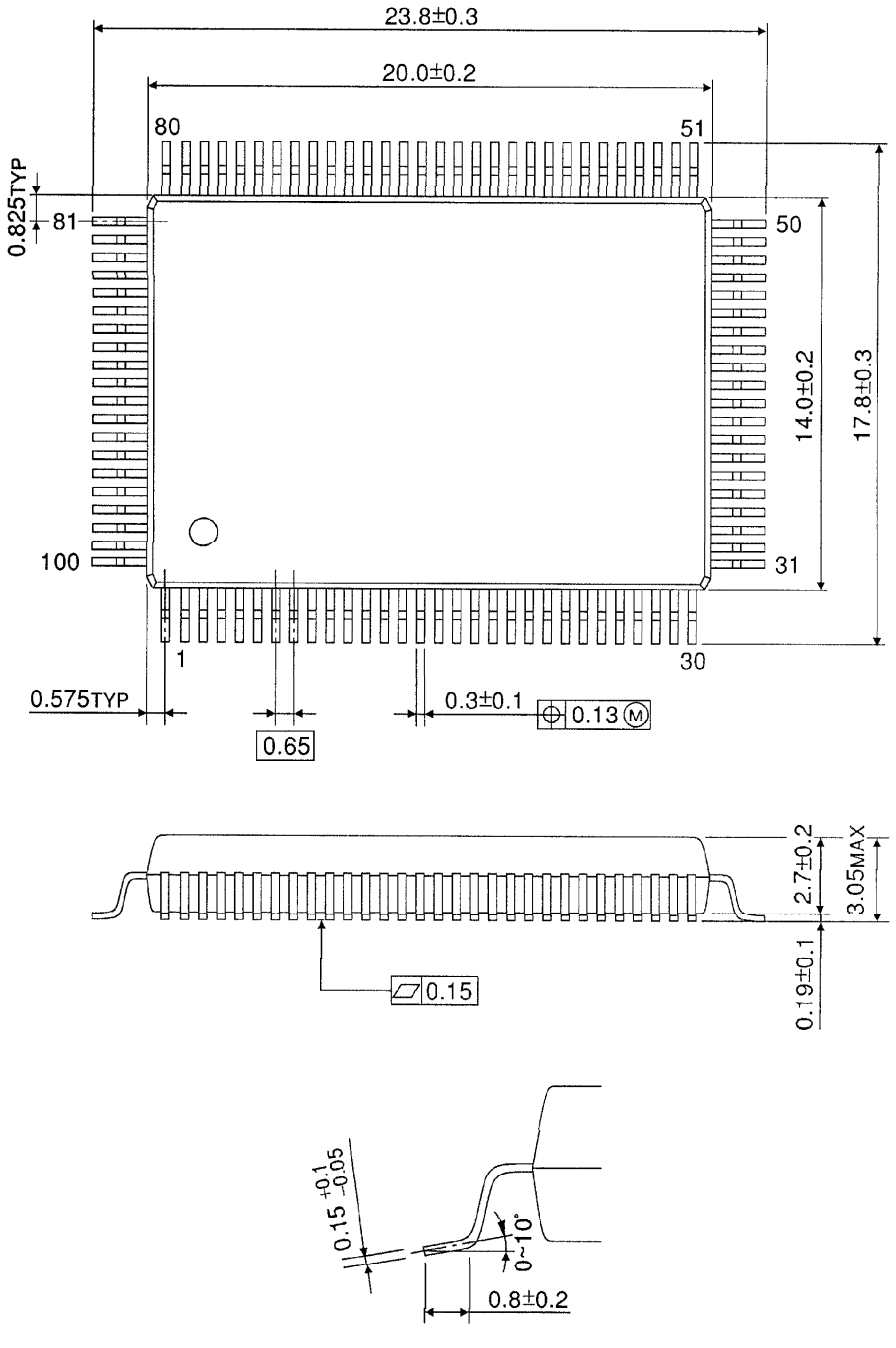
A-WAIT : IEC-A (corresponding)

APPLICATION CIRCUIT



OUTLINE DRAWING

QFP100-P-1420-0.65A Unit : mm



Weight : 1.6 g (Typ.)