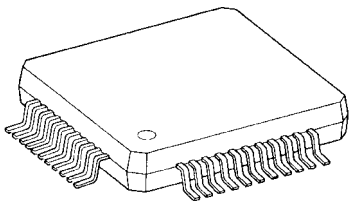
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9456F

Single Chip Surround LSI with a Built-in SRS

TC9456F is single Chip surround LSI with a built-in SRS for portable equipment, Mini compo.

As built-in ADC/DAC, Surround, Digital equalizer, bass boost and SRS of 3D sound reproduction technology, this IC constructs DSP function.



QFP44-P-1414-0.80D

Weight: 1.07 g (typ.)

Features

- Built-in 3channel AD converter.
  THD: −65dB S/N: 78dB (typ.)
  Built-in ope amp for pre-filter.
- Built-in 2channel DA converter.
  THD: −85dB S/N: 93dB (typ.)
  Built-in 3rd analog filter.
- Input: 3 analog channel, 1 digital stereo port.
  Digital input format: MSB first 16, 18, 20 bit effective data before change point of LRCK or I^2S.
- Output: 2 analog output/1 digital stereo port.
  Digital output format: MSB first 16, 20 bit effective data before change point of LRCK or I^2S.
- Built-in 64 Kbit delay RAM.
- DSP function
  - SRS: Eliminate existing sweet spot and restore spatial information, direction cues and other sonic nuance which are either missing or altered during and playback process.
    Correspondence only for fs = 44.1 kHz with SRS.
  - Surround: Real surround to use delay, simulate sound field of hole, church, stadium and etc.
  - Bass boost: Dynamic surround to respond an input
  - 3 Band parametric equalizer: Equalizer of a high precision of 18 bit coefficient
- Package is QFP 44 pins.

Note:

"The word 'SRS' and the SRS symbol (●) are registered trademarks of SRS Labs, Inc."

"Incorporates the SRS (Sound Retrieval System) under license from SRS Labs, Inc."

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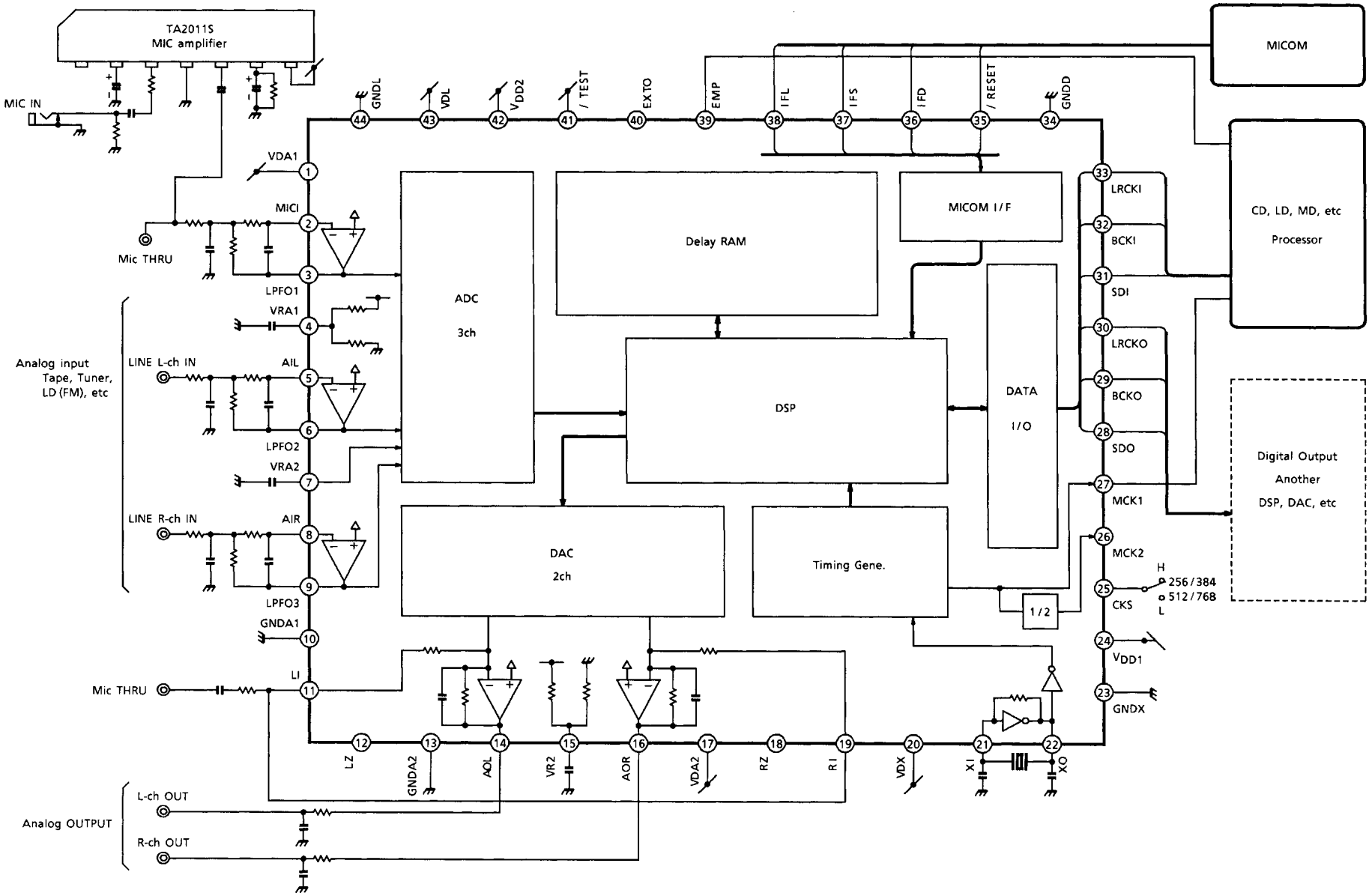
In order to purchase and implement the TC9456F, all customers must enter into a license agreement directly with SRS Labs for payment of royalties and to ensure proper trademark usage. Neither the purchase of the TC9456F, nor the corresponding sale of audio enhancement equipment conveys the right to sell commercialized recordings made with the SRS technology.

Block Diagram/Application Circuit



Terminal Description

No.	Terminal	I/O	Function	Remark
1	VDA1	—	ADC Voltage supply terminal.	
2	MICI	I	MIC LPF input terminal.	
3	LPFO1	O	MIC LPF output terminal.	
4	VRA1	—	ADC reference voltage terminal.	
5	AIL	I	LPF input terminal for L-ch Line input.	
6	LPFO2	O	LPF output terminal for L-ch Line input.	
7	VRA2	—	ADC reference voltage terminal.	
8	AIR	I	LPF input terminal for R-ch Line input.	
9	LPFO3	O	LPF output terminal for L-ch Line input.	
10	GNDA1	—	ADC GND terminal.	
11	LI	I	L-ch Analog additional input terminal. (when not using: OPEN)	
12	LZ	O	L-ch Digital input 0 detect terminal.	
13	GNDA2	—	DAC GND terminal.	
14	AOL	O	L-ch DAC output terminal.	
15	VR2	—	DAC reference voltage terminal.	
16	AOR	O	R-ch DAC output terminal.	
17	VDA2	—	DAC voltage supply terminal.	
18	RZ	O	R-ch Digital input 0 detect terminal.	
19	RI	I	R-ch Analog additional input terminal. (when not using: OPEN)	
20	VDX	—	Crystal oscillator voltage supply terminal.	
21	XI	I	Crystal oscillator connection terminal. (256, 384, 512, 768 fs)	
22	XO	O	Crystal oscillator connection terminal.	
23	GNDX	—	Crystal oscillator GND terminal.	
24	V_{DD1}	—	Digital voltage supply terminal.	
25	CKS	I	Master clock select terminal. (“H”: 256/384 fs, “L”: 512/768 fs)	
26	MCK2	O	1/2 divider clock output terminal.	
27	MCK1	O	Oscillator clock output terminal.	
28	SDO	O	Digital Audio Data output terminal.	
29	BCKO	O	Bit clock output terminal.	
30	LRCKO	O	Channel clock output terminal.	
31	SDI	I	Digital Audio Data input terminal.	
32	BCKI	I	Bit clock input terminal.	
33	LRCKI	I	Channel clock input terminal.	
34	GNDD	—	Digital GND terminal.	
35	$\overline{\text{RESET}}$	I	Reset terminal. (“L” reset active)	pull-up resister
36	IFD	I	μ-COM I/F data input terminal.	
37	IFS	I	μ-COM I/F data shift clock input terminal.	
38	IFL	I	μ-COM I/F latch pulse input terminal.	
39	EMP	I	De-emphasis filter setting terminal. (“H”: de-emphasis filter ON)	
40	EXTO	O	Extend output terminal.	

No.	Terminal	I/O	Function	Remark
41	$\overline{TEST}$	I	Test terminal. Usually “H”	pull-up resister
42	V_{DD2}	—	Digital Voltage supply terminal.	
43	VDL	—	Digital Voltage supply terminal for DRAM.	
44	GNDL	—	Digital GND terminal for DRAM.	

Block Operating Description

1. Operating Clock

Master clock (input or oscillating XI terminal) is 768/512/384/256 fs. These mode are selected by CKS terminal, and 256 fs or 384 fs, 768 fs or 512 fs select is auto detect by this IC.

But following internal synchronize mode can not use 384/768 fs, can only use 256/512 fs.

And DSP calculate steps don’t concern master clock, but DA converter operating clock change by master clock. DAC is Σ-Δ modulation method and operates oversampling, If 256 fs is selected, oversampling ratio is 128 fs and so became worse S/N, THD + N.

Table 1.1 Master Clock Select and DAC Oversampling Ratio.

CKS	Master Clock	DAC Oversampling Ratio
L	768 fs	192 fs
	512 fs	256 fs
H	384 fs	192 fs
	256 fs	128 fs

2. Digital Audio Input/Output

2.1 Synchronize Mode

Data input/output Bit clock is selected internal synchronize or external synchronize by “SYNM1”, “SYNM2”. (μ-COM I/F bit)

Table 2.1.1 Synchronize Mode and Input/Output Bit Clock.

SYNM2	SYNM1	Synchronize	BCKI	BCKO
0	0	internal	(Note 1)	64 fs (Note 2)
0	1	external	32 fs	BCKI
1	0	external	48 fs	BCKI
1	1	external	64 fs	BCKI

Note 1: Table 2.2.1 shown.

Note 2: Internal clock divider.

Input/Output channel clock (LRCKI, LRCKO) data is selected by μ-COM I/F. (RLS bit)

Table 2.1.2 Channel Clock

RLS	Operate
0	LRCKI, LRCKO: “H” Level, L-ch data input/output
1	LRCKI, LRCKO: “L” Level, L-ch data input/output

2.2 Data Input Format

Data input format is Table 2.2.1 and Figure 1.
Selecting use IBIT1 and IBIT2. (μ-COM I/F)

Table 2.2.1 Data Input Format

SYNM2	SYNM1	IBIT2	IBIT1		Format	BCKI
0	0	0	0	INTERNAL SYNCHRONIZE	MSBfirst 16 bit	32 fs~128 fs
0	0	0	1		MSBfirst 18 bit	36 fs~128 fs
0	0	1	0		MSBfirst 20 bit	40 fs~128 fs
0	0	1	1		IIS MAX20 bit	64 fs only
0	1	0	0	EXTERNAL SYNCHRONIZE	MSBfirst 16 bit	32 fs
0	1	0	1		not use	32 fs
0	1	1	0		not use	32 fs
0	1	1	1		not use	32 fs
1	0	0	0		MSBfirst 16 bit	48 fs
1	0	0	1		MSBfirst 18 bit	48 fs
1	0	1	0		MSBfirst 20 bit	48 fs
1	0	1	1		not use	48 fs
1	1	0	0		MSBfirst 16 bit	64 fs
1	1	0	1		MSBfirst 18 bit	64 fs
1	1	1	0		MSBfirst 20 bit	64 fs
1	1	1	1		IIS MAX20 bit	64 fs

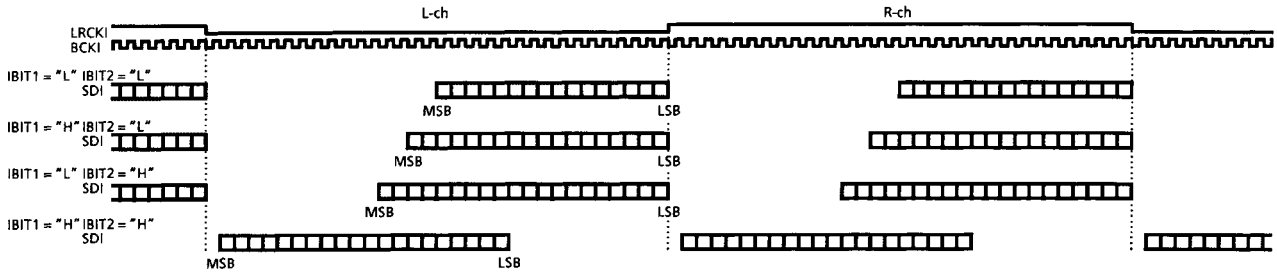


Figure 1 Example Data Input Timing (RLS = "H", SYNM1 = "H", SYNM2 = "H")

2.3 Digital Zero Detect Function

Table 2.3.1 Digital Zero Detect Judge Time

fs	32 kHz	44.1 kHz	48 kHz
Judge Time	1024 ms	743 ms	683 ms

Note 3: Correspondence only for 44.1kHz with SRS

2.4 Stereo/Mono Setting

This IC can input Double music source by "MONO", "CHS" bit. (μ-COM I/F)

And this IC can input Double music source by software coefficient, too. Please show Program manual.

Table 2.4.1 Stereo/Mono Setting

MONO	CHS	Stereo/MONO
0	0	stereo
0	1	ZERO Detect not use ("L" output only)
1	0	L-ch (CH1) MONO OUTPUT
1	1	R-ch (CH2) MONO OUTPUT

2.5 Data Output Formats

Table 2.5.1 Data Output Formats

SYNM2	SYNM1	OBIT2	OBIT1		Format	BCKO
0	0	0	0	INTERNAL SYNCHRONIZE	MSBfirst 16 bit	64 fs
0	0	0	1		MSBfirst 20 bit	64 fs
0	0	1	0		IIS 16 bit	64 fs
0	0	1	1		IIS 20 bit	64 fs
0	1	0	0	EXTERNAL SYNCHRONIZE	MSBfirst 16 bit	32 fs (= BCKI)
0	1	0	1		not use	32 fs (= BCKI)
0	1	1	0		IIS 16 bit	32 fs (= BCKI)
0	1	1	1		not use	32 fs (= BCKI)
1	0	0	0		MSBfirst 16 bit	48 fs (= BCKI)
1	0	0	1		MSBfirst 20 bit	48 fs (= BCKI)
1	0	1	0		IIS 16 bit	48 fs (= BCKI)
1	0	1	1		IIS 20 bit	48 fs (= BCKI)
1	1	0	0		MSBfirst 16 bit	64 fs (= BCKI)
1	1	0	1		MSBfirst 20 bit	64 fs (= BCKI)
1	1	1	0		IIS 16 bit	64 fs (= BCKI)
1	1	1	1		IIS 20 bit	64 fs (= BCKI)

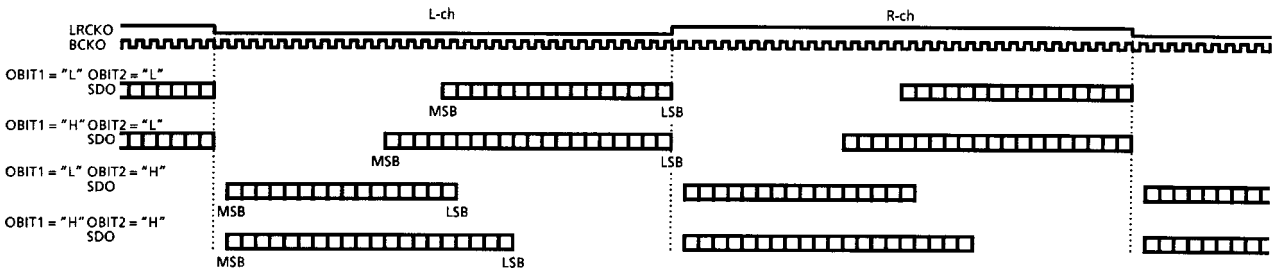


Figure 2 Example Data Output Timing (RLS = "H", SYNM1 = "H", SYNM2 = "H")

3. μ-COM I/F

3.1 Setting

μ-COM I/F setting is 4 Items.

Command is variable length 16~26 bits. (effective data before change point latch pulse)

When command is 8 bits unit, setting is LSB first.

All this IC's setting change at internal program cycle beginning, but without digital attenuator setting, please mute output signal at changing program setting.

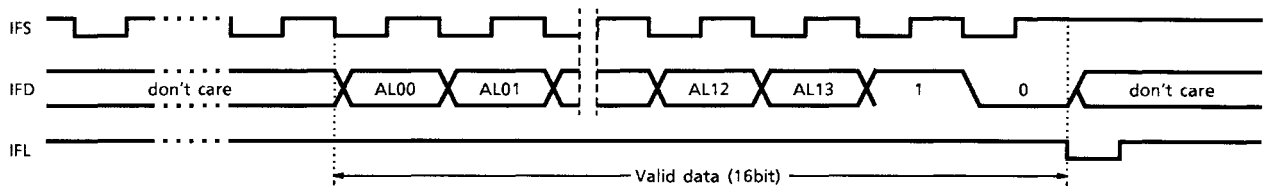
So Coefficient setting and offset RAM writing is one word at a fs.

When many word change, please by careful.

Table 3.1.1 μ-COM I/F Setting

	MODE	FUNC.	ATT.	CRAM	
D25	0	0	0	1	
D24	0	0	1	AD6	
D23	1	1	AL13	AD5	
D22	0	1	AL12	AD4	
D21	CHS	EMS	AL11	AD3	
D20	MONO	EM2	AL10	AD2	
D19	OBIT2	EM1	AL09	AD1	
D18	OBIT1	CEF2	AL08	AD0	1 byte
D17	IBIT2	CEF1	AL07	DT17	
D16	IBIT1	CTDW	AL06	DT16	
D15	SYNM2	CTUP	AL05	DT15	
D14	SYNM1	MUTE	AL04	DT14	
D13	RLS	EXTO	AL03	DT13	
D12	LSM	MSS	AL02	DT12	
D11	RESERVED	DF2	AL01	DT11	
D10	ADPD	DF1	AL00	DT10	2 byte
D09	—	—	—	DT09	
D08	—	—	—	DT08	
D07	—	—	—	DT07	
D06	—	—	—	DT06	
D05	—	—	—	DT05	
D04	—	—	—	DT04	
D03	—	—	—	DT03	
D02	—	—	—	DT02	3 byte
D01	—	—	—	DT01	
D00	—	—	—	DT00	

(1) Digital attenuator (16 bit command)



(2) Coefficient offset RAM writing (26 bit command)

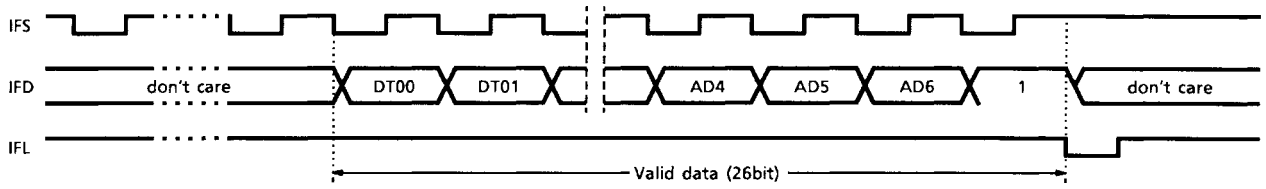


Figure 3 Example μ-COM I/F

3.2 Operating Mode Setting [MODE]

Please set these mode at voltage supply.
When $\overline{\text{RESET}}$ is "L", these data is clear.
ADPD: ADC power down (H: power down)
RESERVED: "L"
LSM: Digital Attenuator soft mute time select ("H": twice)
RLS: Channel clock select (H: LRCK = "L" is L-ch data)
SYNM1, 2: DATA input/output synchronize clock select
IBIT1, 2: Input DATA format select
OBIT1, 2: Output DATA format select
MONO: MONO DATA input select
CHS: At MONO Setting, channel select, At stereo setting, zero detect setting

3.3 DSP Setting [FUNC]

At $\overline{\text{RESET}}$ terminal is "L" level, these data is clear.
DF1, 2: SFC, decimation ratio select
MSS: SRS stereo/mono select ("L": stereo, "H": mono)
EXTO: Expand output terminal OUTPUT DATA
MUTE: OUTPUT mute ("H": mute, ATT setting is hold)
CTUP: Attack time select
CTDW: Release time select
CEF1: "H"
CEF2: Bass Boost effect select ("H": large effect)
EM1, 2: De-emphasis filter select
EMS: "H"

Table 3.3.1 De-Emphasis Setting

Terminal	I/F Setting				
EMP	EMS	EM2	EM1	Function	
0	1	—	—	DAC DF	OFF
1	1	0	0		de-emphasis 44.1 kHz
1	1	0	1		OFF
1	1	1	0		de-emphasis 48 kHz
1	1	1	1		de-emphasis 32 kHz

3.4 Digital Attenuator Setting [ATT]

Table 3.4.1 Digital Attenuator Level Setting

AL [13: 00]	Output Level
3FFFH	−0.000dB
3FFDH	−0.001dB
3FFBH	−0.002dB
・・・	・・・
2D4EH	−3.000dB
・・・	・・・
2013H	−6.000dB
・・・	・・・
0002H	−78.268dB
0001H	−84.288dB
0000H	−∞dB

[Level setting]

AL [13:00] = 3FFFH*10^ (level/20)

Table 3.4.2 Digital Attenuator Mute Time

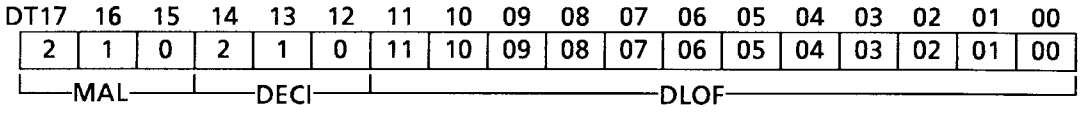
LSM	32 kHz	44.1 kHz	48 kHz
0	32 ms	23 ms	21 ms
1	64 ms	46 ms	42 ms

0dB (3FFFH)~−∞dB (0000H) Changing Time

Note 4: Correspondence only for 44.1 kHz with SRS

3.5 Coefficient, Offset RAM Writing [CRAM]

Coefficient and offset RAM writing operate one word at a fs.
RAM is 128 word × 18 bit.
Delay RAM Address offset data format is as follows.
Detail setting, please show soft ware manual.



MAL [2:0]: Delay RAM setting select

DECI [2:0]: Decimation ratio select

DLOF [11:00]: Offset address select

Figure 4 Coefficient, Offset RAM, Offset Address Setting

4. AD Converter

Built-in Line input L-ch and R-ch AD converter, and Mic signal input AD converter.

When not using AD converter, please short-circuit interval each terminal MICI-LPFO1, AIL-LPFO2 and AIR-LPFO3

5. DA Converter

This is Σ-Δ modulation 1 bit DA converter.

Built-in 3'rd analog Filter. It is possible to add analog through signal (LI and RI terminal) at the output portion of DAC. When not using LI and RI terminal, please do to open these.

6. Timing

6.1 Reset Timing

At power supply, please set $\overline{\text{RESET}}$ terminal "L" level at one time.

Power ON Reset Timing is as follows.

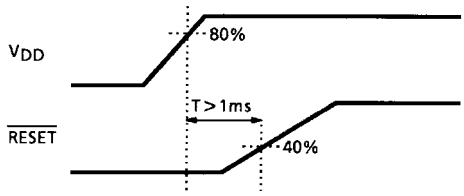
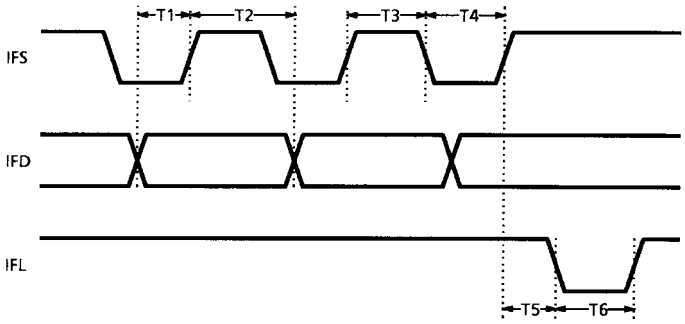


Figure 5 Power On Reset Timing

6.2 μ-COM I/F Timing



T1: Setup time > 1 μs

T2: Hold time > 1 μs

T3, T4, T6: Clock pulse width > 1 μs

T5: Hold time > 1 μs

Figure 6 μ-COM I/F Timing

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	1500	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−55~150	°C

Electrical Characteristics (DC)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V_{DD}	—	Ta = −40~85°C	4.5	5.0	5.5	V
Power supply current		I_{DD}	—	XI = 16.9 MHz, Output No-load	—	48	70	mA
Input voltage	"H" level	V_{IH}	—	Digital input terminal	V_{DD} × 0.8	—	V_{DD}	V
	"L" level	V_{IL}			0	—	V_{DD} × 0.2	
Input current	"H" level	I_{IH}	—	Digital input terminal	—	—	1.0	μA
	"L" level	I_{IL}			−1.0	—	—	
Output current 1	"H" level	I_{OH1}	—	LRCKO, BCKO, SDO	−3.5	—	—	mA
	"L" level	I_{OL1}			—	—	2.0	
Output current 2	"H" level	I_{OH2}	—	MCK1, MCK2	−5.0	—	—	mA
	"L" level	I_{OL2}			—	—	3.0	
Output current 3	"H" level	I_{OH3}	—	EXTO	−2.0	—	—	mA
	"L" level	I_{OL3}			—	—	2.0	
Pull-up resistance		RUP	—	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$	—	50	—	kΩ

Electrical Characteristics (AC)

AD Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input level	Ain	—	V_{DD} = 5.0 V	—	1.1	—	V_{rms}
S/(N + D) ratio	S/N (AD)	—	−30dB 1 kHz Sine wave input (Note 5)	68	78	—	dB
Total harmonic distortion + noise	THD (AD)	—	−0dB 1 kHz Sine wave input	—	−65	−55	dB
Cross-talk	CT (AD)	—	—	—	−68	−60	dB

Note 5: A-weight: ON (typ.)

DA Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output level	Aout	—	—	—	1.2	—	V_{rms}
S/N ratio	S/N (DA)	—	−0dB 1 kHz Sine wave input	87	93	—	dB
Total harmonic distortion + noise	THD1 (DA)	—	−0dB 1 kHz Sine wave input	—	−83	−78	dB
	THD2 (DA)		−0dB 10 kHz Sine wave input	—	−83	−75	
Cross-talk	CT (DA)	—	—	—	−88	−83	dB

Timing

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Rise time	t_r	—	LRCKO, BCKO, SDO, EXTO	—	—	15	ns
		—	MCK1, MCK2	—	—	8	
Fall time	t_f	—	LRCKO, BCKO, SDO, EXTO	—	—	15	ns
		—	MCK1, MCK2	—	—	8	
Delay time	t_d	—	LRCKI → LRCKO (external clock synchronous)	—	—	30	ns
		—	BCKI → BCKO (external clock synchronous)	—	—	20	
		—	BCKO → SDO	—	—	10	
		—	MCK1 → LRCKO (internal clock synchronous)	—	—	50	
		—	MCK1 → BCKO (internal clock synchronous)	—	—	20	
Operating frequency	f_{opr}	—	XI = 256 fs	8.0	11.3	12.5	MHz
			XI = 384 fs	10.0	16.9	18.5	
			XI = 512 fs	16.0	22.6	25.5	
			XI = 768 fs	24.0	33.9	34.0	

Note 6: At the external clock synchronous, LRCKO and BCKO output signal are same as LRCKI and BCKI input signal.

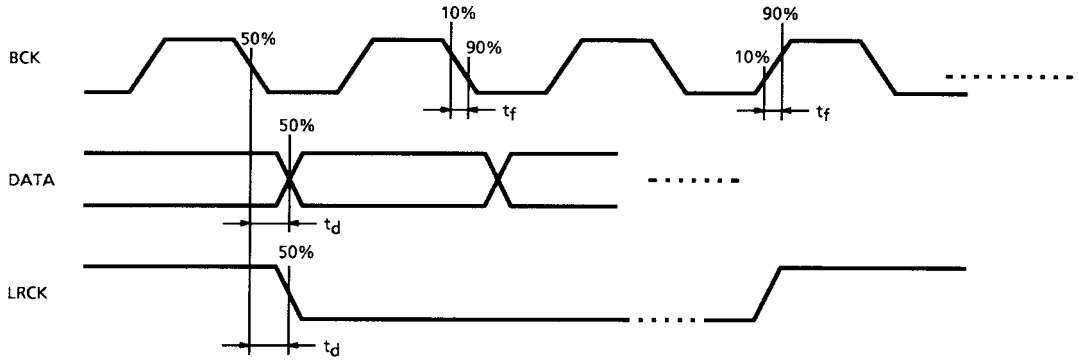
At the internal clock synchronous, LRCKO and BCKO output signal are output synchronously with the falling edge of MCK1.

Note 7: Measured with the output load CL = 10 pF.

Note 8: At the XI clock is 256 fs, 384 fs and 512 fs, it is operated with the fs = 32 kHz, 44.1 kHz and 48 kHz. At the XI clock is 768 fs, it is operated with the fs = 32 kHz and 44.1 kHz.

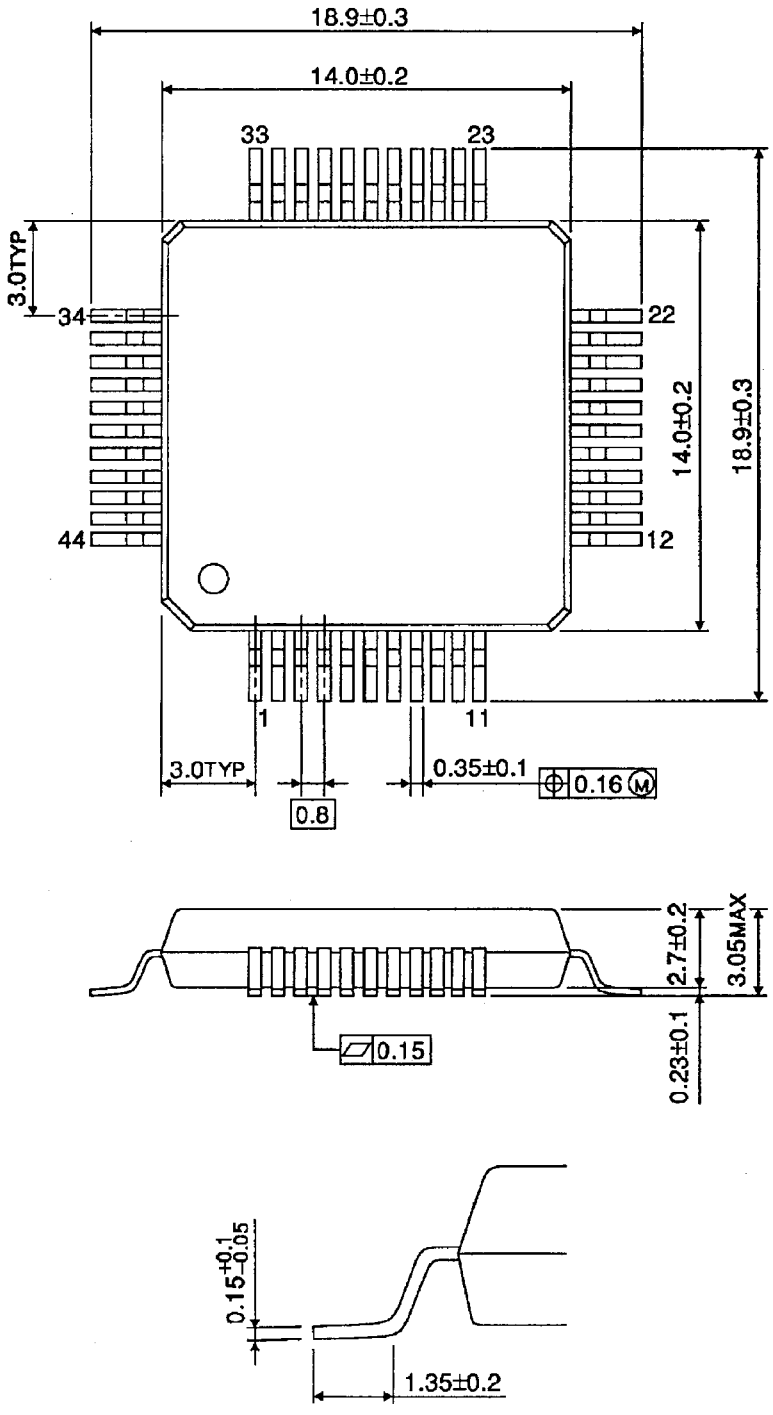
Note 9: Delay RAM applications has limitations with the how to control the DRAM. Show the software manual.

AC Characteristic Point (input signal: LRCK, BCK, DATA)



Package Dimensions

QFP44-P-1414-0.80D Unit : mm



Weight: 1.07 g (typ.)

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