

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC94A14F, TC94A14FA, TC94A14FB

Digital Servo Single-Chip Processor for Use in CD Player

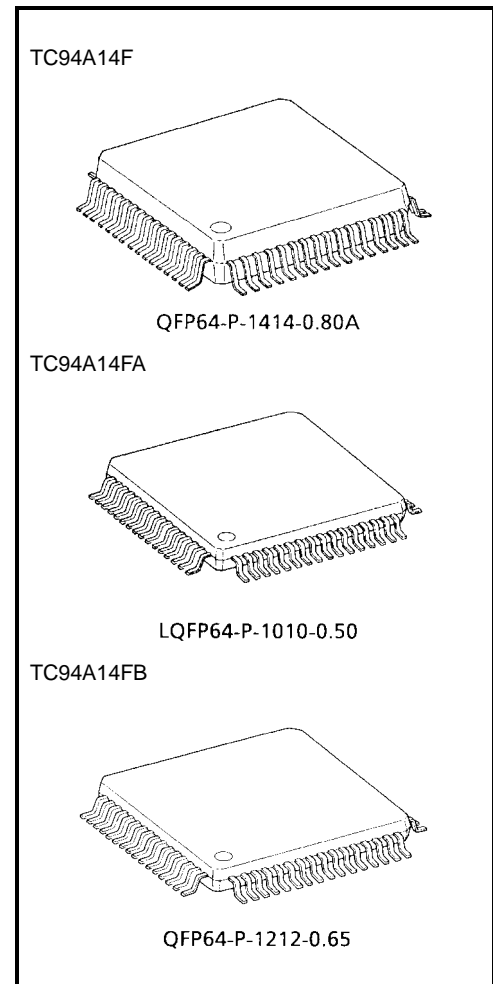
TC94A14F/FA/FB is a single-chip processor which incorporates the following functions: sync separation protection, interpolation, EFM decoder, error correction, micro controller interface, digital equalizer for use in servo LSI, and servo control circuit.

TC94A14F/FA/FB also incorporates a 1-bit DA converter.

Combining TC94A14F/FA/FB with digital servo head amp TA2157F/FN enables very simple and completely adjustment-free CD player systems.

Features

- Capable of decoding the text data.
- Sync pattern detection, sync signal protection, and synchronization can be made correctly.
- Built-in EFM demodulation circuit and sub code demodulation.
- Capable of correcting dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- The TC94A14F/FA/FB respond to variable playback system.
- Jitter absorbing capacity of ± 6 frame.
- Built-in 16 KB RAM.
- Built-in digital out circuit.
- Built-in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Output format for audio out can be selected 32fs, 48fs or 64fs modes.
- Read-timing-free sub code Q data and capable of synchronous output with audio data.
- Built-in data slicer and analog PLL (adjustment-free VCO).
- Capable of automatic adjustment function of focus and tracking servos for loop gain, offset and balance.
- Built-in RF gain automatic adjustment circuit.
- Built-in digital equalizer for phase compensation.
- Built-in RAM for digital equalizer for coefficient, and capable of variable pickup.
- Built-in focus and tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Lens-kick and feed-kick are using speed-controlled form.
- Built-in AFC and APC circuits for CLV servo of disc motor.
- Built-in anti-defect and anti-shock circuit.
- Built-in 8 times over sampling digital filter and 1-bit DA converter.
- Built-in analog filter for 1-bit DA converter.
- Built-in zero data detection output circuit.
- The TC94A14F/FA capable of 4 times speed operation.
- Built-in micro controller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 64-pin flat package.



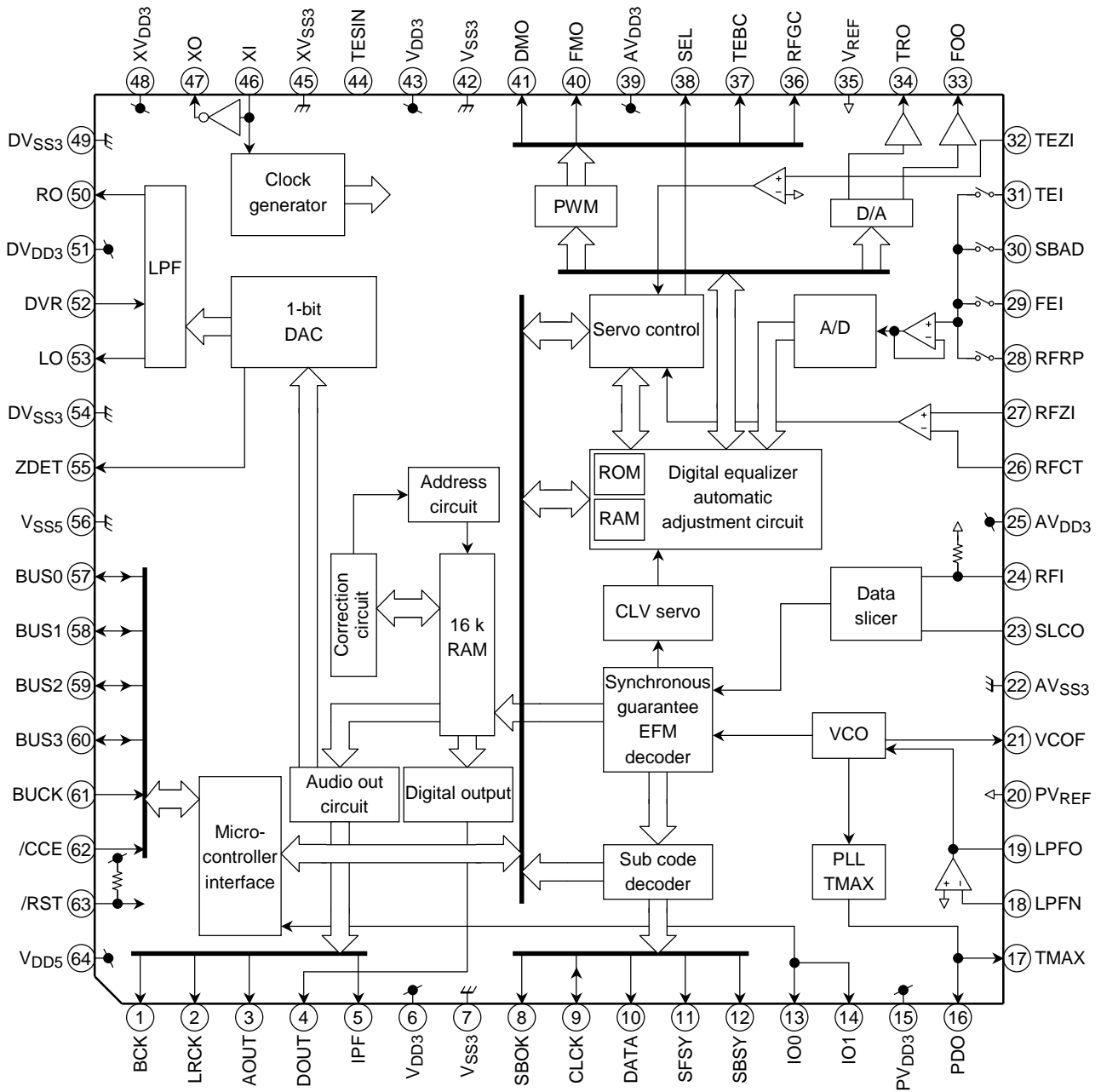
Weight

QFP64-P-1414-0.80A: 0.5 g (typ.)

LQFP64-P-1010-0.50: 0.4 g (typ.)

QFP64-P-1212-0.65: 0.45 g (typ.)

Block Diagram (top view)



Pin Functions

| Pin No. | Symbol | I/O | Function Description | Remarks | | | | | | | | |
|---------------------------|----------------------|---------------|--|---|-------------|--------------------------|----------------------|---------------------|-------|---------------------------|----------------------|---|
| 1 | BCK | O 3-5I/F | Bit clock output pin. 32fs, 48fs, or 64fs selectable by command. | Normal speed: 32fs = 1.4112 MHz | | | | | | | | |
| 2 | LRCK | O 3-5I/F | L/R channel clock output pin. "L" for L channel and "H" for R channel. Output polarity can be inverted by command. | Normal speed: 44.1 kHz | | | | | | | | |
| 3 | AOUT | O 3-5I/F | Audio data output pin. MSB-first or LSB-first selectable by command. | — | | | | | | | | |
| 4 | DOUT | O 3-5I/F | Digital data output pin. Outputs up to double-speed playback. | Based on CP-1201 | | | | | | | | |
| 5 | IPF | O 3-5I/F | Correction flag output pin. When set to "H", AOUT output cannot be corrected by C2 correction processing. | Alias: C2PO | | | | | | | | |
| 6 | V _{DD3} | — | Digital 3.3 V power supply voltage pin. | — | | | | | | | | |
| 7 | V _{SS3} | — | Digital GND pin. | — | | | | | | | | |
| 8 | SBOK | O 3-5I/F | Subcode Q data CRCC result output pin. "H" level when result is OK. | — | | | | | | | | |
| 9 | CLCK | I/O 3-5I/F | Subcode P-W data read clock I/O pin. I/O polarity selectable by command. | Schmitt input | | | | | | | | |
| 10 | DATA | O 3-5I/F | Subcode P-W data output pin. | — | | | | | | | | |
| 11 | SFSY | O 3-5I/F | Playback frame sync signal output pin. | — | | | | | | | | |
| 12 | SBSY | O 3-5I/F | Subcode block sync signal output pin. "H" level at S1 when subcode sync is detected. | — | | | | | | | | |
| 13 | IO0 | I/O 3-5I/F | General-purpose input / output pins. Input port at reset. | Schmitt at input | | | | | | | | |
| 14 | IO1 | | | | | | | | | | | |
| 15 | PV _{DD3} | — | PLL-only 3.3 V power supply voltage pin. | — | | | | | | | | |
| 16 | PDO | O AI/F | EFM and PLCK phase difference signal output pin. | 4-state output (PV _{DD3} , HiZ, PV _{REF} , AV _{SS3}) | | | | | | | | |
| 17 | TMAX | O AI/F | <p>TMAX detection result output pin.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TMAX Detection Result</th> <th>TMAX Output</th> </tr> </thead> <tbody> <tr> <td>Longer than fixed period</td> <td>"PV_{DD3}"</td> </tr> <tr> <td>Within fixed period</td> <td>"HiZ"</td> </tr> <tr> <td>Shorter than fixed period</td> <td>"AV_{SS3}"</td> </tr> </tbody> </table> | TMAX Detection Result | TMAX Output | Longer than fixed period | "PV _{DD3} " | Within fixed period | "HiZ" | Shorter than fixed period | "AV _{SS3} " | 3-state output (PV _{DD3} , HiZ, AV _{SS3}) |
| TMAX Detection Result | TMAX Output | | | | | | | | | | | |
| Longer than fixed period | "PV _{DD3} " | | | | | | | | | | | |
| Within fixed period | "HiZ" | | | | | | | | | | | |
| Shorter than fixed period | "AV _{SS3} " | | | | | | | | | | | |
| 18 | LPFN | I AI/F | Inverted input pin for PLL LPF amp. | Analog input | | | | | | | | |
| 19 | LPFO | O AI/F | Output pin for PLL LPF amp. | Analog output | | | | | | | | |
| 20 | PV _{REF} | — | PLL-only V _{REF} pin. | — | | | | | | | | |
| 21 | VCOF | O AI/F | VCO filter pin. | Analog output | | | | | | | | |
| 22 | AV _{SS3} | — | Analog GND pin. | — | | | | | | | | |
| 23 | SLCO | O AI/F | DAC output pin for data slice level generation. | Analog output | | | | | | | | |
| 24 | RFI | I AI/F | RF signal input pin. Zin selectable by command. | Analog input | | | | | | | | |
| 25 | AV _{DD3} | — | Analog 3.3 V power supply voltage pin. | — | | | | | | | | |

| Pin No. | Symbol | I/O | Function Description | Remarks |
|---------|--------|-----------|--|--|
| 26 | RFCT | I AI/F | RFRP signal center level input pin. | Analog input: Zin = 33 kΩ |
| 27 | RFZI | I AI/F | RFRP signal zero-cross input pin. | Analog input |
| 28 | RFRP | I AI/F | RF ripple signal input pin. | Analog input |
| 29 | FEI | I AI/F | Focus error signal input pin. | Analog input |
| 30 | SBAD | I AI/F | Sub-beam adder signal input pin. | Analog input |
| 31 | TEI | I AI/F | Tracking error input pin. Inputs when tracking servo is on. | Analog input |
| 32 | TEZI | I AI/F | Tracking error signal zero-cross input pin. | Analog input: Zin = 10 kΩ |
| 33 | FOO | O AI/F | Focus equalizer output pin. | Analog output (AVSS3~AVDD3) |
| 34 | TRO | O AI/F | Tracking equalizer output pin. | |
| 35 | VREF | — | Analog reference power supply voltage pin. | — |
| 36 | RFGC | O AI/F | RF amplitude adjustment control signal output pin. | 3-state output (PWM carrier = 88.2 kHz) (AVDD3, VREF, AVSS3) |
| 37 | TEBC | O AI/F | Tracking balance control signal output pin. | |
| 38 | SEL | O AI/F | APC circuit ON/OFF signal output pin. At laser on, high impedance with UHS = "L", H output with UHS = "H". | 3-state output |
| 39 | AVDD3 | — | Analog 3.3 V power supply voltage pin. | — |
| 40 | FMO | O AI/F | Feed equalizer output pin. | 3-state output (PWM carrier = 88.2 kHz) (AVDD3, VREF, AVSS3) |
| 41 | DMO | O AI/F | Disc equalizer output pin. | |
| 42 | VSS3 | — | Digital GND pin. | — |
| 43 | VDD3 | — | Digital 3.3 V power supply voltage pin. | — |
| 44 | TESIN | I 3I/F | Test input pin. Normally, fixed to "L". | — |
| 45 | XVSS3 | — | System clock oscillator GND pin. | — |
| 46 | XI | I AI/F | System clock oscillator input pin. | — |
| 47 | XO | O AI/F | System clock oscillator output pin. | — |
| 48 | XVDD3 | — | System clock oscillator 3.3 V power supply voltage pin. | — |
| 49 | DVSS3 | — | DA converter GND pin. | — |
| 50 | RO | O AI/F | R-channel data forward output pin. | — |
| 51 | DVDD3 | — | DA converter 3.3 V power supply pin. | — |
| 52 | DVR | — | Reference voltage pin. | — |
| 53 | LO | O AI/F | L-channel data forward output pin. | — |
| 54 | DVSS3 | — | DA converter GND pin. | — |

| Pin No. | Symbol | I/O | Function Description | Remarks |
|---------|------------------|-------------------------|--|-----------------------------|
| 55 | ZDET | $\overset{O}{3-5I/F}$ | 1 bit DA converter zero data detection flag output pin. | — |
| 56 | V _{SS5} | — | Microcontroller interface GND pin. | — |
| 57 | BUS0 | $\overset{I/O}{3-5I/F}$ | Microcontroller interface data I/O pins. | Schmitt input CMOS ports |
| 58 | BUS1 | | | |
| 59 | BUS2 | | | |
| 60 | BUS3 | | | |
| 61 | BUCK | $\overset{I}{3-5I/F}$ | Microcontroller interface clock input pin. | Schmitt input |
| 62 | /CCE | $\overset{I}{3-5I/F}$ | Microcontroller interface chip enable signal input pin. At "L", BUS0 to BUS3 are active. | Schmitt input |
| 63 | /RST | $\overset{I}{3-5I/F}$ | Reset signal input pin. At reset, "L". | Built-in pull-up resistor |
| 64 | V _{DD5} | — | Microcontroller interface 5 V power supply pin. | — |

Note: AI/F: analog input/output pin
 3-5I/F: 3-5 interface built-in pin (5 V input/output pin)
 3I/F: 3 V input/output pin

Maximum Ratings (unless otherwise specified, GND reference, Ta = 25°C)

| Characteristics | Symbol | Rating | Unit | Remarks |
|-----------------------|------------------|-----------------------------|------|---|
| Power supply voltage | V _{DD5} | -0.3~6.0 | V | 64-56 pin |
| | V _{DD3} | -0.3~4.5 | | 6-7 pin 15, 25, 39-22 pin 43-42 pin 48-45 pin 51-49, 54 pin |
| Input voltage | V _{IN5} | -0.3~V _{DD5} + 0.3 | V | 9, 13, 14, 57~63 pin |
| | V _{IN3} | -0.3~V _{DD3} + 0.3 | | 18, 24, 26~32, 44 pin |
| Power dissipation | P _D | 1910 | mW | TC94A14F |
| | | 1000 | | TC94A14FA |
| | | 1310 | | TC94A14FB |
| Operating temperature | T _{opr} | -40~+85 | °C | — |
| Storage temperature | T _{stg} | -55~+150 | °C | — |

Electrical Characteristics

DC Characteristics (1)

(unless otherwise specified, $V_{DD5} = 5\text{ V}$, $V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = PV_{DD3} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | |
|---------------------------------------|--|---------------|---------------|--|--|------|------|---------------|---------------|
| Operating power supply voltage | | V_{DD5} | — | — | 4.5 | 5.0 | 5.5 | V | |
| | | V_{DD3} | — | — | 3.0 | 3.3 | 3.6 | | |
| | | AV_{DD3} | — | — | | | | | |
| | | DV_{DD3} | — | — | | | | | |
| | | XV_{DD3} | — | — | | | | | |
| | | PV_{DD3} | — | — | | | | | |
| Operating power supply current | | Normal speed | I_{DD5} (1) | XI = 16.9344 MHz | — | 2 | 5 | mA | |
| | | | I_{DD3} (1) | | — | 30 | 50 | | |
| | | Double speed | I_{DD5} (2) | | — | 2.5 | 6 | | |
| | | | I_{DD3} (2) | | — | 35 | 60 | | |
| | | 4 times speed | I_{DD5} (3) | | — | 3 | 7 | | |
| | | | I_{DD3} (3) | | — | 40 | 70 | | |
| Input voltage 1 | | "H" level | V_{IH5} | CMOS input pins except for analog input pins (5 V) | 3.5 | — | — | V | |
| | | "L" level | V_{IL5} | | — | — | 1.5 | | |
| Input current 1 | | "H" level | I_{IH5} | $V_{IH5} = 5\text{ V}$ | — | — | 1.0 | μA | |
| | | "L" level | I_{IL5} | $V_{IL5} = 0\text{ V}$ | -1.0 | — | — | | |
| Tri-state leak current 1 | | "H" level | I_{TLH5} | $V_{IH5} = 5\text{ V}$ | Pins grouped as 1, 2, 3 in the following table | — | — | 1.0 | μA |
| | | "L" level | I_{TLL5} | $V_{IL5} = 0\text{ V}$ | | -1.0 | — | — | |
| Output current 1 | | "H" level | I_{OH5} (1) | $V_{OH5} = 4.6\text{ V}$ | Pins grouped as 1 in the following table | — | — | -2.0 | mA |
| | | "L" level | I_{OL5} (1) | $V_{OL5} = 0.4\text{ V}$ | | 2.0 | — | — | |
| | | "H" level | I_{OH5} (2) | $V_{OH5} = 4.6\text{ V}$ | Pins grouped as 2 and 3 in the following table | — | — | -4.0 | |
| | | "L" level | I_{OL5} (2) | $V_{OL5} = 0.4\text{ V}$ | | 4.0 | — | — | |
| Input voltage 2 | | "H" level | V_{IH3} | CMOS input pins except for analog input pins (3 V) | 2.3 | — | — | V | |
| | | "L" level | V_{IL3} | | — | — | 1.0 | | |
| Input current 2 | | "H" level | I_{IH3} | $V_{IH3} = 3.3\text{ V}$ | — | — | 1.0 | μA | |
| | | "L" level | I_{IL3} | $V_{IL3} = 0\text{ V}$ | -1.0 | — | — | | |
| Tri-state leak current 2 | | "H" level | I_{TLH3} | $V_{IH3} = 3.3\text{ V}$ | Pins grouped as 4 and 5 in the following table | — | — | 1.0 | μA |
| | | "L" level | I_{TLL3} | $V_{IL3} = 0\text{ V}$ | | -1.0 | — | — | |
| Output current 2 | | "H" level | I_{OH3} (1) | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 4 in the following table | — | — | -2.0 | mA |
| | | "L" level | I_{OL3} (1) | $V_{OL3} = 0.4\text{ V}$ | | 2.0 | — | — | |
| | | "H" level | I_{OH3} (2) | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 5 in the following table | — | -80 | — | μA |
| | | "L" level | I_{OL3} (2) | $V_{OL3} = 0.4\text{ V}$ | | — | 80 | — | |
| | | "H" level | I_{OH3} (3) | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 6 in the following table | — | -121 | — | |
| | | "L" level | I_{OL3} (3) | $V_{OL3} = 0.4\text{ V}$ | | — | 121 | — | |
| V _{REF} output on resistance | | R_{ON} | — | — | — | — | 500 | Ω | |
| Pull-up resistance | | R_{UP} | — | Pins grouped as 8 in the following table | 25 | 50 | 75 | k Ω | |
| Pin built-in output resistance | | R_{O1} | — | Pins grouped as 5 in the following table | — | 5.0 | — | k Ω | |
| | | R_{O2} | — | Pins grouped as 6 and 7 in the following table | — | 3.3 | — | | |

DC Characteristics (2)

(unless otherwise specified, $V_{DD5} = V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = PV_{DD3} = 3.3\text{ V}$,
 $T_a = 25^\circ\text{C}$)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | | |
|--------------------------------|--|---------------|---------------|--|---------------------------|--|------|------------------|---------------|---------------|
| Operating power supply voltage | | V_{DD5} | — | — | 3.0 | 3.3 | 3.6 | V | | |
| | | V_{DD3} | — | — | | | | | | |
| | | AV_{DD3} | — | — | | | | | | |
| | | DV_{DD3} | — | — | | | | | | |
| | | XV_{DD3} | — | — | | | | | | |
| | | PV_{DD3} | — | — | | | | | | |
| Operating power supply current | | Normal speed | $I_{DD3} (1)$ | — | — | 32 | 55 | mA | | |
| | | Double speed | $I_{DD3} (2)$ | — | $XI = 16.9344\text{ MHz}$ | — | 37.5 | | 66 | |
| | | 4 times speed | $I_{DD3} (3)$ | — | | — | 43 | | 77 | |
| Input voltage | | "H" level | V_{IH3} | — | | CMOS input pins except for analog input pins (3 V) | 2.3 | — | V | |
| | | "L" level | V_{IL3} | — | — | | — | 1.0 | | |
| Input current | | "H" level | I_{IH3} | — | $V_{IH3} = 3.3\text{ V}$ | — | — | 1.0 | μA | |
| | | "L" level | I_{IL3} | — | $V_{IL3} = 0\text{ V}$ | -1.0 | — | — | | |
| Tri-state leak current | | "H" level | I_{TLH3} | — | $V_{IH3} = 3.3\text{ V}$ | Pins grouped as 4 and 5 in the following table | — | — | 1.0 | μA |
| | | "L" level | I_{TLL3} | — | $V_{IL3} = 0\text{ V}$ | | -1.0 | — | — | |
| Output current | | "H" level | $I_{OH3} (1)$ | — | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 1 in the following table | — | — | -1.0 | mA |
| | | "L" level | $I_{OL3} (1)$ | — | $V_{OL3} = 0.4\text{ V}$ | | 1.0 | — | — | |
| | | "H" level | $I_{OH3} (2)$ | — | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 2 and 3 in the following table | — | — | -2.0 | mA |
| | | "L" level | $I_{OL3} (2)$ | — | $V_{OL3} = 0.4\text{ V}$ | | 2.0 | — | — | |
| | | "H" level | $I_{OH3} (3)$ | — | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 4 in the following table | — | — | -2.0 | mA |
| | | "L" level | $I_{OL3} (3)$ | — | $V_{OL3} = 0.4\text{ V}$ | | 2.0 | — | — | |
| | | "H" level | $I_{OH3} (4)$ | — | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 5 in the following table | — | -80 | — | μA |
| | | "L" level | $I_{OL3} (4)$ | — | $V_{OL3} = 0.4\text{ V}$ | | — | 80 | — | |
| | | "H" level | $I_{OH3} (5)$ | — | $V_{OH3} = 2.9\text{ V}$ | Pins grouped as 6 in the following table | — | -121 | — | μA |
| | | "L" level | $I_{OL3} (5)$ | — | $V_{OL3} = 0.4\text{ V}$ | | — | 121 | — | |
| VREF output on resistance | | R_{ON} | — | — | — | — | 500 | Ω | | |
| Pull-up resistance | | R_{UP} | — | Pins grouped as 8 in the following table | 50 | 80 | 120 | $\text{k}\Omega$ | | |
| Pin built-in output resistance | | R_{O1} | — | Pins grouped as 5 in the following table | — | 5.0 | — | $\text{k}\Omega$ | | |
| | | R_{O2} | — | Pins grouped as 6 and 7 in the following table | — | 3.3 | — | | | |

| Pin Group | Pin Name |
|-----------|--|
| 1 | SBOK, SFSY, SBSY, IO0, IO1, ZDET |
| 2 | BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA |
| 3 | BUS3, BUS2, BUS1, BUS0 |
| 4 | SEL, TMAX |
| 5 | PDO |
| 6 | RFGC, TEBC, FMO, DMO |
| 7 | FOO, TRO |
| 8 | /RST |

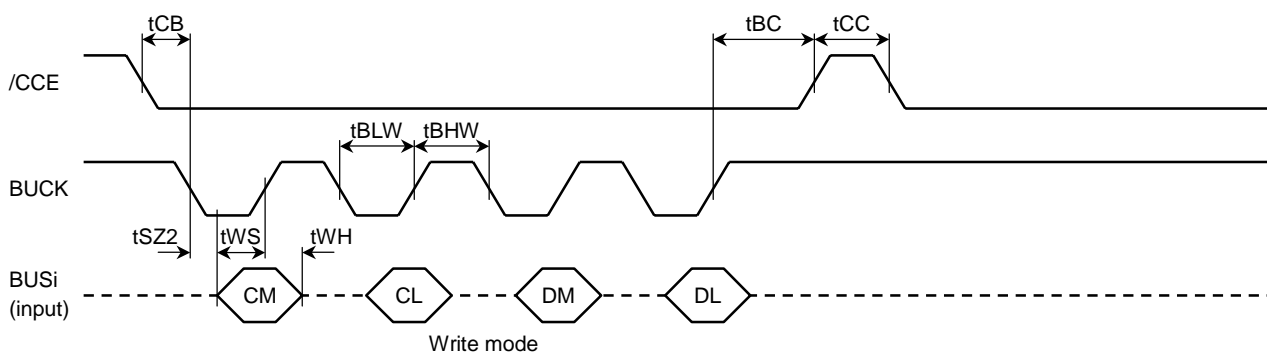
AC Characteristics

(unless otherwise specified, $V_{DD5} = 5\text{ V}$, $V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = PV_{DD3} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)

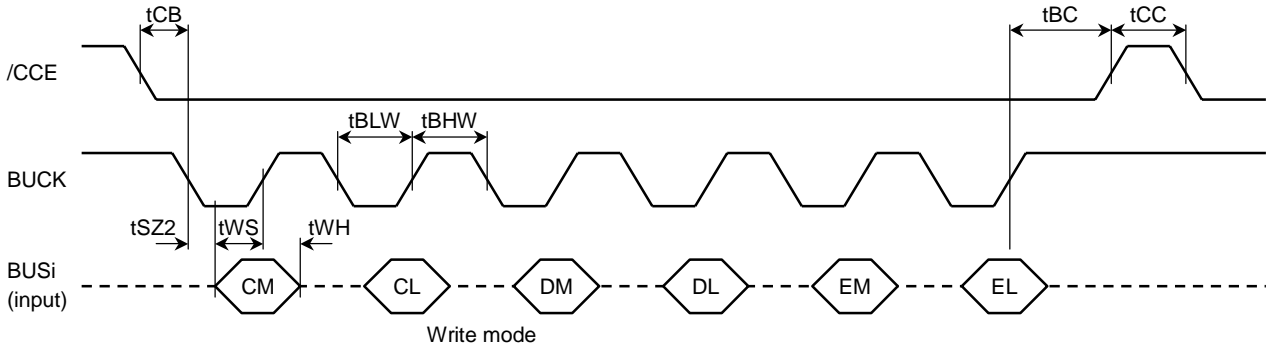
1. Microcontroller Interface Timing

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|----------------------------|--------|--------------|-------------------------------|------|------|-----|------|
| /CCE = "H" pulse width | tCC | — | — | 120 | — | — | ns |
| Data disable time | tSZ1 | — | BUCK rise reference | 0 | — | — | |
| /CCE, BUCK delay time | tCB | — | /CCE fall reference | 0 | — | — | |
| BUCK, /CCE delay time | tBC | — | BUCK rise reference | 0 | — | — | |
| BUCK = "L" pulse width | tBLW | — | Write, SRC mode | 120 | — | — | |
| | tBLW | — | QDRC mode | 240 | — | — | |
| BUCK = "H" pulse width (1) | tBHW | — | Write, SRC mode | 120 | — | — | |
| BUCK = "H" pulse width (2) | tBHW | — | QDRC mode (normal speed) | 3000 | — | — | |
| BUCK = "H" pulse width (3) | tBHW | — | QDRC mode (double speed) | 1500 | — | — | |
| BUCK = "H" pulse width (4) | tBHW | — | QDRC mode ($\times 4$ speed) | 800 | — | — | |
| Write data setup time | tWS | — | BUCK rise reference | 60 | — | — | |
| Write data hold time | tWH | — | BUCK rise reference | 20 | — | — | |
| Data disable time | tSZ2 | — | BUCK fall reference | 0 | — | — | |
| Read data access time | tRD | — | BUCK fall reference | 0 | — | — | |

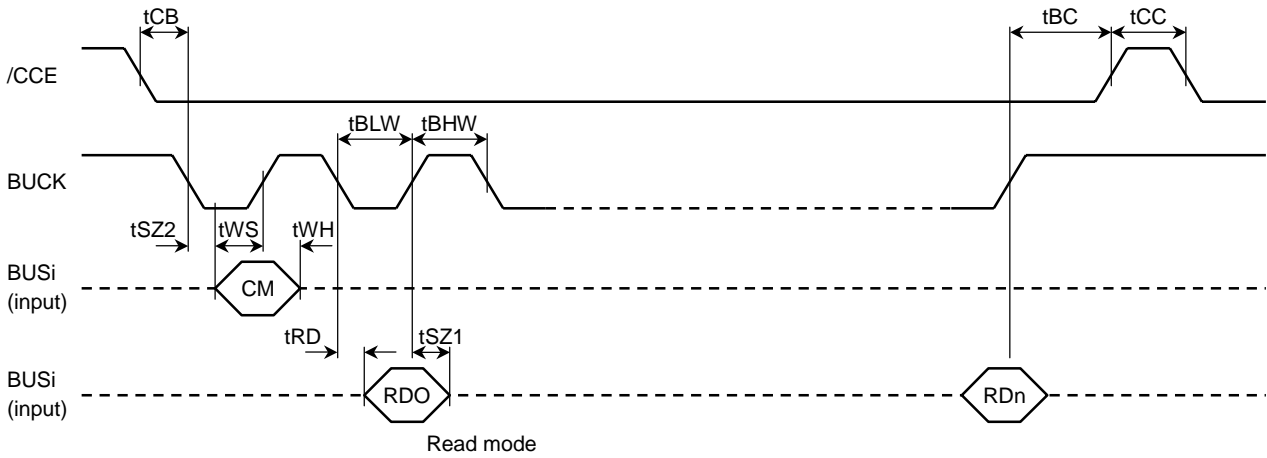
(1) Write command mode



(2) Write command mode: Bxxxxx, Fxxxxx commands

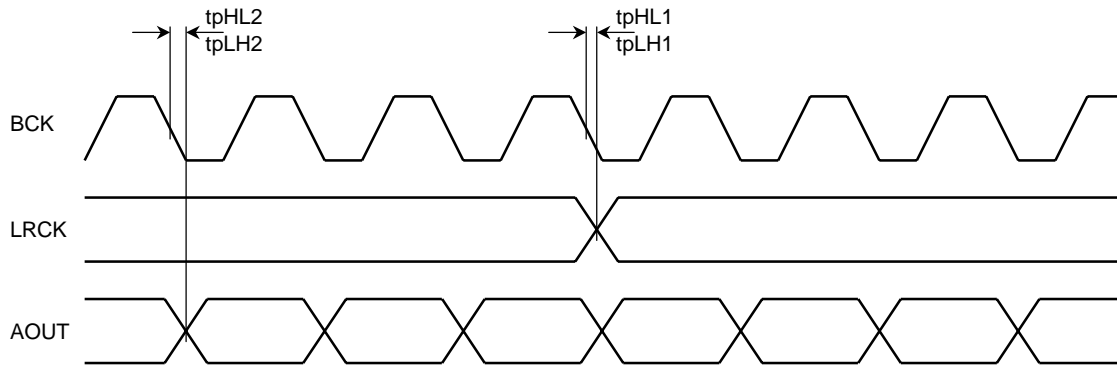


(3) Read command mode



2. AOUT Data Output Timing

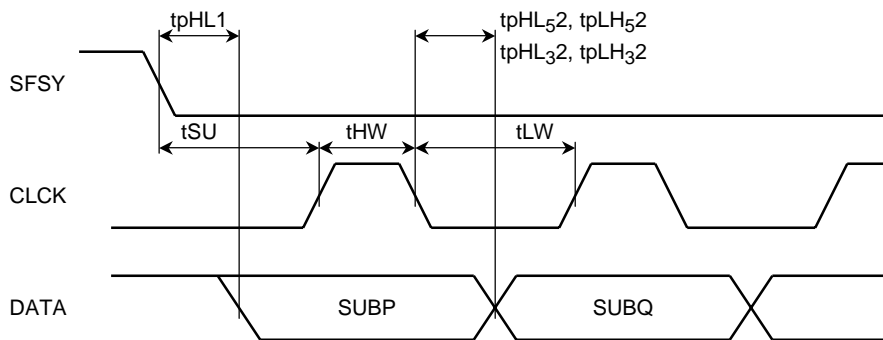
| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------|-----------|--------------|----------------|-----|------|-----|------|
| Transfer time (1) | "H" level | tpLH1 | LRCK | — | — | 5 | ns |
| | "L" level | tpHL1 | | — | — | 5 | |
| Transfer time (2) | "H" level | tpLH2 | AOUT | — | — | 5 | |
| | "L" level | tpHL2 | | — | — | 5 | |



3. DATA, CLCK Input/Output Timing

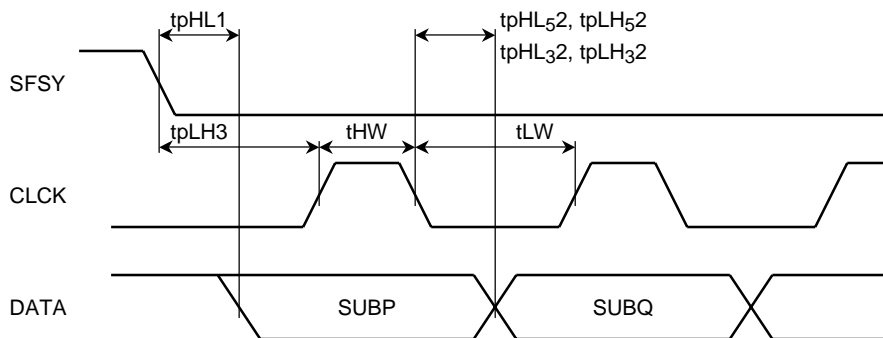
(1) CLCK input mode (regardless of setting of HS and UHS bits of SPEED command)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------|-----------|--------|--------------|--------------------------|-----|------|-----|------|
| Clock pulse width | "H" level | tHW | — | CLCK input mode | 50 | — | — | ns |
| | "L" level | tLW | — | | 50 | — | — | |
| Input setup time | | tSU | — | CLCK input mode | — | — | — | |
| Transfer time (1) | "L" level | tpHL1 | — | CLCK input mode | — | — | 5 | |
| Transfer time (2) | "H" level | tpLH52 | — | CLCK input mode | — | — | 15 | |
| | "L" level | tpHL52 | — | | — | — | 15 | |
| | "H" level | tpLH52 | — | V _{DD5} = 3.3 V | — | — | 20 | |
| | "L" level | tpHL52 | — | | — | — | 20 | |



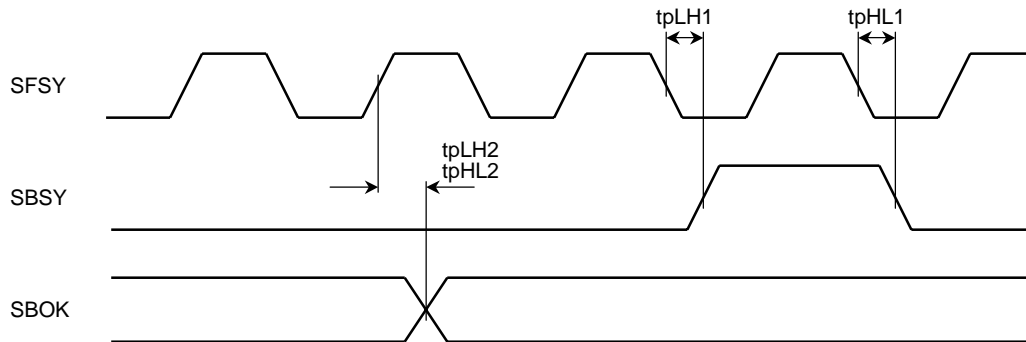
(2) CLCK output mode (tHW, tLW, tpLH3 only, × 1/n at × n speed)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------|-----------|--------|--------------|--------------------------|-----|------|-----|------|
| Clock pulse width | "H" level | tHW | — | CLCK output mode | — | — | 950 | ns |
| | "L" level | tLW | — | | — | — | 950 | |
| Transfer time (1) | "L" level | tpHL1 | — | CLCK output mode | — | — | 5 | |
| Transfer time (2) | "H" level | tpLH52 | — | CLCK output mode | — | — | 15 | |
| | "L" level | tpHL52 | — | | — | — | 15 | |
| | "H" level | tpLH32 | — | V _{DD5} = 3.3 V | — | — | 20 | |
| | "L" level | tpHL32 | — | | — | — | 20 | |
| Transfer time (3) | "H" level | tpLH3 | — | CLCK output mode | — | — | 850 | |



4. SBSY, SBOK Input/Output Timing

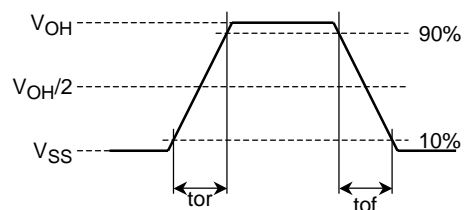
| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------|-----------|--------|--------------|----------------|-----|------|-----|------|
| Transfer time (1) | "H" level | tpLH1 | — | SBSY | — | — | 5 | ns |
| | "L" level | tpHL1 | — | | — | — | 10 | |
| Transfer time (2) | "H" level | tpLH2 | — | SBOK | — | — | 15 | |
| | "L" level | tpHL2 | — | | — | — | 20 | |



5. Output Pin Timing

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|------------------------|-------|--------|--------------|---|-----|------|-----|------|
| Output rise time 5 (1) | tor51 | — | — | Pins grouped as 1 below $V_{DD5} = 3.3\text{ V}$ | — | — | 7 | ns |
| Output fall time 5 (1) | tof51 | | | | — | — | 12 | |
| Output rise time 3 (1) | tor31 | | | | — | — | 14 | |
| Output fall time 3 (1) | tof31 | | | | — | — | 24 | |
| Output rise time 5 (2) | tor52 | — | — | Pins grouped as 2 below $V_{DD5} = 3.3\text{ V}$ | — | — | 7 | |
| Output fall time 5 (2) | tof52 | | | | — | — | 7 | |
| Output rise time 3 (2) | tor32 | | | | — | — | 14 | |
| Output fall time 3 (2) | tof32 | | | | — | — | 14 | |
| Output rise time 5 (3) | tor53 | — | — | Pins grouped as 3 below $V_{DD5} = 3.3\text{ V}$ | — | — | 7 | |
| Output fall time 5 (3) | tof53 | | | | — | — | 7 | |
| Output rise time 3 (3) | tor33 | | | | — | — | 14 | |
| Output fall time 3 (3) | tof33 | | | | — | — | 14 | |
| Output rise time 5 (4) | tor54 | — | — | Pins grouped as 4 below | — | — | 10 | |
| Output fall time 5 (4) | tof54 | — | — | | — | — | 10 | |

| Pin Group | Pin Name |
|-----------|--|
| 1 | SBOK, SFSY, SBSY, IO0, IO1, ZDET |
| 2 | BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA |
| 3 | BUS3, BUS2, BUS1, BUS0 |
| 4 | TMAX, SEL |



Analog Circuit Characteristics

1. AD Converter

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|------------------------|--------------|---|------------------------|-------|------------------------|------|
| Resolution | — | — | — | 8 | — | bit |
| Sampling frequency | FE | — | — | 176.4 | — | kHz |
| | TE | | — | 176.4 | — | |
| | SBAD | | — | 88.2 | — | |
| | RFRP | | — | 176.4 | — | |
| Conversion input range | — | $AV_{SS} = 0\text{ V}$ $AV_{DD3} = 3.3\text{ V}$ | $0.15 \times AV_{DD3}$ | — | $0.85 \times AV_{DD3}$ | V |

2. DA Converter (focus and tracking equalizer output)

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---------------------|--------------|--|------------|------|------------|------|
| Number of bits | — | — | — | — | 5 | bit |
| Sampling frequency | — | — | — | — | 2.8 | MHz |
| Signal output range | — | $AV_{SS} = 0\text{ V}$, $AV_{DD3} = 3.3\text{ V}$ | AV_{SS3} | — | AV_{DD3} | V |

3. PLL Filter Amp

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--------------------------|--------------|-----------------------|------------|------|------------|------|
| I/O signal range | — | — | AV_{SS3} | — | PV_{DD3} | V |
| Frequency characteristic | — | -3dB point (Gain = 1) | — | 8 | — | MHz |

4. VCO (PLL)

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|------------------------------|--------------|--------------------|-----|----------|-----|------|
| Center oscillation frequency | — | $LPFO = V_{REF}$ | — | 34 | — | MHz |
| Frequency variable range | — | [VCOGSL] bit = "L" | — | ± 50 | — | % |
| | — | [VCOGSL] bit = "H" | — | ± 60 | — | |

5. TEZI Signal Comparator

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--------------------|--------------|---------------------|------------|----------|------------|------|
| Input range | — | — | AV_{SS3} | — | AV_{DD3} | V |
| Hysteresis voltage | — | V_{REF} reference | — | ± 50 | — | mV |

6. RFZI Signal Comparator

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--------------------|--------------|---------------------|------------|----------|------------|------|
| Input range | — | — | AV_{SS3} | — | AV_{DD3} | V |
| Hysteresis voltage | — | V_{REF} reference | — | ± 50 | — | mV |

7. Data Slicer Circuit

(1) Comparator

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-----------------|--------------|----------------------------|-----|------|-----|-----------------|
| Input amplitude | — | V _{REF} reference | 0.6 | 1.2 | 2.0 | V _{pp} |

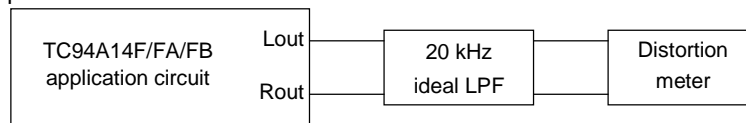
(2) R-2R DAC (digital slicer DAC)

| Characteristics | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-------------------------|--------------|----------------|-------------------|------|-------------------|------|
| Output conversion range | — | — | AV _{SS3} | — | AV _{DD3} | V |
| Output impedance | — | — | — | 2.5 | — | kΩ |

8. Audio DAC Characteristics

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|-----------------------------------|-------------|--------------|---|-----|------|-----|-------|
| Total harmonic distortion + noise | THD + N (1) | 1 | 1 kHz sine wave, full-scale input | — | -88 | -80 | dB |
| | THD + N (2) | | 10 kHz sine wave, full-scale input | — | -80 | -75 | |
| S/N ratio | S/N (1) | 1 | Internal Zero detect = OFF | 87 | 92 | — | dB |
| | S/N (2) | | Internal Zero detect = ON | 95 | 100 | — | |
| Dynamic range | DR | 1 | 1 kHz sine wave, -60dB input conversion | 85 | 90 | — | dB |
| Cross talk | CT | 1 | 1 kHz sine wave, full-scale input | — | -90 | -85 | dB |
| Analog output amplitude | DAC out | 1 | 1 kHz sine wave, full-scale input | 790 | 820 | 850 | mVrms |

Test Circuit 1: Application circuit is used.

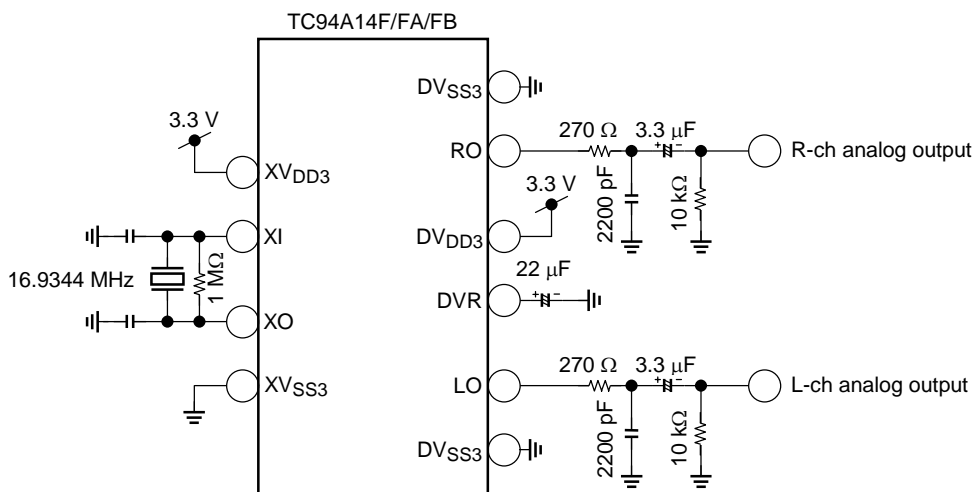


LPF: Filter with built-in Shibasoku 725D
Distortion meter: Shibasoku 725D equivalent

| Characteristic | Distortion Filter Setting A-weight |
|----------------|------------------------------------|
| THD + N, CT | OFF |
| S/N, DR | ON |

A-weight: IEC-A equivalent

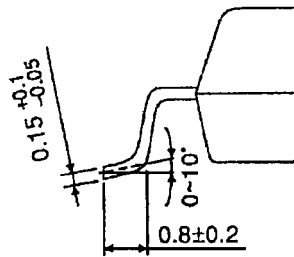
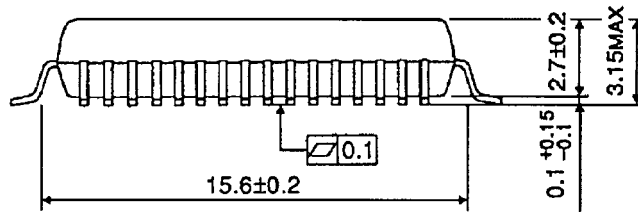
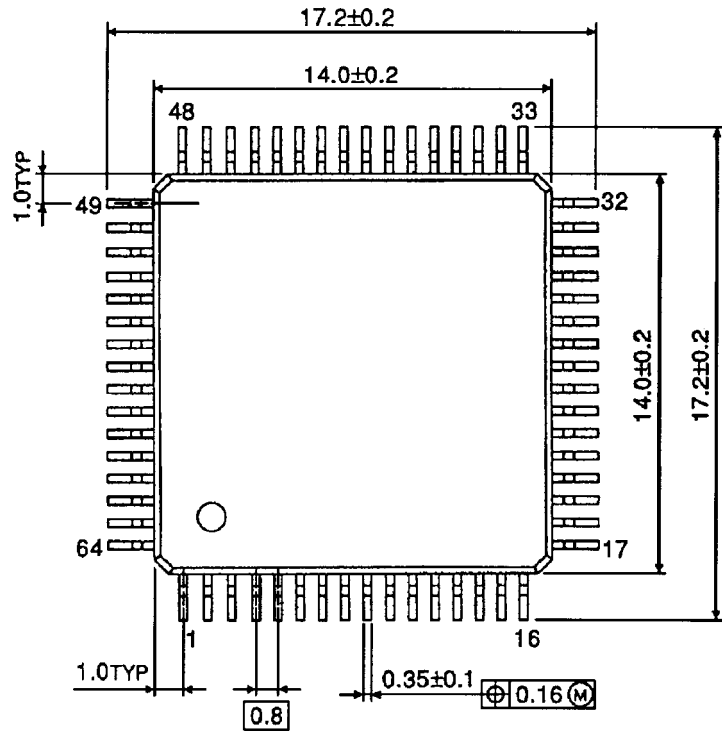
Application Circuit



Package Dimensions

QFP64-P-1414-0.80A

Unit : mm

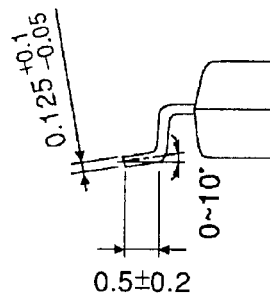
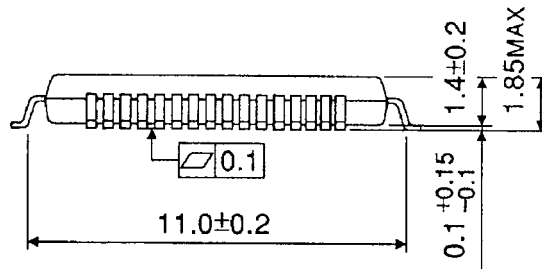
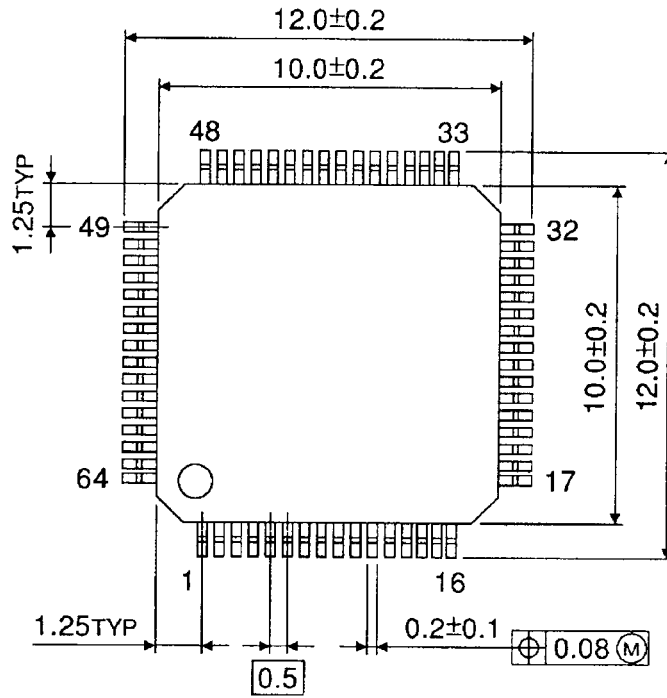


Weight: 0.5 g (typ.)

Package Dimensions

LQFP64-P-1010-0.50

Unit : mm

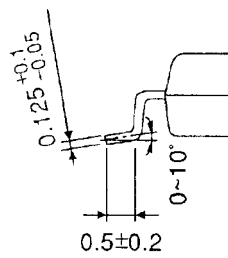
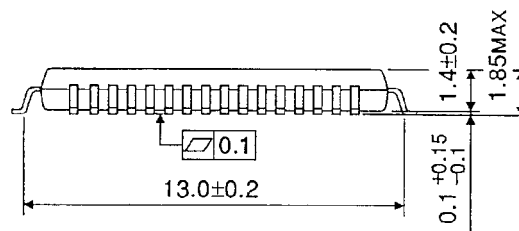
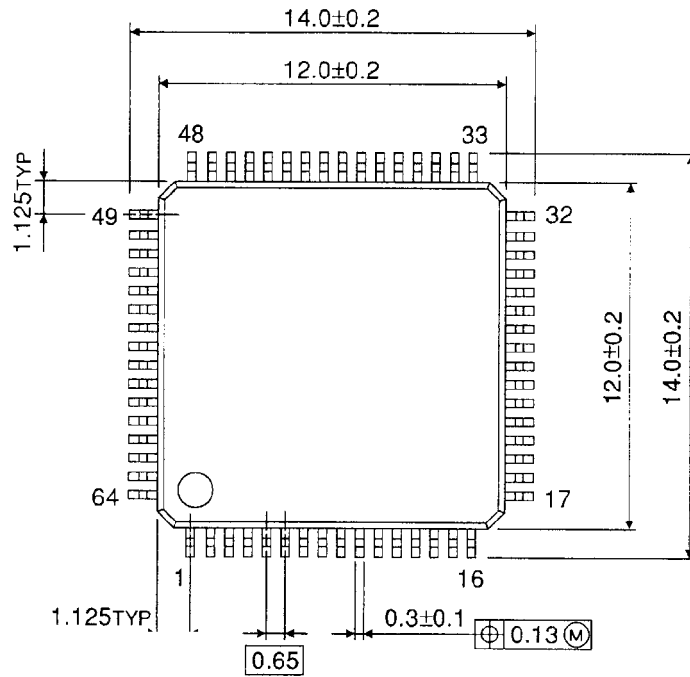


Weight: 0.4 g (typ.)

Package Dimensions

QFP64-P-1212-0.65

Unit : mm



Weight: 0.45 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.