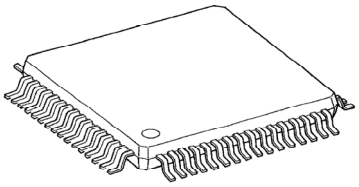
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC94A48FG

Single-chip Audio Digital Signal Processor

The TC94A48FG is a single-chip audio Digital Signal Processor, incorporating two channels A D converter and six channels DA converter.
It can realize many applications, including sound field control, such as hall simulation, digital filters, such as equalizers, surround sound, base boost and more.



P-LQFP64-1010-0.50E

Weight: 0.4 g (typ.)

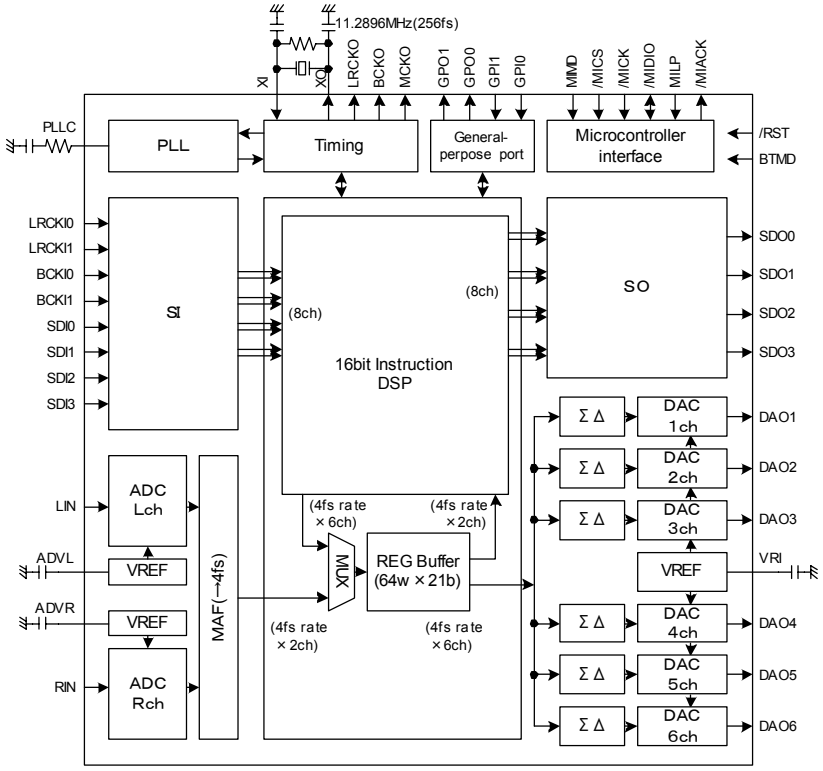
Features

- Incorporates a 1-bit Σ-Δ AD converter (2 channels).
  THD+N: -78 dB (typ.), S/N ratio: 92 dB (typ.)
- Incorporates a multi-bit Σ-Δ DA converter (6 channels).
  THD+N: -88 dB (typ.), S/N ratio: 98 dB (typ.)
- Digital input/output ports
  Four input ports (8 channels)
  Four output ports (8 channels)
- The DSP block specifications are as follows:

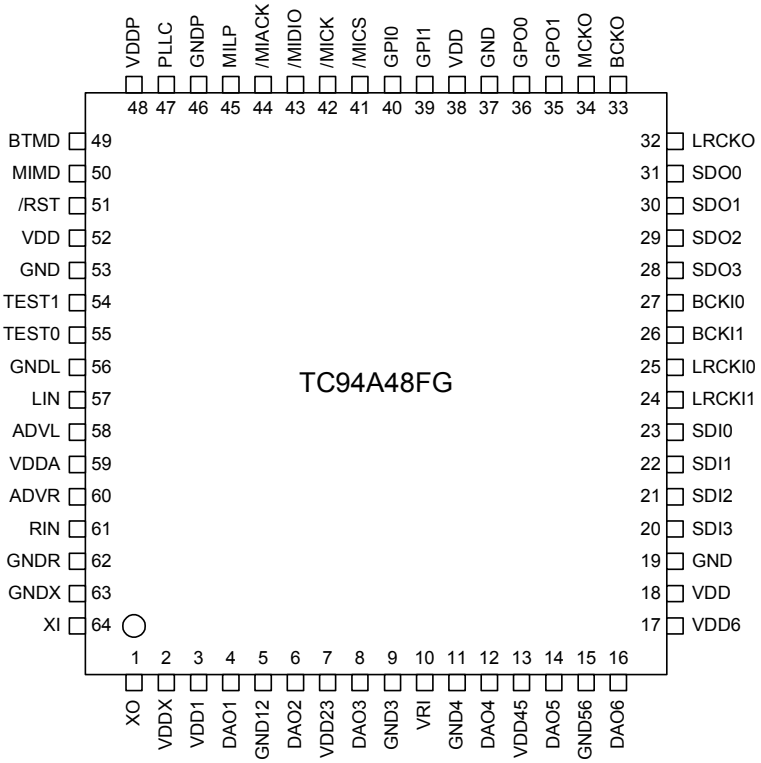
Data bus	: 24 bits
Multiplier/adder	: 24 bits × 24 bits + 51 bits → 51 bits
Accumulator	: 51 bits (sign extension: 4 bits)
Program ROM	: 3072 words × 16 bits
Program RAM	: 1024 words × 16 bits
XRAM	: 4096 words × 24 bits
YRAM	: 1024 words × 24 bits
CROM	: 1024 words × 24 bits

- The microcontroller interface can be selected between serial mode and I^2C bus mode.
- Operating supply voltage: 3.3 V (some pins accept 5 V)
- CMOS silicon structure supports high speed.
- The package is a 64-pin LQFP (0.5-mm pitch) package.

Block Diagram



Pin Layout



Pin Function

Pin No.	Symbol I/O		Function	Remarks
1	XO	O	Crystal oscillator connecting or clock output pin	
2	V_{DDX}	—	Power pin for oscillator circuit	
3	V_{DD1}	—	Analog power pin for DAC1	
4	DAO1	O	DAC1 signal output pin	
5	GND12	—	Analog ground pin for DAC1/2	
6	DAO2	O	DAC2 signal output pin	
7	V_{DD23}	—	Analog power pin for DAC2/3	
8	DAO3	O	DAC3 signal output pin	
9	GND3	—	Analog power pin for DAC3	
10	VRI	I	Reference voltage pin for DAC	
11	GND4	—	Analog ground pin for DAC4	
12	DAO4	O	DAC4 signal output pin	
13	V_{DD45}	—	Analog power pin for DAC4/5	
14	DAO5	O	DAC5 signal output pin	
15	GND56	—	Analog ground pin for DAC5/6	
16	DAO6	O	DAC6 signal output pin	
17	V_{DD6}	—	Analog power pin for DAC6	
18	V_{DD}	—	Digital power pin	
19	GND	—	Digital ground pin	
20	SDI3	I	Audio serial data input pin 3 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
21	SDI2	I	Audio serial data input pin 2 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
22	SDI1	I	Audio serial data input pin 1 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
23	SDI0	I	Audio serial data input pin 0 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
24	LRCKI1	I	LR clock input pin 1 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
25	LRCKI0	I	LR clock input pin 0 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
26	BCKI1	I	Bit clock input pin 1 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
27	BCKI0	I	Bit clock input pin 0 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
28	SDO3	O	Audio serial data output pin 3 It leaves to open when if it is unused.	Push-pull output
29	SDO2	O	Audio serial data output pin 2 It leaves to open when if it is unused.	Push-pull output
30	SDO1	O	Audio serial data output pin 1 It leaves to open when if it is unused.	Push-pull output
31	SDO0	O	Audio serial data output pin 0 It leaves to open when if it is unused.	Push-pull output
32	LRCKO	O	LR clock output pin It leaves to open when if it is unused.	Push-pull output
33	BCKO	O	Bit clock output pin It leaves to open when if it is unused.	Push-pull output

Pin No.	Symbol	I/O	Function	Remarks
34	MCKO	O	System clock output pin It leaves to open when if it is unused.	Push-pull output
35	GPO1	O	General-purpose output pin 1 It leaves to open when if it is unused.	Open-drain output 5V tolerant
36	GPO0	O	General-purpose output pin 0 It leaves to open when if it is unused.	Open-drain output 5V tolerant
37	GND	—	Digital ground pin	
38	VDD	—	Digital power pin	
39	GPI1	I	General-purpose input pin 1 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
40	GPI0	I	General-purpose input pin 0 It connects to GND or V_{DD} pins when if it is unused this pin.	Schmitt input 5V tolerant
41	/MICS	I	Microcontroller interface: Chip select signal input pin	Schmitt input 5V tolerant
42	/MICK	I	Microcontroller interface: Clock input pin	Schmitt input 5V tolerant
43	/MIDIO	I/O	Microcontroller interface: Data input/output pin	Schmitt input / Open-drain output, 5V tolerant
44	/MIACK	O	Microcontroller interface: Acknowledge signal output pin	Open-drain output 5V tolerant
45	MILP	I	Microcontroller interface: Latch pulse input pin	Schmitt input 5V tolerant
46	GNDP	—	Ground pin for PLL	
47	PLLC	I	Charge pump for PLL	
48	VDDP	—	Power pin for PLL	
49	BTMD	I	Boot mode setting pin It is set to "L" when if software specification does not indicate since there is deference by each program ROMs.	Schmitt input 5V tolerant
50	MIMD	I	Microcontroller interface: Mode select input pin	Schmitt input 5V tolerant
51	/RST	I	Reset input pin	Schmitt input 5V tolerant
52	VDD	—	Digital power pin	
53	GND	—	Digital ground pin	
54	TEST1	I	Test setting pin 1 Usually it connects to GND pins.	Schmitt input 5V intolerant
55	TEST0	I	Test setting pin 0 Usually it connects to GND pins.	Schmitt input 5V intolerant
56	GNDL	—	Ground pin for ADC-Lch	
57	LIN	I	ADC-Lch signal input pin	
58	AVDL	I	Reference voltage pin for ADC-Lch	
59	VDDA	—	Analog power pin for ADC	
60	ADVR	I	Reference voltage pin for ADC-Rch	
61	RIN	I	ADC-Rch signal input pin	
62	GNDR	—	Ground pin for ADC-Rch	
63	GNDX	—	Ground pin for oscillator circuit	
64	XI	I	Crystal oscillator connecting or clock input pin	5V intolerant

Note 1: 5V tolerant pins can have voltage applied even when the power to the device is turned off.

Description of Operation

1. T iming System

The TC94A48FG uses pulses from the XI-XO pins as the reference clock. The system is divided into blocks that use the reference clock directly or by dividing its frequency and blocks that operate on a clock the PLL generates based on the crystal resonation clock. The analog and microcontroller interface blocks operate on the crystal resonation clock while the DSP block operates on the PLL-generated clock.

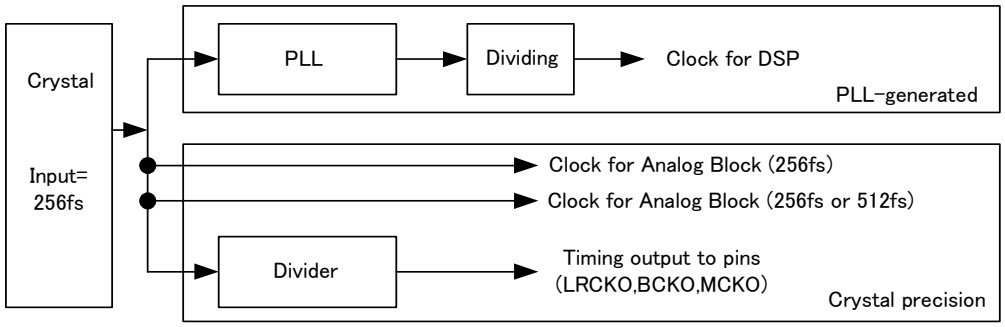


Figure 1 Timing System

The system can divide the clock from the crystal and provide three types of clock from output pins.

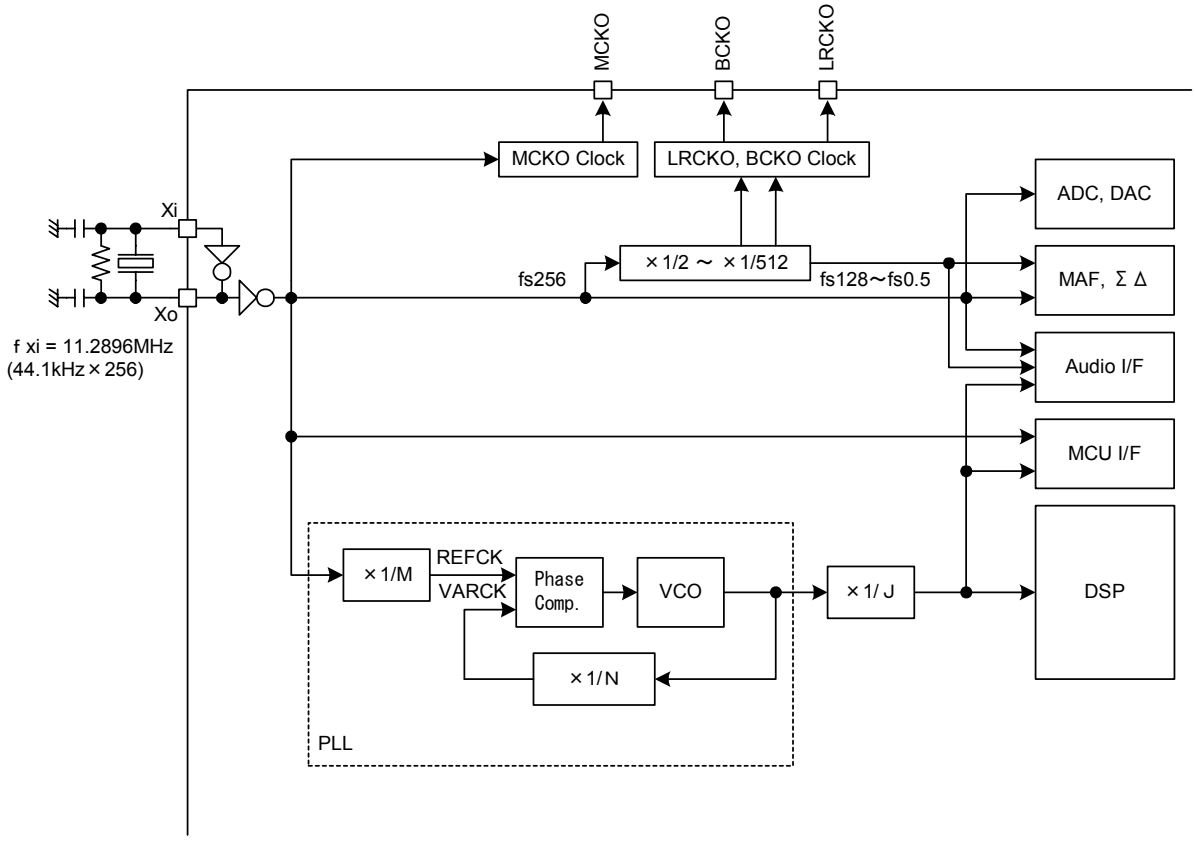


Figure 2 Block diagram of clock generator circuit

1.1 Timing register setting

[AIFA]

Bit	Default	Contents	
15-14	*	BCKi-1 clock frequency	
		00	32fs
		01	48fs
		10	64fs
		11	64fs
13-12	*	BCKi-0 clock frequency	
		00	32fs
		01	48fs
		10	64fs
		11	64fs
11	*	LRCKi-1 polarity	
		0	Lch=Low (interrupt by fall edge)
		1	Lch=High (interrupt by rise edge)
10	*	LRCKi-0 polarity	
		0	Lch=Low (interrupt by fall edge)
		1	Lch=High (interrupt by rise edge)
9	*	SDi clock select	
		0	LRCKi-0/BCKi-0
		1	LRCKi-1/BCKi-1
8	*	SDo clock select	
		0	LRCKi-0/BCKi-0
		1	LRCKi-1/BCKi-1
7-6	*	SDi input format	
		00	LSB justified
		01	MSB justified
		10	I^2S
		11	I^2S
5-4	*	SDi input bit clock	
		00	16bit
		01	18bit
		10	20bit
		11	24bit
3-2	*	SDo output format	
		00	LSB justified
		01	MSB justified
		10	I^2S
		11	I^2S
1-0	*	SDo output bit clock	
		00	16bit
		01	18bit
		10	20bit
		11	24bit

Note 2: In 48fs frequency setup of BCKi-1 and BCKi-0, LRCKi/BCKi coresponds only an input, and LRCKo / BCKo does not correspond.

[MOD_O]

Bit	Default	Contents	
15-12		Reserved	
		Fixed to “0”	
11	*	SDo3 is used as a general-purpose output Po5.	
		0	Disable
		1	Enable
10	*	SDo2 is used as a general-purpose output Po4.	
		0	Disable
		1	Enable
9	*	SDo1 is used as a general-purpose output Po3.	
		0	Disable
		1	Enable
8	*	SDo0 is used as a general-purpose output Po2.	
		0	Disable
		1	Enable
7		Reserved	
		Fixed to “0”	
6		Reserved	
		Fixed to “1”	
5	*	Synchronization of LRCKi and LRCKo	
		0	Disable
		1	Enable
4	*	BCCMP/BCJMP Enable	
		0	Disable
		1	Enable
3	*	DAC Enable	
		0	Disable
		1	Enable
2	*	ADC Enable	
		0	Disable
		1	Enable
1	*	LRCKo is connected to LRCKi1.	
		0	It does not connect.
		1	It connects.
0	*	LRCKo is connected to LRCKi0.	
		0	It does not connect.
		1	It connects.

[TMGA]

Bit	Default	Contents	
15-14		Reserved	
		Fixed to “0”	
13		DSP clock output select	
	*	0	Disable
		1	Enable
12-7		Reserved	
		Fixed to “0”	
6		MCKO clock output select	
	*	0	1/1 Xi clock
		1	1/2 Xi clock
5-3		Reserved	
		Fixed to “0”	
2-0		DSP clock divider setting (1/J)	
		000	1/1
		001	1/2
		010	1/4
		011	1/8
		100	1/16
	*	101	1/3
		110	1/6
		111	Prohibit

[TMGB]

Bit	Default	Contents	
15-14		LRCKo/BCKo clock select	
	*	00	FS1/FS32(BCK=fs32)
		01	FS1/FS64(BCK=fs64)
		10	FS2/FS64(BCK=fs32)
		11	FS2/FS128(BCK=fs64)
13		LRCKo/BCKo output clock select	
	*	0	Disable
		1	Enable
12-8		Reference clock divider setting (1/M)	
		00h	1/1
		01h	1/2
		.	
		.	
	*	09h	1/10
		.	
		1Fh	1/32
7-0		Variable clock divider setting (1/N)	
		00h	1/1
		01h	1/2
		.	
		.	
	*	3Fh	1/64
		.	
		FFh	1/256

1.2 Timing Output

LRCKO / BCKO Pin Output Settings

Mode	LRCKO Pin Output	BCKO Pin Output	Remarks
0	Fixed to GND	Fixed to ground	Initial Value
1 1fs		32fs	
2 1fs		64fs	
3 2fs		64fs	
4 2fs		128fs	

MCKO Pin Output Settings

Mode MCKO	Pin Output	Remarks
0	Fixed to GND	It can be initialized by reset. Undefined until set by microcontroller or built-in DSP program
1	XCKI (=XI)	
2 0.	5 × XCKI	

Note 3: A setup of a timing output is performed by the built-in firmware.

1.3 Example of oscillator circuit

The example of a circuit at the time of the crystal oscillator use in an oscillation part is shown in figure 3.

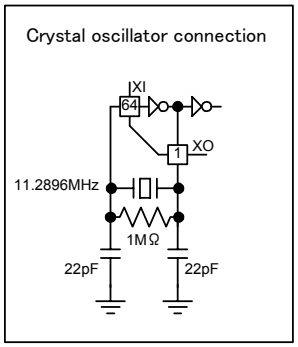


Figure 3 Example of oscillator circuit

1.4 Example of PLL circuit

A PLL circuit can consist of connecting LPF to a PLLC terminal easily. The example of a circuit is shown in figure 4.

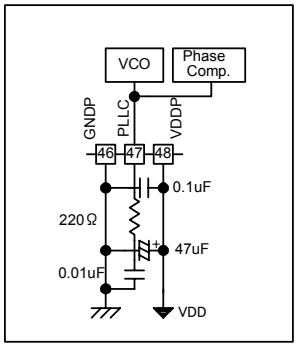


Figure 4 Example of PLL circuit

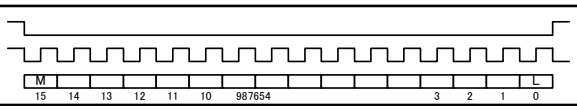
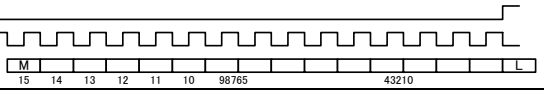
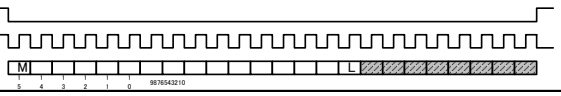
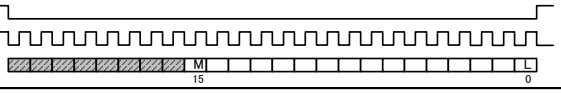
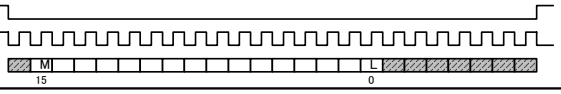
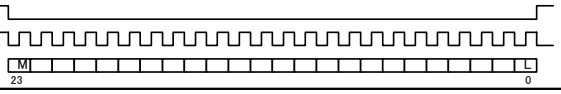
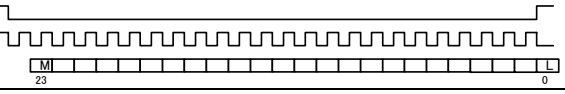
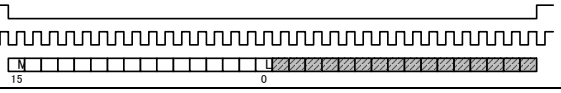
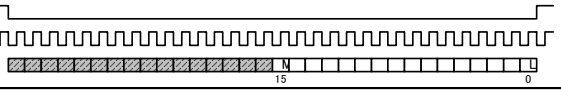
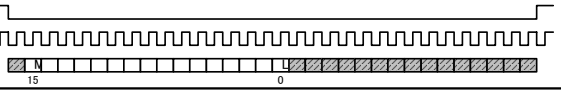
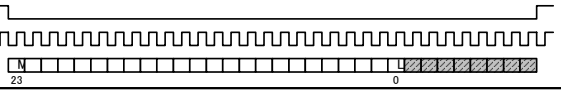
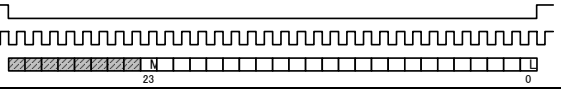
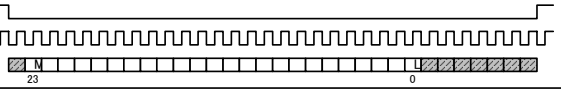
The above-mentioned external constant is a reference value. It may change with application.

1.5 A udio Input/Output Format

1.5.1 Audio Serial Data Input Format

The TC94A48FG supports MSB-first input only. In slave mode, it supports all setting formats for the number of bit clock slots. In master mode, it does not support 24 slots.

M = MSB L = LSB don't care(invalid data, padded with "0" when read by DSP internal firmware)

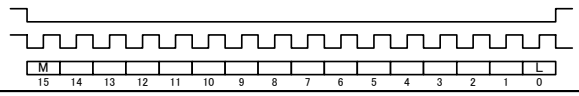
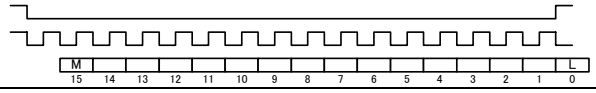
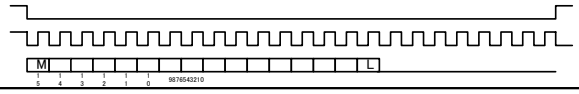
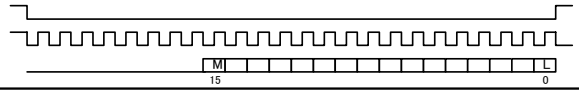
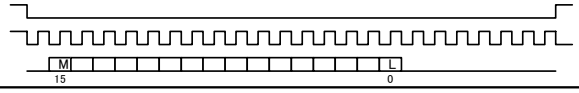
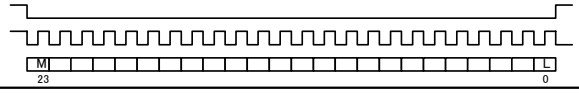
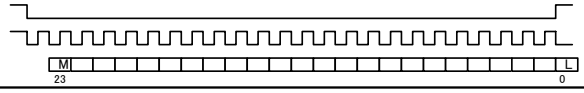
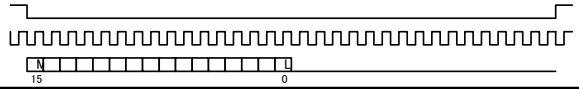
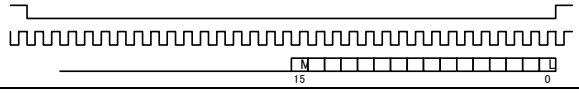
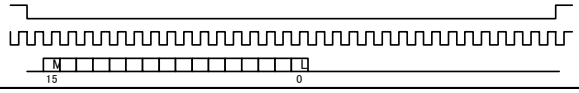
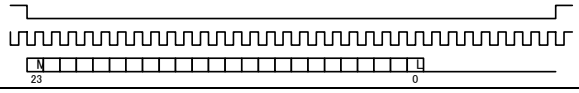
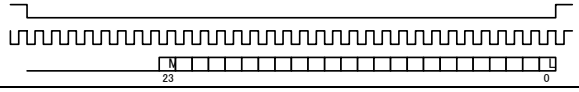
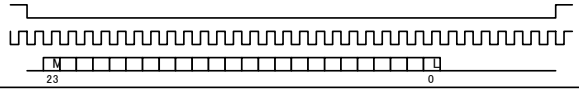
MODE	Number of Slots	Data Word Length (bit)	Format	Timing Chart	Remarks
0	16	16	MSB-justified (LSB-justified)		Initial Value
1			I²S		
2	24	16	MSB-justified		Unavailable in master mode(Note)
3			LSB-justified		
4			I²S		
5		24	MSB-justified (LSB-justified)		
6			I²S		
7	32	16	MSB-justified		
8			LSB-justified		
9			I²S		
10		24	MSB-justified		
11			LSB-justified		
12			I²S		

Note 4: These formats cannot be used in master mode (when LRCK and BCK are supplied to external devices).

1.5.2 Audio Serial Data Output Format

The valid part of data is the same as that for the input format. The TC94A48FG supports MSB-first output only. In slave mode, it supports all setting formats for the number of bit clock slots. In master mode, it does not support 24 slots.

M =MSB L =LSB ____ =fixed to "0" (data sent from DSP is ignored)

MODE	Number of SLOT	Data Word Length (bits)	Format	Timing Chart	Remarks
0	16	16			Initial value
1			I^2S		
2	24	16			Unavailable in master mode(Note)
3					
4			I^2S		
5		24			
6			I^2S		
7	32	16			
8					
9			I^2S		
10		24			
11					
12			I^2S		

Note 5: These formats cannot be used in master mode (when LRCK and BCK are supplied to external devices).

The audio input block and output block support different clock settings. Input and output port settings are, however, shared as follows:

LR Clock Setting for Input Block

Mode S	ignal
Master Mode	Signal delivered to LRCKO pin (crystal resonation clock divided)
Slave Mode	LRCKI0 pin input
	LRCKI1 pin input

Bit Clock Setting for Input Block

Mode S	ignal
Master Mode	Signal delivered to BCKO pin (crystal resonation clock divided)
Slave Mode	BCKI0 pin input
	BCKI1 pin input

LR Clock Setting for Output Block

Mode S	ignal
Master Mode	Signal delivered to LRCKO pin (crystal resonation clock divided)
Slave Mode	LRCKI0 pin input
	LRCKI1 pin input

Bit Clock Setting for Input Block

Mode S	ignal
Master Mode	Signal delivered to BCKO pin (crystal resonation clock divided)
Slave Mode	BCKI0 pin input
	BCKI1 pin input

2. Microcontroller Interface

The TC94A48FG can exchange data with a microcontroller in either normal transmission mode or I²C mode. It uses the MIMD pin to select the mode and inputs/outputs data in MSB-first format.
Table 1 shows the features supported and the pins used in each mode.
Table 2 shows the bit composition of a 24-bit command.

Note 6: This data sheet shows general control methods. Refer to the separate program explanation data sheet for a complete command list or detailed description of control methods.

Table 1 Pins Used and Features Supported in Normal Transmission Mode and I^2C Mode

Transmission Mode		Normal Transmission Mode (MIMD=L)	I^2C Mode (MIMD=H)
Pin I	nput/Output	Function	Function
/MICS	Input	Chip select Input	Not used (fixed to "L")
MILP	Input	Latch pulse input	Not used (fixed to "L")
/MIDIO	Input Output (open-drain)	Data input / output	Data input / output (SDA)
/MICK	Input, Input / Output (I^2C mode)	Clock input	Clock input (SCL)
/MIACK	Output (open-drain)	Acknowledge output	Not used

Note 7: The input High voltage for these pins should be V_{DD}-0.2 V to 5.5V.

Note 8: The open-drain /MIDIO and /MIACK pins require external pull-up resistors.

In I^2C mode, the /MICK pin also requires a pull-up resistor.

The pulled-up voltage for these pins should be V_{DD}-0.2V to 5.5V.

Note9: The I^2C bus write address is 30 h and read address is 31h.

Table 2 Bit Composition of a 24-bit Command

Bit F	unction	Remarks
23-8 16	-bit address	Refer to the command list in the program explanation data sheet.
7	Not used	—
6	Start program RAM boot	"1" starts program RAM boot.
5	Specify soft reset	"1" triggers a soft reset.
4	Specify read or write (R/W)	"1" specifies a read.
3-0	Set the number of words to be transmitted	0h" ; 1word ↓ "7h" ; 8words

2.1 Normal Transmission Mode

2.1.1 Data Transfer Format in Normal Transmission Mode

Figure 1 shows the data transfer format in normal transmission mode.
In normal transmission mode, the system first drives /MICS low and then checks that /MIACK is low before transferring a 24-bit command MSB first. It cannot transfer data if /MIACK is high.
The system then reads or writes as many 24-bit data words (one to eight) as specified with the 24-bit command and finally drives /MICS high. For a read, it should also make sure that /MIACK is low after transferring a 24-bit command because /MIACK becomes high temporarily after the command is transferred.

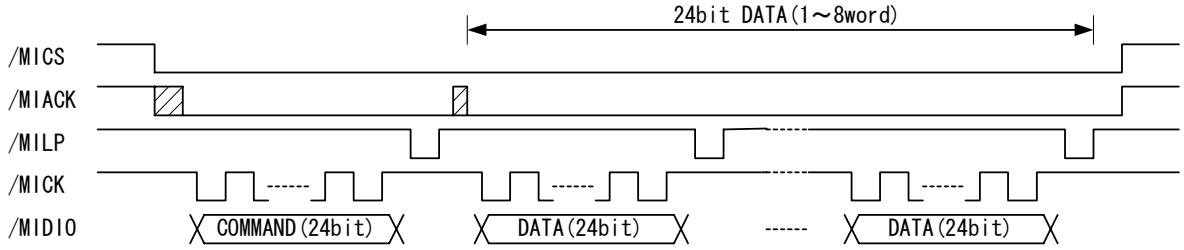


Figure 5(a) Data Transfer Format in Normal Transmission Mode

2.1.2 Data Transfer Method in Normal Transmission Mode

(1) Program boot and program start

The TC94A48FG has 1k-word RAM assigned to program addresses 000h to 3FFh, in which 000h to 003h are interrupt vector addresses. To enable the TC94A48FG to operate, a program must be booted to an interrupt vector address. If you want to store a program in the area from 004h to 3FFh, a program loading process must follow the interrupt vector address. For a program boot, the 24-bit command transferred upon a reset must have the program RAM boot start bit and soft reset bit set to "1" (command = xxxx60h).
The command must be followed by 16-bit program data, set in lower bits in 24-bit data.
The write address is automatically incremented (by one) from the command (000h). The program boot completes once /MICS is driven high upon transferring the required number of words.
The write address for a program boot always starts from the command (000h). To start the program, transfer a 24-bit command with the soft reset bit cleared and then drive /MICS high without transferring data.
Figure 6 shows the program boot and program start procedure.

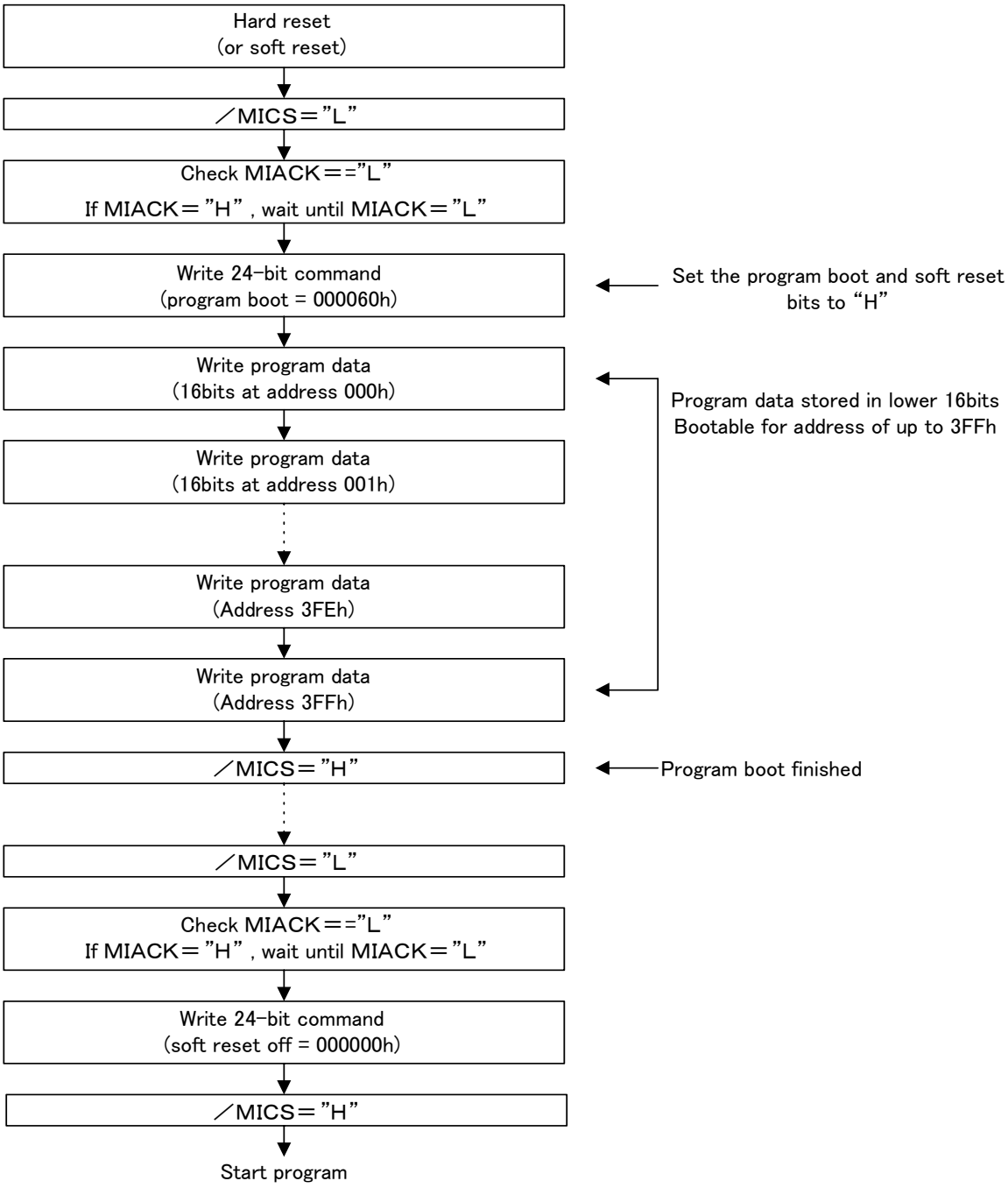


Figure 6 Pr ogram Boot and Program Start Procedure

(2) W riting 24-bit data

When the host microcontroller writes data to the TC94A48FG during the execution of a program, it sets a 16-bit address in a 24-bit command as well as sets its R/W bit to "0" and sets the number of words to be written. Then, it transfers the 24-bit command, followed by a required number of 24-bit data words.
Figure 7 shows the 24 bit data write procedure.

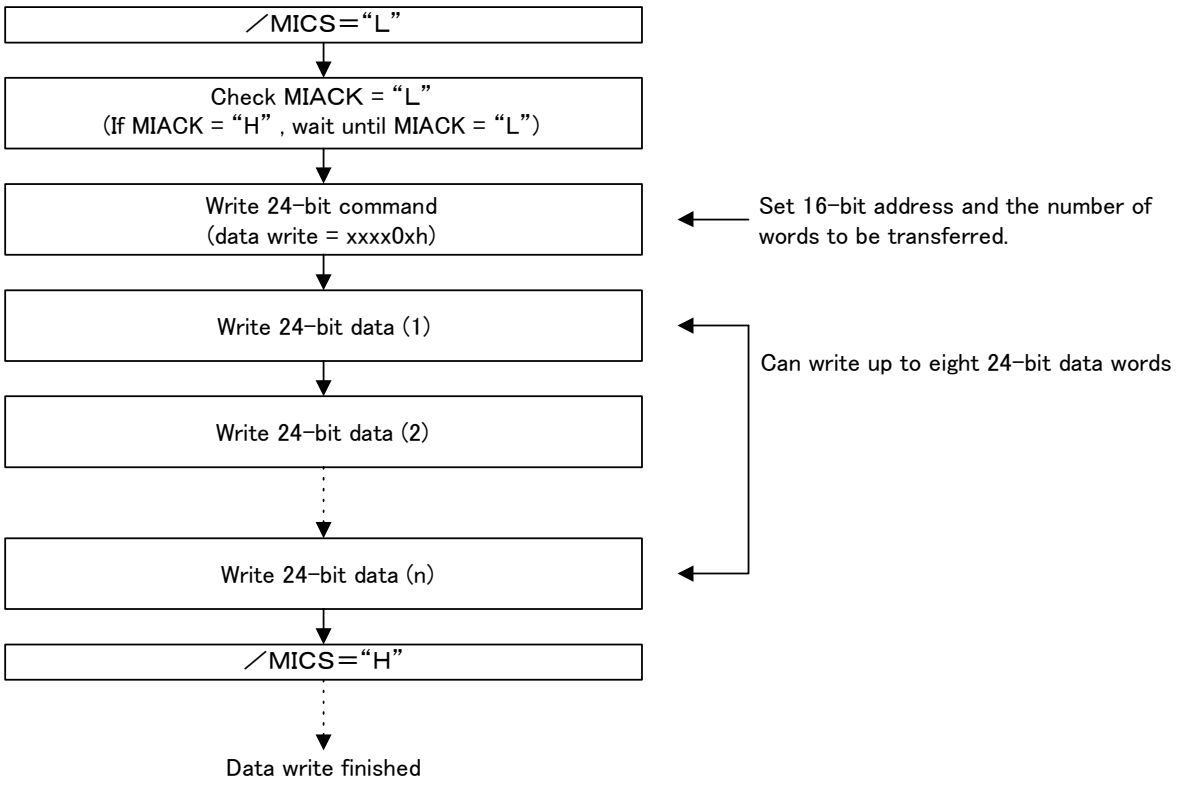


Figure 7 shows the 24-bit data write procedure.

(3) Read ing 24-bit data

When the host microcontroller reads data from the TC94A48FG during the execution of a program, it sets a 16-bit address in a 24-bit command as well as sets its R/W bit to "1" and sets the number of words to be read. Then, it transfers the 24-bit command, check that /MIACK = "L", and read a required number of 24-bit data words.

The host microcontroller should check that /MIACK = "L" because it has to wait until the data to be read is set in the data buffer.

Figure 8 shows the 24 bit data read procedure.

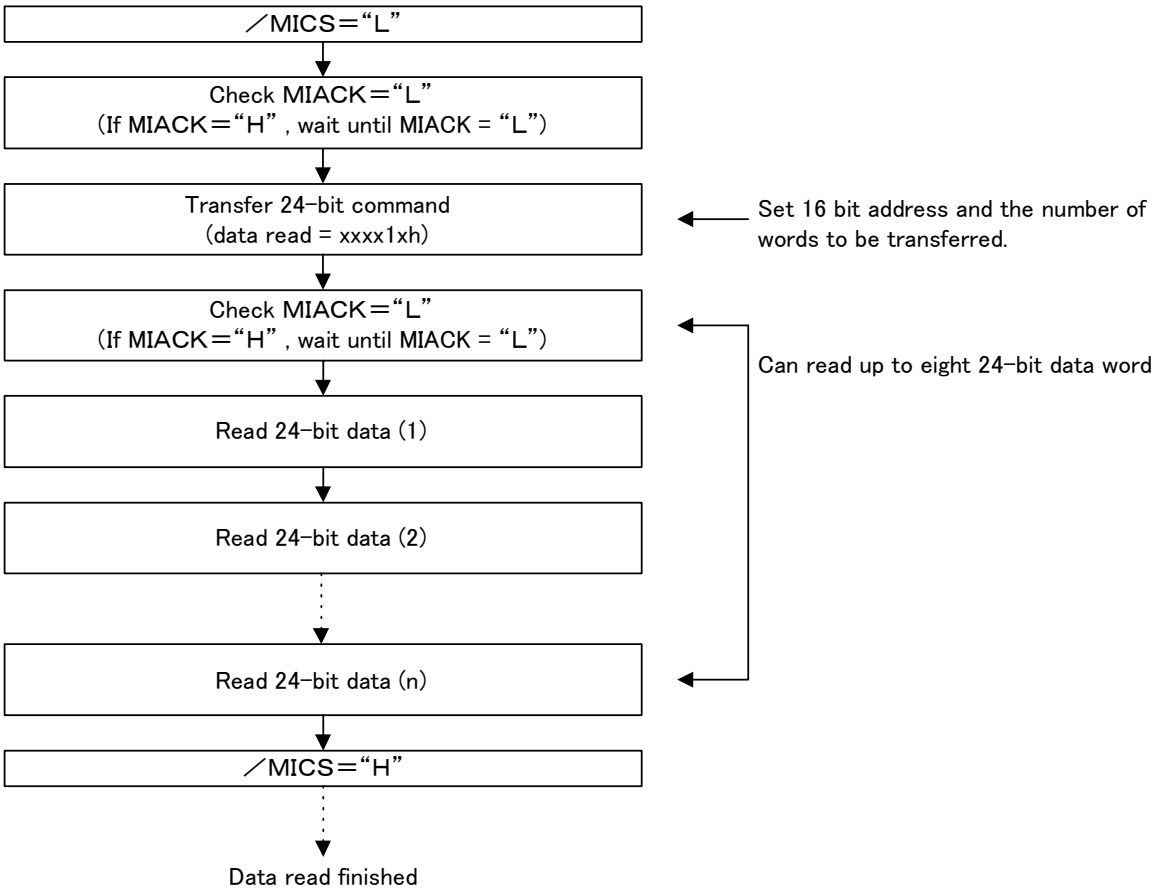


Figure 8 shows the 24-bit data read procedure.

(4) Triggering and terminating a soft reset

A soft reset is required before the system can start a program after program boot or restart a program.

A 24-bit command with its soft reset bit set to "1" triggers a soft reset and a command with the bit cleared terminates a soft reset.

When trigging or terminating a soft reset, drive /MICS high after transferring the 24-bit command because no data needs to follow the command.

Figure 9 shows the procedure for trigging or terminating a soft reset.

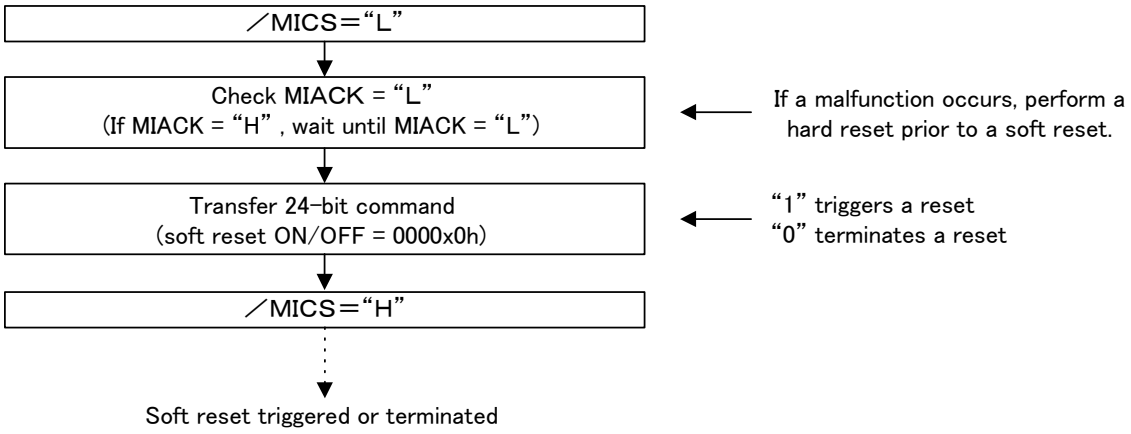


Figure 9 Procedure for Trigging or Terminating a Soft Reset

2.2 I²C Bus Mode

2.2.1 Data Transfer Format in I²C Bus Mode

Figure 10 shows the data transfer format in I²C bus mode.
In I²C bus mode, the host microcontroller first transfers an I²C address (write = 30h) and then checks that the ACK bit is low. If the ACK bit is high, it retransmits a start condition (without transmitting a stop condition) and then transfers an I²C address of 30h. After transferring an I²C address, the host microcontroller transfers a 24-bit command. When the host microcontroller writes data to the TC94A48FG, it writes as many 24-bit data words as specified with the 24-bit command (1 to 8 words) and then transfers an end condition.
When the host microcontroller reads data from the TC94A48FG, it transfers a 24-bit command and then, without transmitting an end condition, transfers an I²C address (read =31h) and check that the ACK bit is low. If the ACK bit is high, the host microcontroller retransmits a start condition (without transmitting a stop condition) and then transfers an I²C address of 31h. After checking that the ACK bit is low, the host microcontroller reads as many 24-bit data words as specified with the 24-bit command (1 to 8 words). During a read, the host microcontroller sets the ACK bit to low after reading every eight bits. The ACK bit accompanying the last eight bits must be set to high, after which the host microcontroller transmits a stop condition. When transferring only a 24-bit command without reading or writing data, transmit an end condition after transferring the command.
Figures 11 to 13 show the data transfer formats for writing, reading, and transferring a command only.

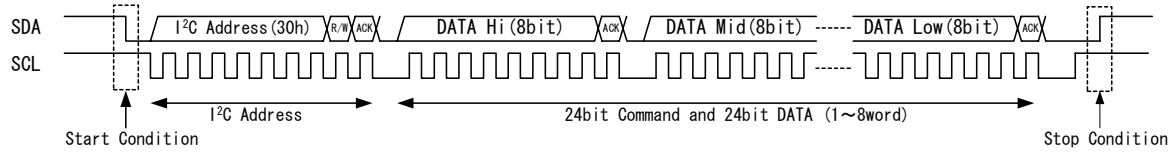


Figure 10 Data Transmission Format in I²C Mode

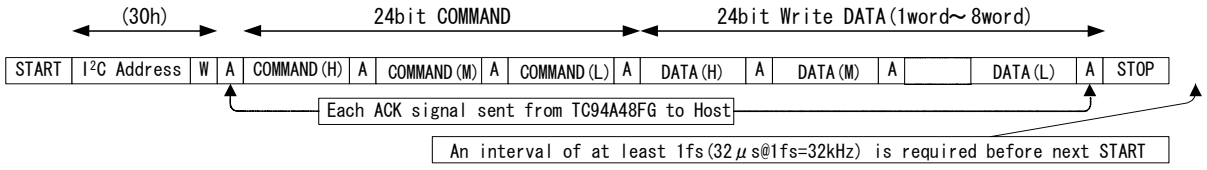


Figure 11 Format for Writing

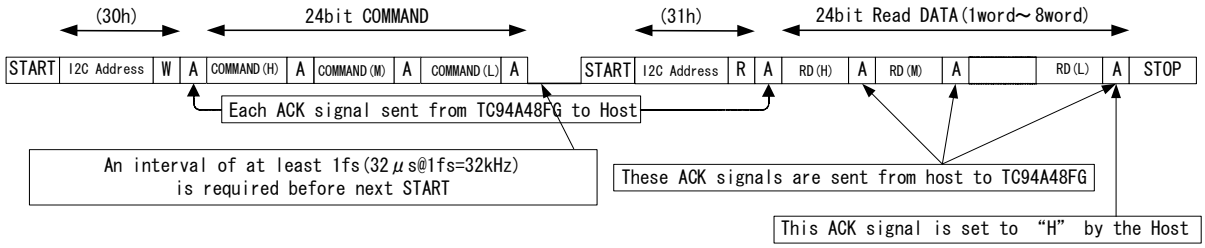


Figure 12 Format for Reading

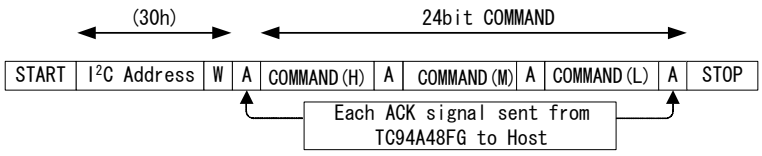


Figure 13 Format for Transferring a Command Only

2.2.2 Data Transfer Method in I^2C Mode

(1) Program boot and program start

The TC94A48FG has 1k-word RAM assigned to program addresses 000h to 3FFh, in which 000h to 003h are interrupt vector addresses. To enable the TC94A48FG to operate, a program must be booted to an interrupt vector address. If you want to store a program in the area from 004h to 3FFh, a program loading process must follow the interrupt vector address. For a program boot, the 24-bit command transferred upon a reset must have the program RAM boot start bit and soft reset bit set to "1" (command = xxxx60h).

The command must be followed by 16-bit program data, set in lower bits in 24-bit data.

The write address is automatically incremented (by one) from the command (000h). The program boot completes once an end condition is transmitted upon transferring the required number of words. The write address for a program boot always starts from the command (000h). To start the program, transfer a 24-bit command with the soft reset bit cleared and then transmit an end condition without transferring data.

Figure 14 shows the program boot and program start procedure.

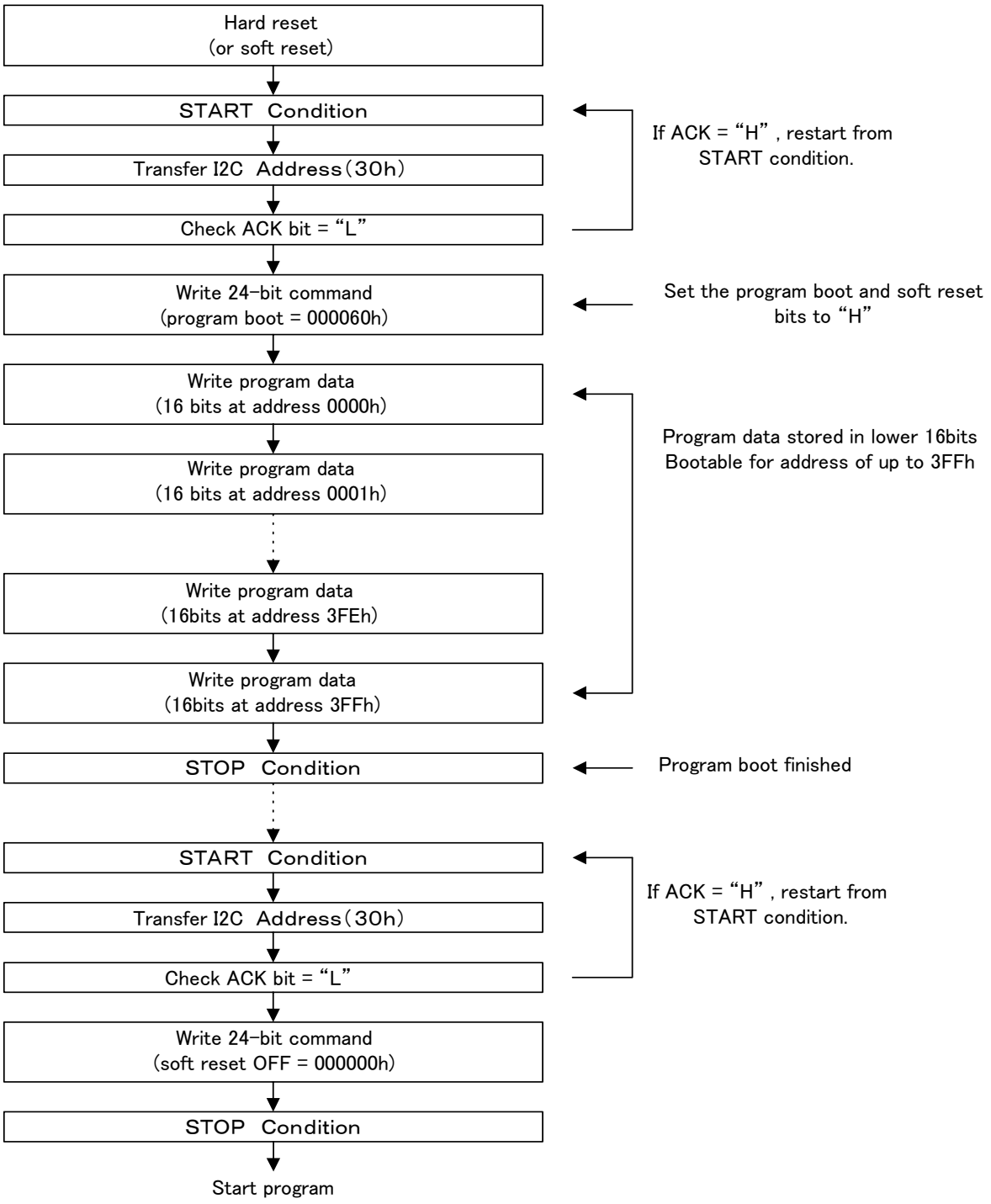


Figure 14 Program Boot and Program Start Procedure

(2) Writing 24-bit data

When the host microcontroller writes data to the TC94A48FG during the execution of a program, it sets a 16-bit address in a 24-bit command as well as sets its R/W bit to "0" and sets the number of words to be written. Then, it transfers the 24-bit command, followed by a required number of 24-bit data words.

An interval of at least 1fs(32 μ s@1fs=32kHz) is required before next started.

Figure 15 shows the 24 bit data write procedure.

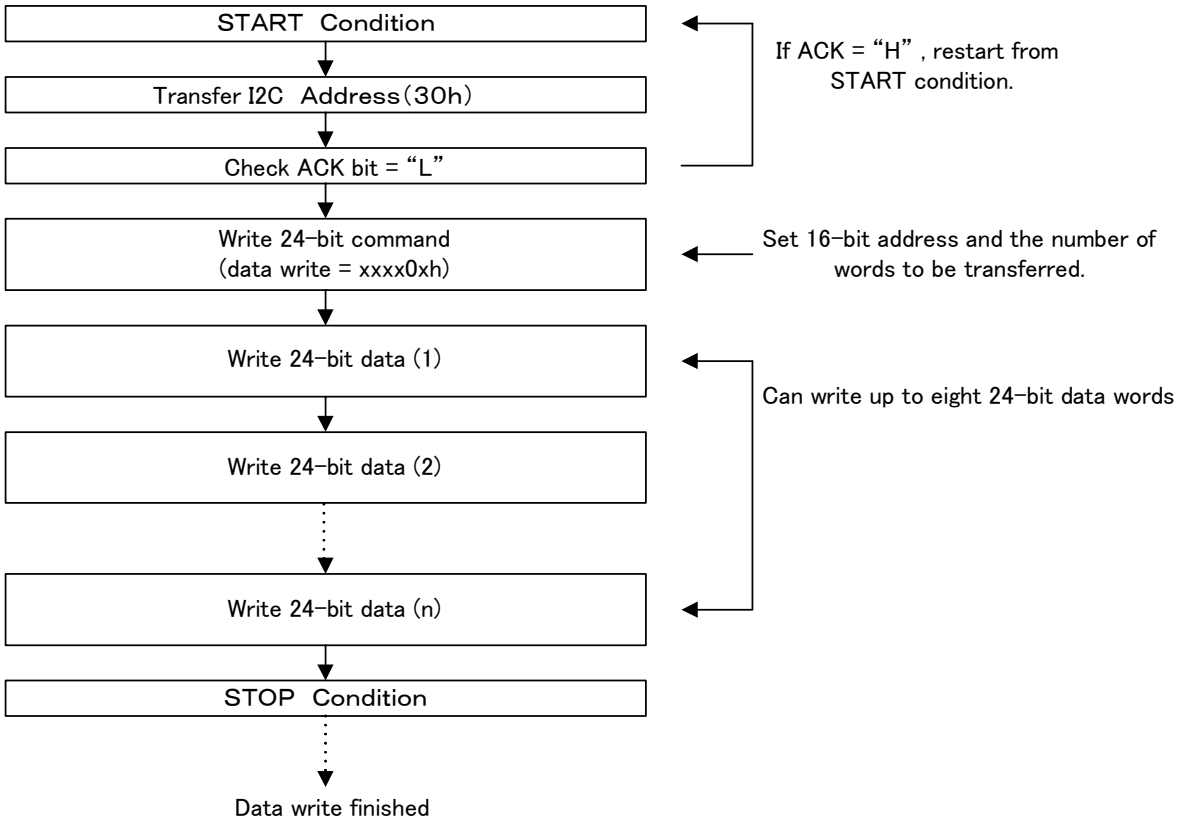


Figure 15 shows the 24-bit Data Write Procedure.

(3) Reading 24-bit data

When the host microcontroller reads data from the TC94A48FG during the execution of a program, it sets a 16-bit address in a 24-bit command as well as sets its R/W bit to "1" and sets the number of words to be read. Then, it transfers the 24-bit command, waits about 1fs, and then transfers an I2C address of 31h, followed by a start condition. Finally, it reads a required number of 24-bit data words. During a read, the host microcontroller should set the ACK bits to low but the ACK bit accompanying the last eight bits of data must be high, thus causing the TC94A48FG to relinquish the SDA bus line so that the host microcontroller can transmit a stop condition.
The host microcontroller should wait about 1fs after transferring a command because it has to wait until the data to be read is set in the data buffer of the TC94A48FG.
Figure 16 shows the 24-bit data read procedure.

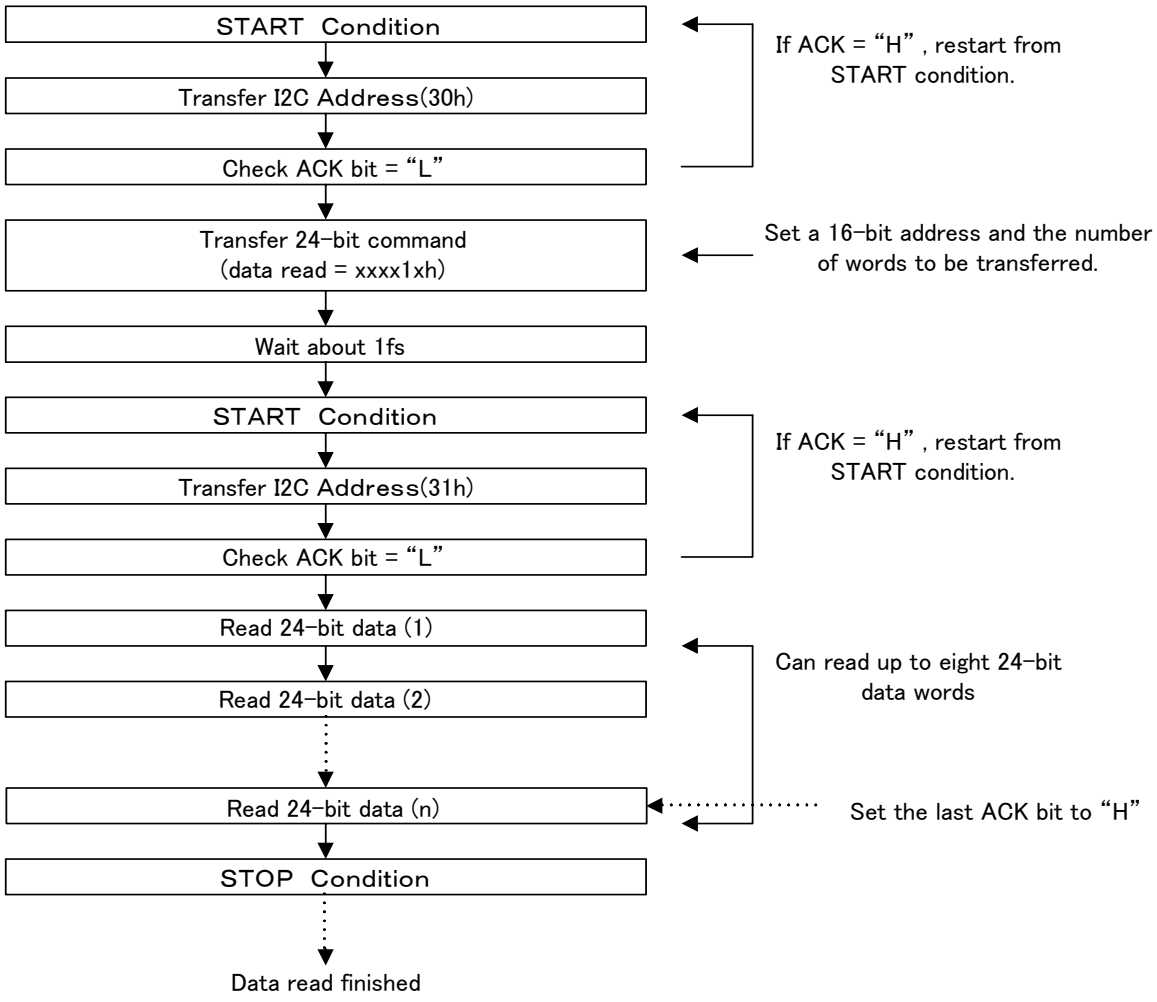


Figure 16 shows the 24-bit Data Read Procedure

(4) Triggering and terminating a soft reset

A soft reset is required before the system can start a program after program boot or restart a program.

A 24-bit command with its soft reset bit set to "1" triggers a soft reset and a command with the bit cleared terminates a soft reset.

When trigging or terminating a soft reset, transmit a stop condition after transferring the 24-bit command because no data needs to follow the command.

Figure 17 shows the procedure for triggering or terminating a soft reset.

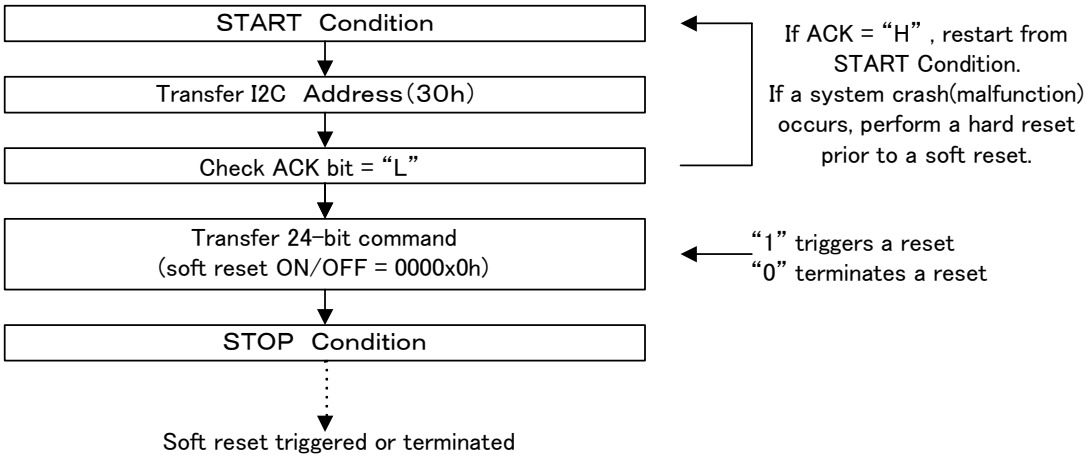


Figure 17 Procedure for Triggering or Terminating a Soft Reset

3. Write and Read Commands

The specifications of write and read commands depend on the built-in program. For details, refer to the program explanation data sheet.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	−0.3~4.0	V
Input voltage 1	V_{in1}	−0.3~V_{DD} + 0.1	V
Input voltage 2 (Note10)	V_{in2}	−0.3~+ 5.5	V
Power dissipation	P_D	400	mW
Operating temperature	T_{opr}	−40~+85	°C
Storage temperature	T_{stg}	−55~+150	°C

Note10: SDI0~3, LRCKI0~1, BCKI0~1, GPI0~1, /MICS, /MICK, /MIDIO, MILP, BTMD, MIMD, /RST

Electrical Characteristics (u nless otherwise specified, Ta = 25°C, V_{DD} = V_{DDX} = V_{DD12} = V_{DD3} = V_{DD45} = V_{DD6} = V_{DDP} = V_{DDA} = 3.3V)

DC Characteristics

Characteristics Sy	mbol	Test circuit	Test Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	—	Ta = −40~85°C	3.0	3.3	3.6	V
Operating frequency range	f_{opr}	—	Using PLL for DSP clock	30	—	75	MHz
PLL clock frequency range	f_{plo}	—		90	—	225	MHz
Operating supply current	I_{DD}	—	fopr =75MHz (75MIPS)	—	90	100	mA

Clock pins (XI,XO)

Characteristics Sy		mbol	Test circuit	Test Condition		Min.	Typ.	Max.	Unit
Input voltage(1)	"H" level	V_{IH1} 2.	— XI	pin		8	—	—	V
	"L" level	V_{IL1}				—	— 0.	5	
Output voltage(1)	"H" level	I_{OH1}	—	V_{OH} = 2.8 V	XO pin	—	—	−2.5	mA
	"L" level	I_{OL1}		V_{OL} = 0.5 V		3.0	—	—	

Input pins

Characteristics Sy		mbol	Test circuit	Test Condition		Min.	Typ.	Max.	Unit
Input voltage(2)	"H" level	V_{IH2}	— (N	ote 11)		2.8	—	—	V
	"L" level	V_{IL2}				—	— 0.	5	
Input leakage current	"H" level	I_{IH2}	—	V_{IN} = V_{DD}	(Note 11),	—	— 10		μA
	"L" level	I_{IL2}		V_{IN} = 0 V	(Note 12)	−10	—	—	

Note 11: SDI0~3, LRCKI0~1, BCKI0~1, GPI0~1, /MICS, /MICK, /MIDIO, MILP, BTMD, MIMD, /RST, TEST0~1, PLLC

Note 12 : XI

Output pins

Characteristics Sy		mbol	Test circuit	Test Condition		Min.	Typ.	Max.	Unit
Output current(2)	"H" level	I_{OH2}	—	V_{OH} = 2.8 V	(Note 13)	—	—	−5	mA
	"L" level	I_{OL2}		V_{OL} = 0.5 V	(Note 13)	5	—	—	
Output current(3)	"H" level	I_{OH3}	—	V_{OH} = 2.8 V	(Note 14)	—	—	−3	
	"L" level	I_{OL3}		V_{OL} = 0.5 V	(Note 14)	3	—	—	
Output current(4)	"L" level	I_{OL4}	—	V_{OL} = 0.5 V	(Note 15)	5	—	—	
Output-off leakage current		I_{OZ5}	—	V_{OH} = V_{DD}	(Note 15)	—	—	±10	μA

Note 13: SDO0~3, LRCKO, BCKO (push-pull output)

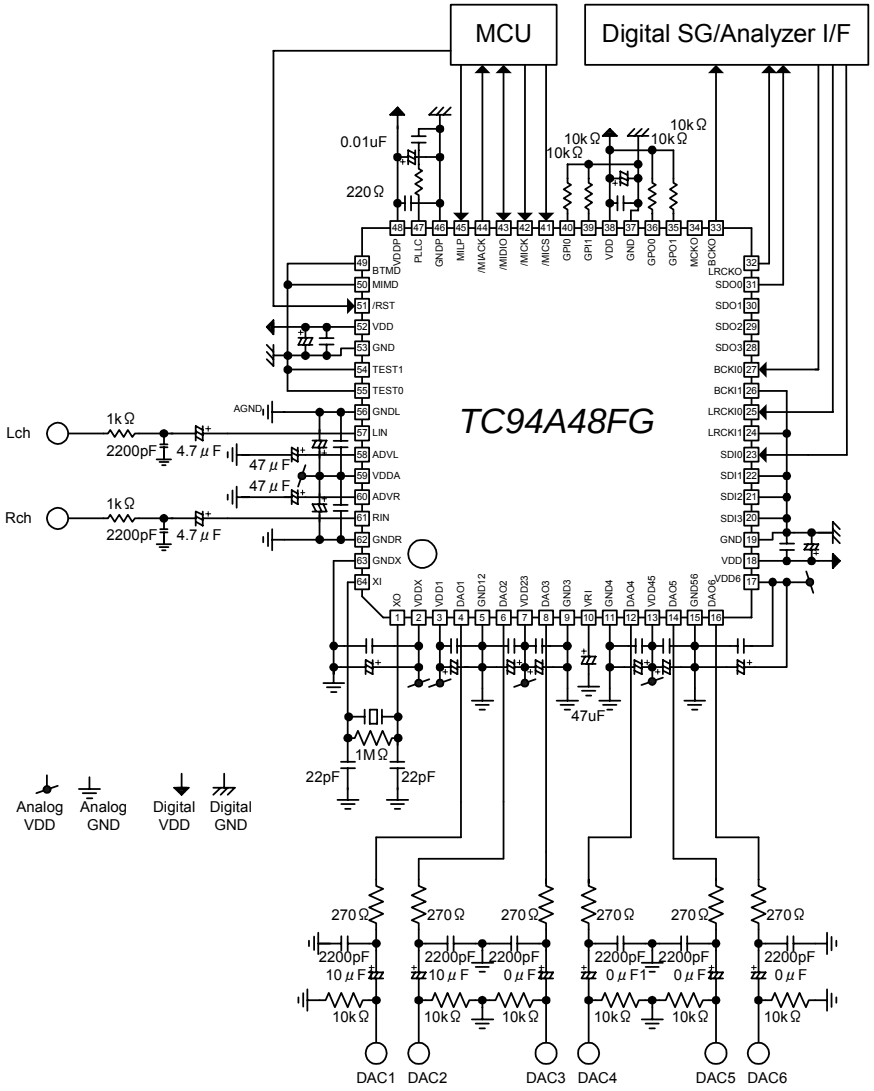
Note 14: MCKO (push-pull output)

Note 15: GPO0~1, /MIDIO, /MIACK (open-drain output)

AC Characteristics

<Common test conditions unless otherwise specified>

- The gain through the firmware is 0 dB (pass-through), except for +2 dB for DC-cut-HPF.
- VDD (for all power supplies) = 3.3V, Ta = 25°C
- Test circuit



AD Conv erter: LIN and RIN pin input, V in_ref: 1 kHz, 800 m Vrms (unless oth erwise specified), SDO0 pin output monitored

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum input signal	Vin	Input level t hat dri ves ADC output to digital full scale.	—	— 800		mVrms
Input impedance	Zin	Each of LIN and RIN pins	20	27	34	kΩ
S/N ratio	S/Na	A-Weight, Input AC shorted, Crystal: 11.2896 MHz	87 93		—	dB
THD + N	THDa	20 kHz LPF, Crystal: 11.2896 MHz	—	−83	−77	
Crosstalk C	Ta	20 kHz LPF, Lch to Rch/ Rch to Lch, Crystal: 11.2896 MHz	—	−85	−78	
Dynamic range	DRa	A-Weight, -60dB for Vin_ref input, Crystal: 11.2896 MHz	87 93		—	
L to R gain error	Vdlr		−0.5	0	0.5	

DA Converter: S DO0 to SDO3 pin inpu t, SDI0_r ef = 0 dBFS, 1 kH z (un less o therwise specified), DAO1 to DAO6 pin output monitored.

Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
Output signal level	Ao	Output voltage at digital full-scale input	790	830	870	mVrms
S/N ratio	S/Nd	A-Weight, Crystal: 11.2896 MHz	90 98		—	dB
THD + N	THDd	20 kHz LPF Crystal: 11.2896 MHz	—	−88	−75	
Crosstalk C	Td	20 kHz LPF, Crystal: 11.2896 MHz	—	−90	−83	
Dynamic range	DRd	A-Weight Crystal: 11.2896 MHz	88 95		—	
Channel-to-channel gain error	Vddo	DAO1~DAO6 pin output monitored.	−0.5 0		0.5	

Timing

Clock input pin (XI)

Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
Clock cycle	t_{XI}	fs=32kHz~48kHz, 256fs input	80.0	88.6	124.0	ns
Clock “H” duration	t_{XIH}	— 4	0.0	44.3	62.0	
Clock “L” duration	t_{XIL}	— 4	0.0	44.3	62.0	

Reset pin (/RST)

Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
Standby time	t_{RRS}	— 10		—	—	ms
Reset pulse width	t_{WRS}	— 1.	0	—	—	μs

Note 16: The /RST pin must be driven low at power-on.

Audio Serial Interface (BCKI0~1, BCKO, LRCKI0~1, LRCKO, SDI0~3, SDO0~3)

Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
LRCKIx setup time	t_{LBS}	CL = 30 pF	75	—	—	ns
LRCKIx hold time	t_{LBH}	fs = 48 kHz or lower BCKI0 and BCKI1 input: 64 fs or lower	–75	—	75	
SDIx setup time	t_{SDI}		50	—	—	
SDIx hold time	t_{HDI} 50			—	—	
BCKIx clock cycle	t_{BCK} 3		00	—	—	
BCKIx clock “H” duration	t_{BCH}		150	—	—	
BCKIx clock “L” duration	t_{BCL}		150	—	—	
SDOx output delay(1)	t_{DO1} C	$_L$ = 30 pF	—	— 60		
SDOx output delay(2)	t_{DO2}	C_L = 30 pF	—	—	60	
LRCKO output delay	t_{DCLR} C	$_L$ = 30 pF	—	— 40		

Microcontroller Interface

Normal Transmission Mode (/MICS, /MICK, /MIDIO, MILP, /MIACK)

Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
Standby time	t_{STB}	— 20		—	— ms	
/MICS fall to /MICK rise setup time	t_1	— 0.	5	—	—	
/MIACK fall to /MICK rise setup time	t_2	— 0.	5	—	—	
/MICK clock cycle	t_3	— 1.	0			
/MICK “L” duration	t_4	— 0.	5	—	—	
/MICK “H” duration	t_5	— 0.	5	—	—	
/MICK rise to /MILP fall setup time	t_6	— 0.	5	—	—	
MILP “L” duration	t_7	— 0.	5	—	—	μs
/MIDIO input data setup time	t_8	— 0.	5	—	—	
/MIDIO input data hold time	t_9	— 0.	5	—	—	
/MIDIO output data delay	t_{10}	—	—	—	0.5	
/MICS “H” duration	t_{11}	—	0.5	—	—	
/MIACK output delay	t_{12}	—	—	—	1.0	
MILP rise to /MICS rise setup time	t_{13}	—	0.5	—	—	

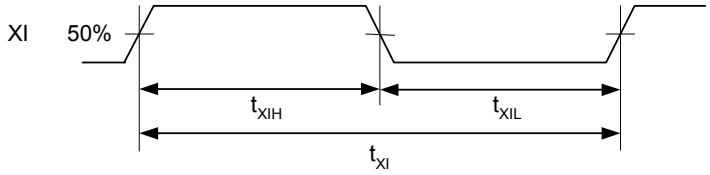
Note 17: The /MIACK output timing and /MIACK "H" duration vary with the firmware.

I^2C Mode (/MICK, /MIDIO)

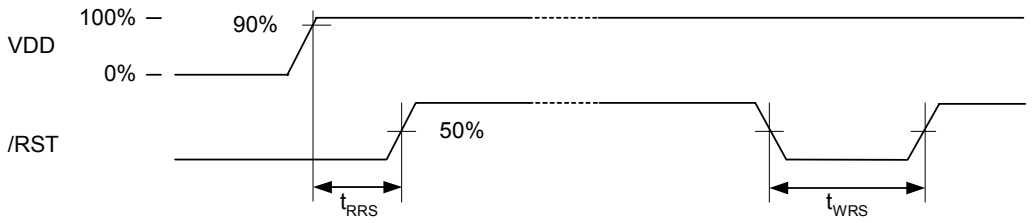
Characteristics Sy	mbol	Test Condition	Min.	Typ.	Max.	Unit
/MICK clock frequency	f_{IFCK}	C_L = 400 pF	0	—	400	kHz
/MICK “H” duration	t_H	C_L = 400 pF	0.6	—	—	
/MICK “L” duration	t_L	C_L = 400 pF	1.3	—	—	
Data setup time	t_{DS}	C_L = 400 pF	0.2	—	—	
Data hold time	t_{DH}	C_L = 400 pF	0	—	0.9	
Transmission start condition hold time	t_{SCH}	C_L = 400 pF	0.6	—	—	
Repeated transmission start condition setup time	t_{SCS}	C_L = 400 pF	0.6	—	—	μs
Transmission end condition setup time	t_{ECS} C	$_L$ = 400 pF	0.6	—	—	
Data transmission interval	t_{BUF}	C_L = 400 pF	1.3	—	—	
I^2C rise time	t_R	C_L = 400 pF	—	—	0.3	
I^2C fall time	t_F	C_L = 400 pF	—	—	0.3	

AC Characteristics Measurement Points

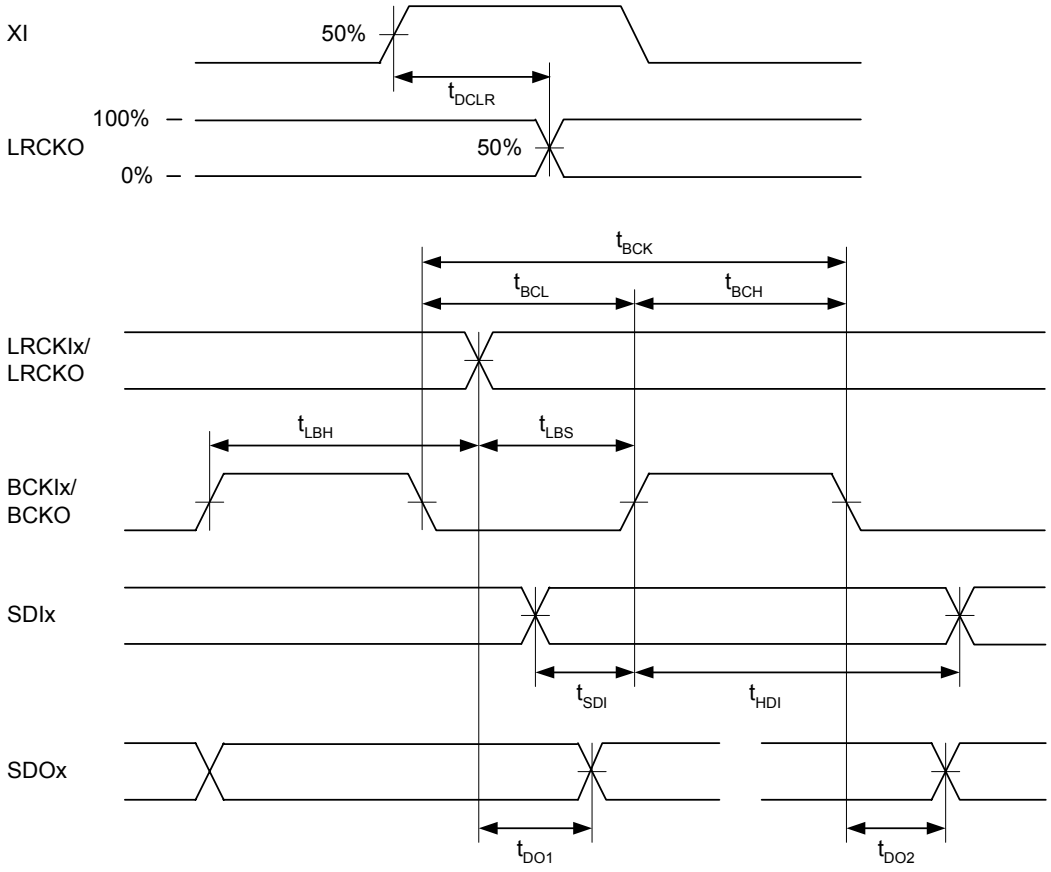
1. Cl ock Pin (XI)



2. Reset Pin (/RST)

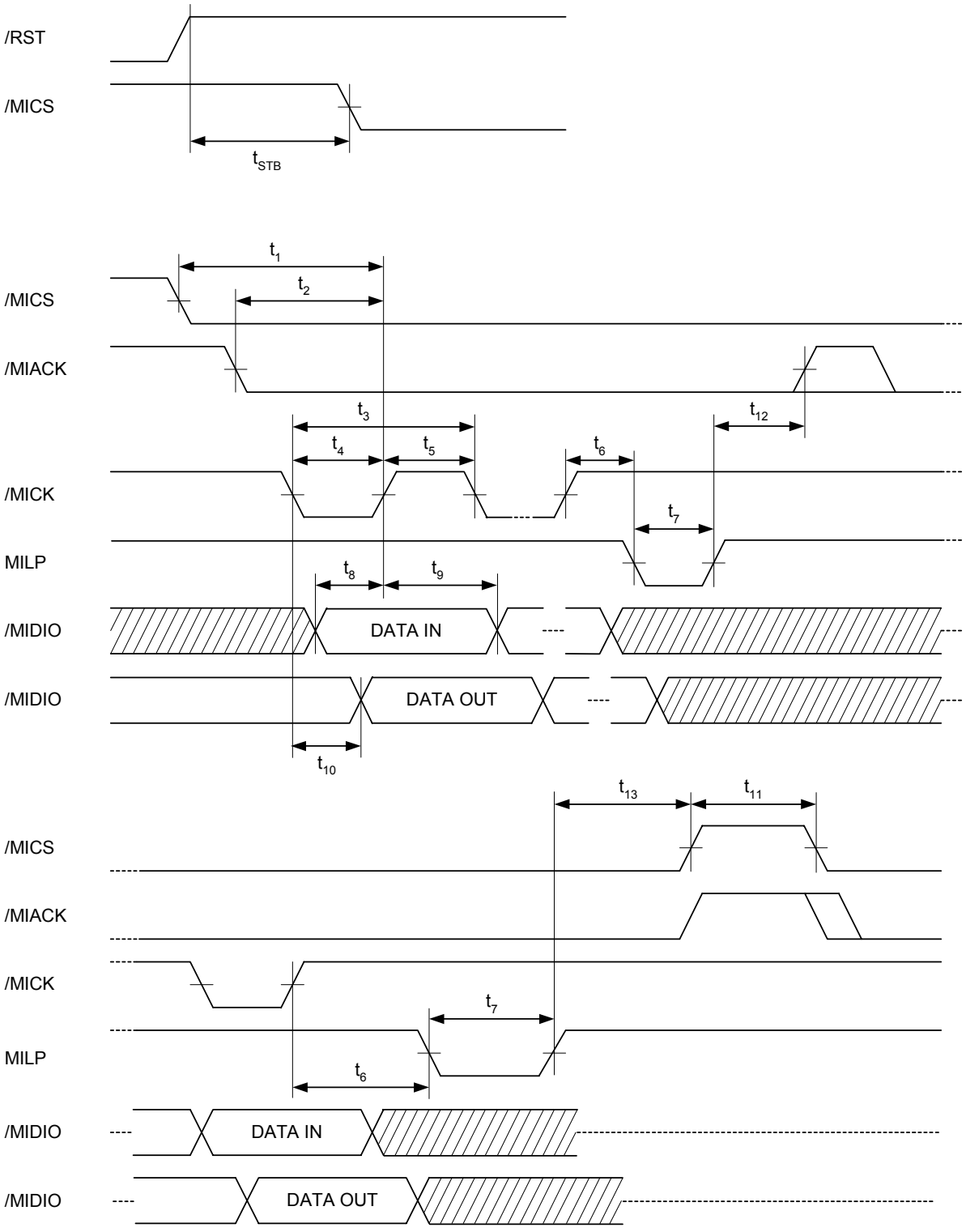


3. Audio Serial Interface (LRCKIx, BCKIx, SDIx, LRCKO, BCKO, SDOx, MCKO)

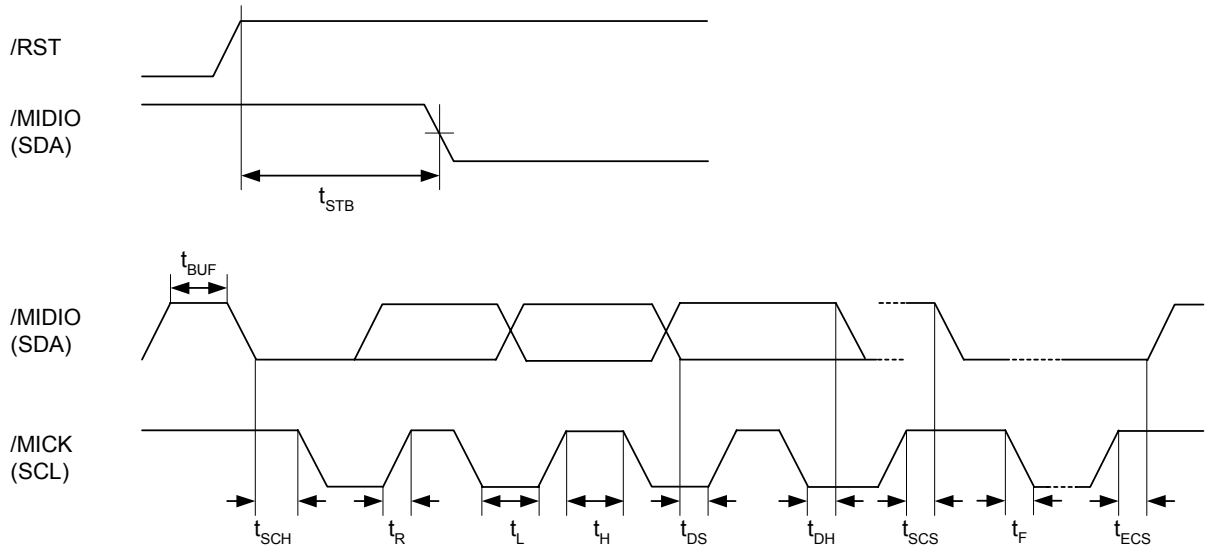


4. Micr ocontroller Interface

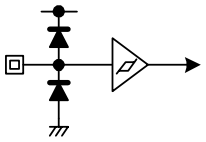
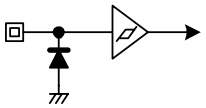
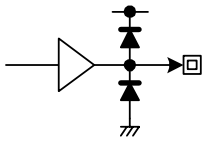
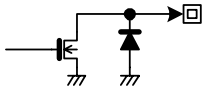
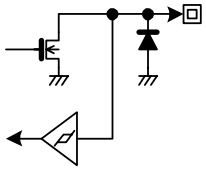
4-1. Serial Mode (/MICS, /MICK, /MIDIO, MILP, /MIACK)



4-2. I^2C Mode (/MICK, /MIDIO)



Equivalent Circuit Diagrams

Type	Equivalent Circuit Diagram	Description
A		Schmitt Input
B		Schmitt Input. 5V tolerant. A voltage can be applied to this pin even when the power supply pin of the TC94A48FG is driven to 0V.
C		Push-pull output. The amplitude is 3.3 V. If external devices require 5V amplitude, perform a level conversion.
D		Open-drain output This pin must be pulled up to VDD or 5V externally.
E		Schmitt input and open-drain output This pin must be pulled up to VDD or 5V externally. A voltage can be applied to this pin even when the power supply pin of the TC94A48FG is driven to 0V. [Caution] When using the pin for input, connect it to an open-drain output pin of an external device.

Type A: TEST0, TEST1

Type B: SDI0~3, LRCKI0~1, BCKI0~1, GPI0~1, BTMD, MILP, /MICK, /MICS, MIMD, /RST

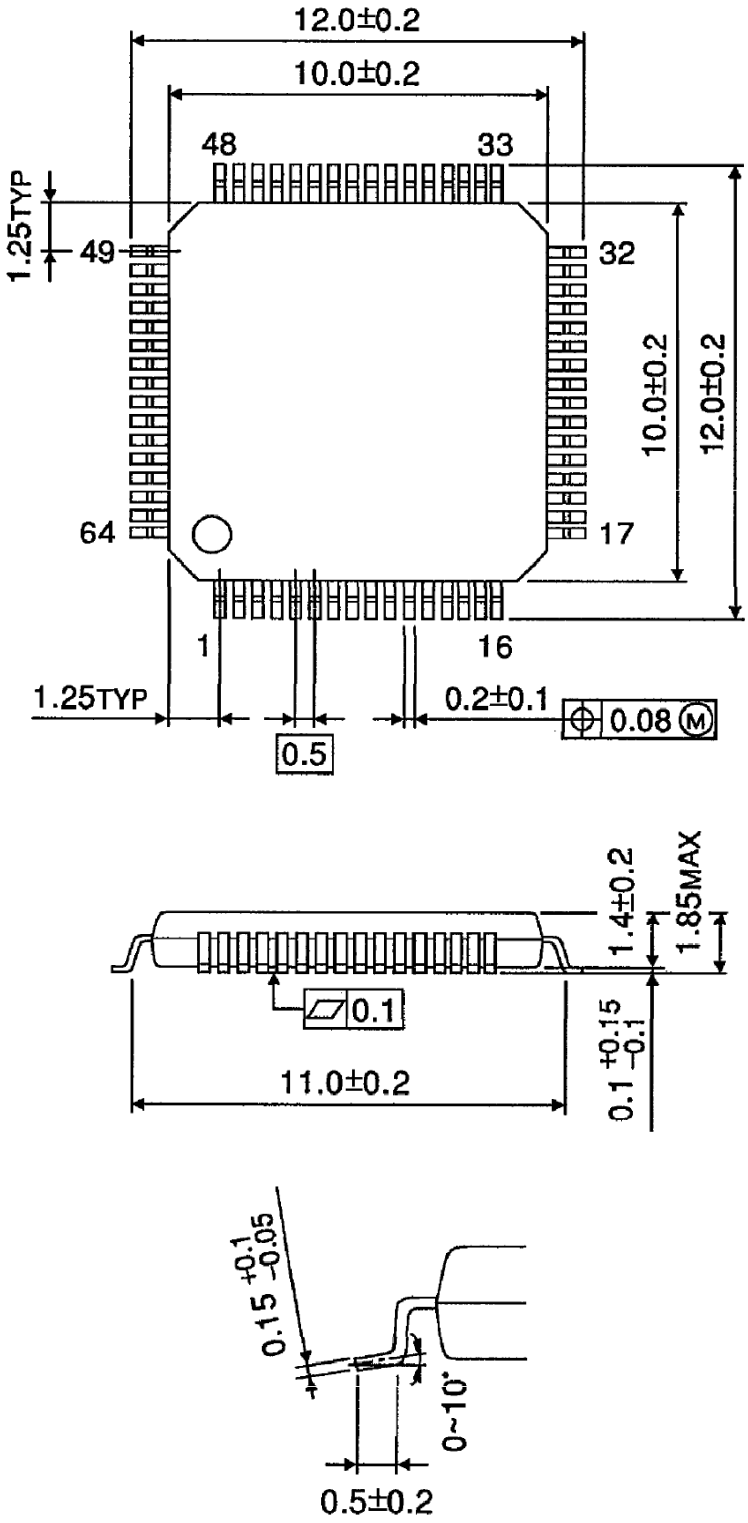
Type C: SDO0~3, MCKO, BCKO, LRCKO

Type D: GPO0~1, /MIACK

Type E: /MIDIO

Package Dimensions

LQFP64-P-1010-0.50E Unit: mm



(Note) Palladium plate

Weight : 0.4g (typ.)

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030619EBA

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