LINEAR INTEGRATED CIRCUIT

TCA940N

10W AUDIO POWER AMPLIFIER

The TCA 940N is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier. The TCA 940N provides 10W output power @ 20V/4Ω, 7W @ 16V/4Ω and 6.5W @ 20V/8Ω. It gives high output current (up to 3A), very low harmonic and cross-over distortion. Besides the thermal shut-down, the device contains a current limiting circuit which restricts the operation within the safe operating area of the power transistors. The TCA 940N is pin to pin equivalent to the TBA 810 AS.

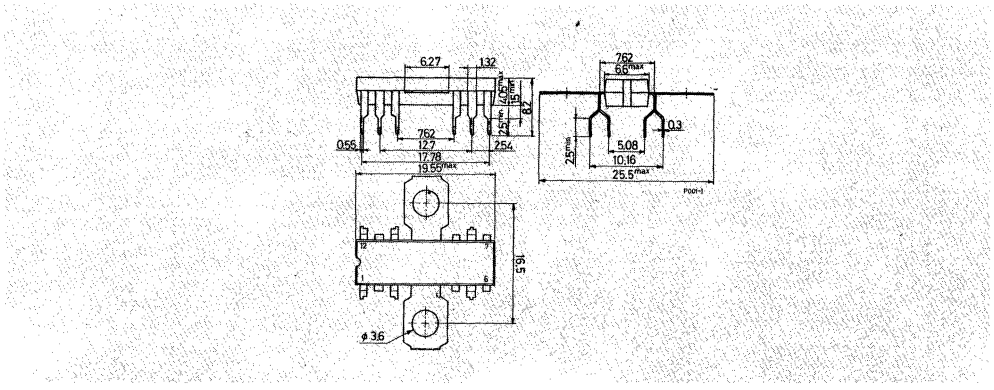
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (non-repetitive)	3.5	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation: at T_{amb} = 50°C	1.25	W
	at T_{tab} = 70°C	8	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TCA 940N

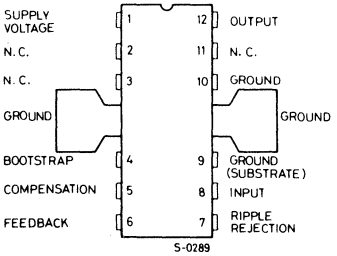
MECHANICAL DATA

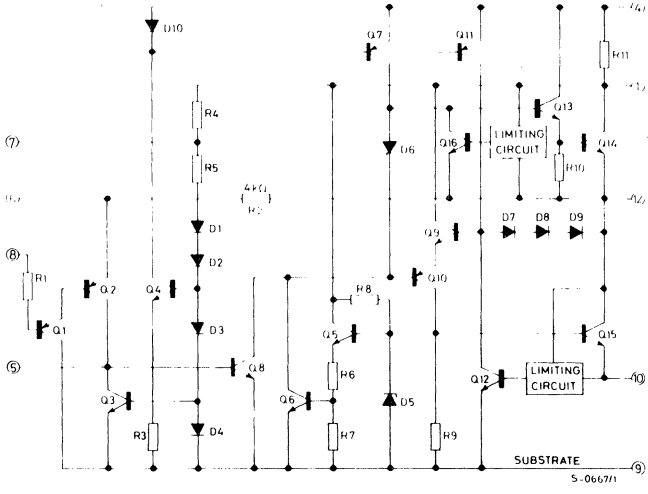
Dimensions in mm



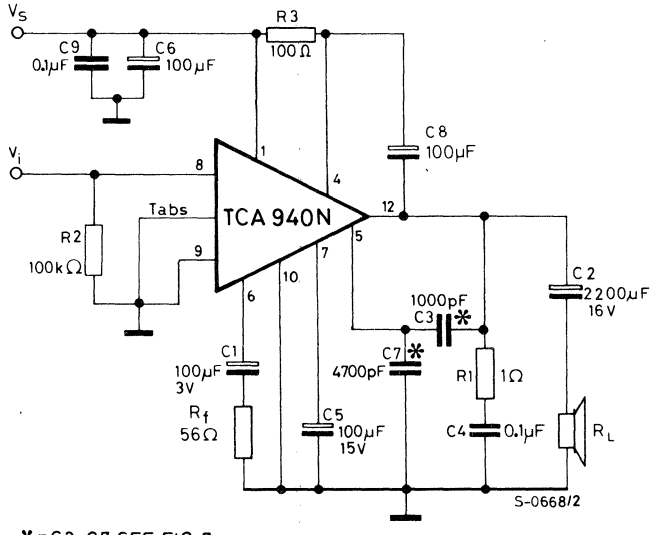
CONNECTION AND SCHEMATIC DIAGRAMS

(top view)





TEST AND APPLICATION CIRCUIT



*=C3, C7 SEE FIG. 7

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		6		28	V
V_o	Quiescent output voltage (pin 12)	V_s = 18V	8.2	9	9.8	V
I_d	Quiescent drain current	V_s = 12V V_s = 24V		13 20		mA mA
I_b	Input bias current (pin 8)	V_s = 18V		0.5		μA
P_o	Output power	d = 10% f = 1 kHz V_s = 20V R_L = 4Ω V_s = 18V R_L = 4Ω V_s = 16V R_L = 4Ω V_s = 20V R_L = 8Ω V_s = 18V R_L = 8Ω	 7	 10 9 7 6.5 5		 W W W W W
$V_{i(rms)}$	Voltage for input saturation		250			mV
V_i	Input sensitivity	P_o = 9W V_s = 18V R_L = 4Ω f = 1 kHz		 90		 mV
B	Frequency response (-3 dB)	V_s = 18V R_L = 4Ω C_3 = 1000 pF	40 Hz to 20 KHz			
d	Distortion	P_o = 50 mW to 5W V_s = 18V R_L = 4Ω f = 1 kHz		 0.3		 %
R_i	Input resistance (pin 8)			5		MΩ
G_v	Voltage gain (open loop)	V_s = 18V R_L = 4Ω f = 1 kHz		 75		 dB
G_v	Voltage gain (closed loop)	V_s = 18V R_L = 4Ω f = 1 kHz	 34	 37	 40	 dB
e_N	Input noise voltage	V_s = 18V R_g = 0		3		μV
i_N	Input noise current	V_s = 18V		0.15		nA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
η	Efficiency	P_o = 9W V_s = 18V R_L = 4Ω f = 1 kHz		65		%
SVR	Supply voltage rejection	V_s = 24V R_L = 4Ω f_{ripple} = 100 Hz		45		dB
I_d	Drain current	P_o = 9W V_s = 18V R_L = 4Ω		770		mA
T_{sd}	Thermal shut-down (*) Case temperature	P_{tot} = 4.8W		110		°C

(*) See fig. 15.

Fig. 1 - Output power vs. supply voltage.

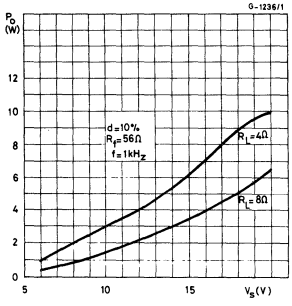


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

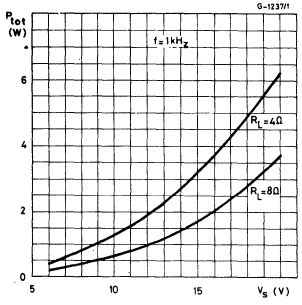


Fig. 3 - Distortion vs. output power.

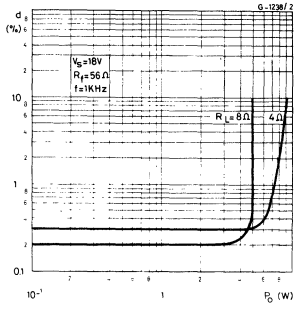


Fig. 4 - Voltage gain and input sensitivity vs. feedback resistance (R_f)

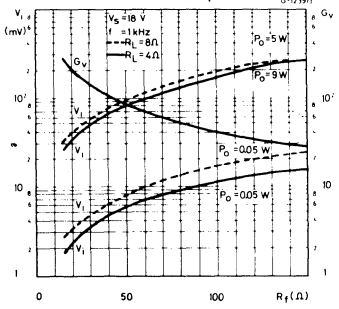


Fig. 5 - Distortion vs. frequency (R_L= 4Ω)

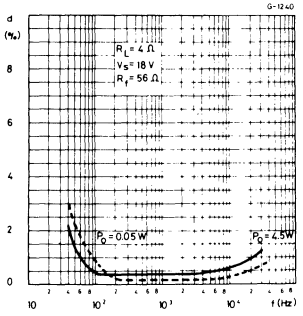


Fig. 6 - Distortion vs. frequency (R_L= 8Ω)

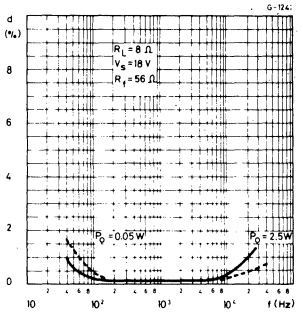


Fig. 7 - Value of C3 vs. R_f for different bandwidths

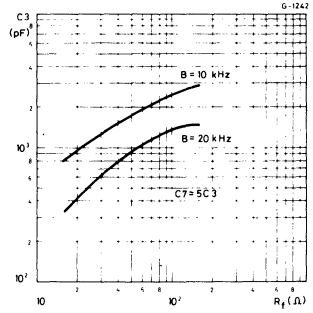


Fig. 8 - Supply voltage rejection vs. feedback resistance (R_f)

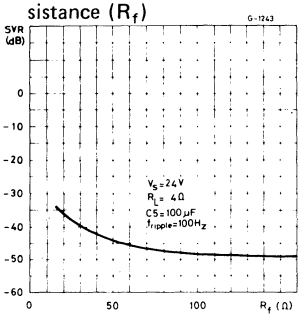


Fig. 9 - Power dissipation and efficiency vs. output power (R_L= 4Ω)

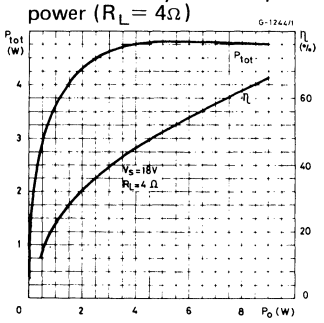


Fig. 10 - Power dissipation and efficiency vs. output power (R_L= 8Ω)

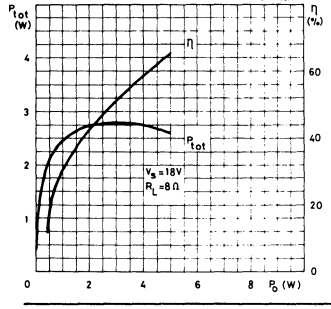


Fig. 11 - Quiescent output voltage (pin 12) vs. supply voltage

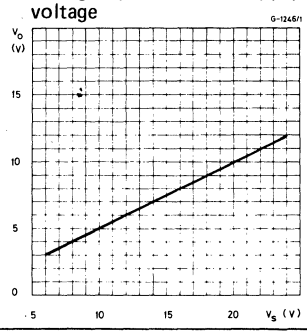
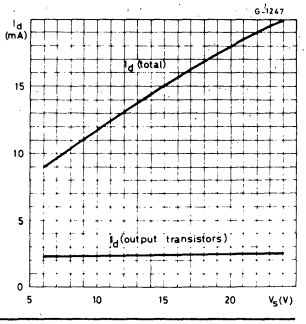


Fig. 12 - Quiescent current vs. supply voltage



SHORT CIRCUIT PROTECTION

The most important innovation in the TCA 940N is an original circuit which limits the current of the output transistors. Fig. 13 shows that the maximum output current is a function of the collector-emitter voltage; hence the circuit works within the safe operating area of the output power transistors. This can therefore be considered as being power limiting rather than simple current limiting. The TCA 940N is thus protected against temporary overloads or short circuit by the above circuit. Should the short circuit exists for a longer time, the thermal shut-down comes into action and keeps the junction temperature within safe limits.

Fig. 13 - Maximum output current vs. voltage (V_{CE}) across each output transistor

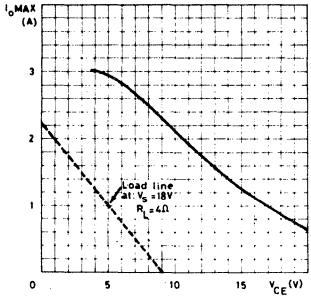
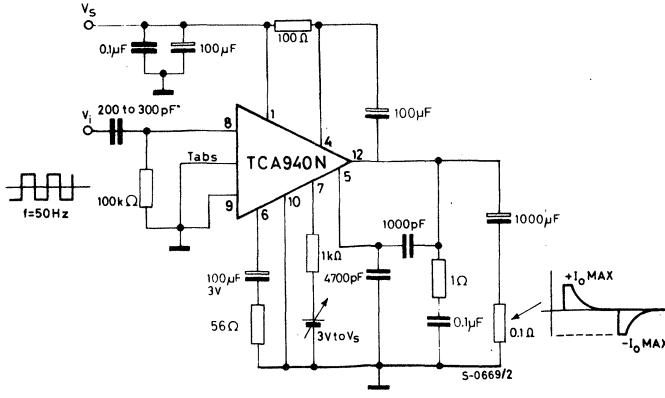


Fig. 14 - Test circuit for the limiting characteristics

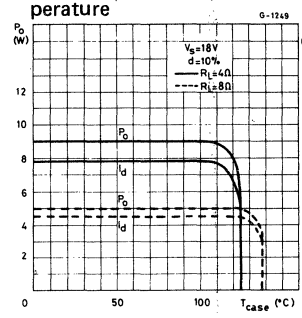


THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of too high a junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (fig. 15).

Fig. 15 - Output power and drain current vs. case temperature



MOUNTING INSTRUCTION

The power dissipated in the circuit may be removed by connecting the tabs to an external heatsink according to fig. 16. The desired thermal resistance may be obtained by fixing the TCA 940N to a suitably dimensioned plate as shown in fig. 17. This plate can also act as a support for the whole printed circuit board; the mechanical stresses do not damage the integrated circuit. During soldering the tabs temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 16 - Maximum allowable power dissipation vs. ambient temperature

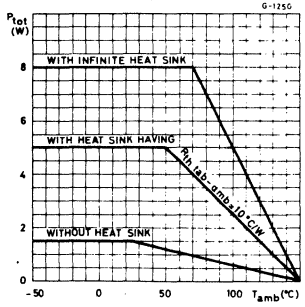


Fig. 17 - Mounting example

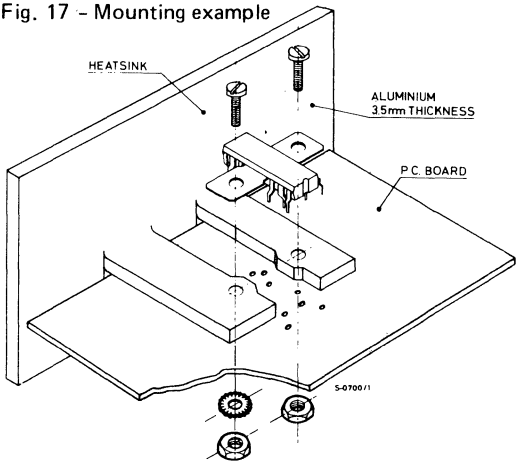


Fig. 18 - P.C. board and components layout of the test and application circuit (1:1 Scale).