

TENTATIVE TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

# TCD141ARC

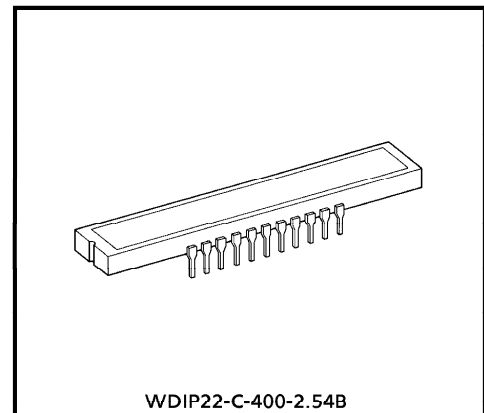
The TCD141ARC is a high sensitive and low dark current 5000-elements linear image sensor.

The sensor can be used for facsimile, imagescanner and OCR.

The device is contains a row of 5000 photodiodes, which provide a 16 lines/mm (400 DPI) across a A3 size paper.

**FEATURES**

- Number of Image Sensing Elements : 5000
- Image Sensing Element Size : 7 $\mu$ m by 7 $\mu$ m on 7 $\mu$ m centers
- Photo Sensing Region : High sensitive and low dark current pn photodiode
- Clock : 2 phase (12V)
- Package : 22 pin DIP
- Window Glass : Antireflected coating



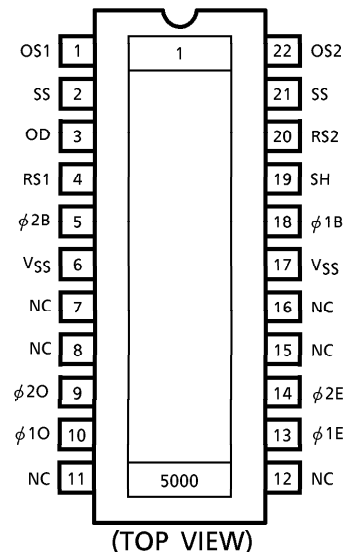
Weight : 5.4g (Typ.)

**MAXIMUM RATINGS (Note 1)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	$V_{\phi}$	- 0.3~15	V
Shift Pulse Voltage	$V_{SH}$		V
Reset Pulse Voltage	$V_{RS}$		V
Power Supply Voltage	$V_{OD}$		V
Operating Temperature	$T_{opr}$	- 25~60	°C
Storage Temperature	$T_{stg}$	- 40~100	°C

(Note 1) All voltage are with respect to SS and  $V_{SS}$  terminals (Ground).

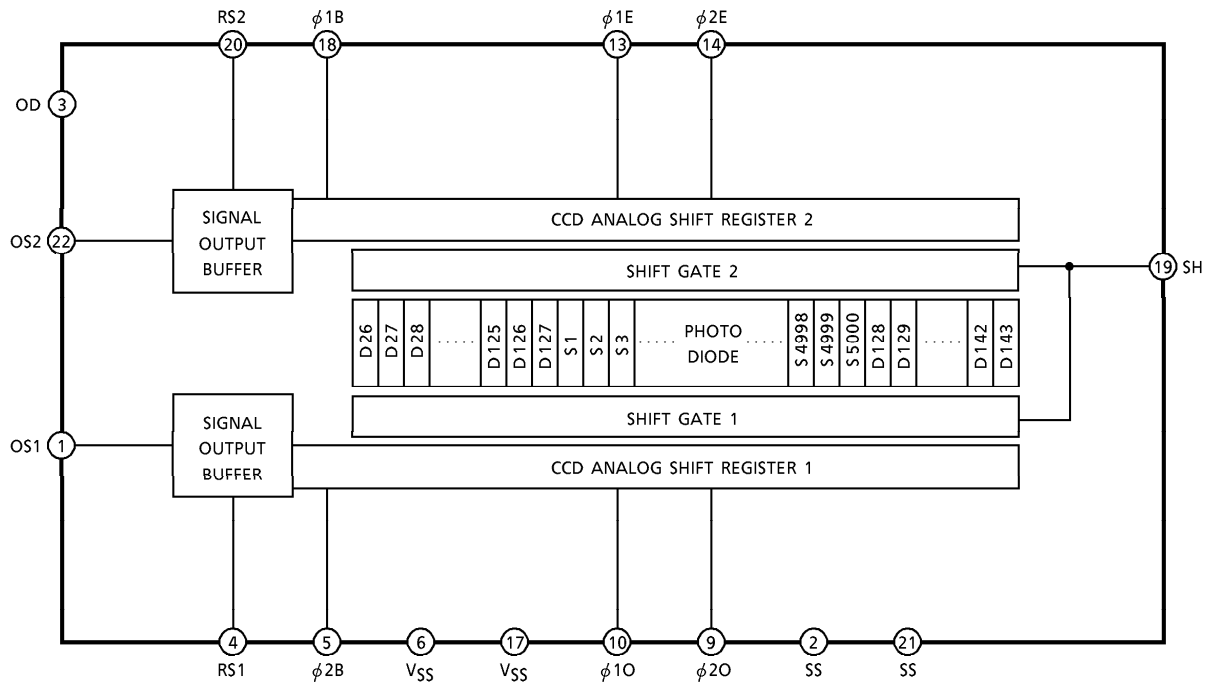
**PIN CONNECTIONS**



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CIRCUIT DIAGRAM



PIN NAMES

$\phi 1E, O$	Clock (Phase 1)
$\phi 2E, O$	Clock (Phase 2)
$\phi 1B$	Final Stage Clock (Phase 1)
$\phi 2B$	Final Stage Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
OS1	Signal Output 1
OS2	Signal Output 2
OD	Power
SS	Ground (Analog)
V <sub>SS</sub>	Ground (Digital)
NC	Non Connection

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**OPTICAL / ELECTRICAL CHARACTERISTICS**

(Ta = 25°C, V<sub>OD</sub> = 12V, V<sub>φ</sub> = V<sub>RS</sub> = V<sub>SH</sub> = 12V (PULSE), f<sub>φ</sub> = 1.0MHz, t<sub>INT</sub> (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP, LOAD RESISTANCE = 100kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	2.0	2.5	3.0	V / lx·s	(Note 2)
Photo Response Non Uniformity	PRNU (1)	—	—	10	%	(Note 3)
	PRNU (3)	—	—	10	mV	(Note 4)
Saturation Output Voltage	V <sub>SAT</sub>	1.0	1.5	—	V	(Note 5)
Saturation Exposure	SE	0.33	0.6	—	lx·s	(Note 6)
Dark Signal Voltage	V <sub>DRK</sub>	—	—	5	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	—	—	5	mV	(Note 7)
DC Power Dissipation	P <sub>D</sub>	—	100	325	mW	
Total Transfer Efficiency	TTE	92	95	—	%	
Output Impedance	Z <sub>O</sub>	—	0.5	1.0	kΩ	
Dynamic Range	DR	—	300	—		(Note 8)
DC Signal Output Voltage	V <sub>OS1</sub>	3.0	4.0	5.5	V	(Note 9)
	V <sub>OS2</sub>	3.0	4.0	5.5	V	(Note 9)
DC Mismatch Voltage	V <sub>OS1</sub> -V <sub>OS2</sub>	—	—	300	mV	

(Note 2) Sensitivity for 2856K W-lamp is 7.5V / lx·s (Typ.)

(Note 3) Measured at 50% of SE (Typ.)

$$\text{Definition of PRNU : PRNU} = \frac{\Delta x}{\bar{x}} \times 100 (\%)$$

Where  $\bar{x}$  is average of total signal outputs and  $\Delta x$  is the maximum deviation from  $\bar{x}$  under uniform illumination. (Channel 1)

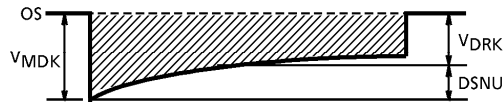
In the case of 2500 elements (Channel 2), the condition is the same as above too.

(Note 4) PRNU (3) is defined as maximum voltage with next pixel.  
Where measured 5% of SE (Typ.)

(Note 5) V<sub>SAT</sub> is defined as minimum saturation output voltage of all effective pixels.

$$\text{(Note 6) Definition of SE : SE} = \frac{V_{SAT}}{R} \text{ (lx·s)}$$

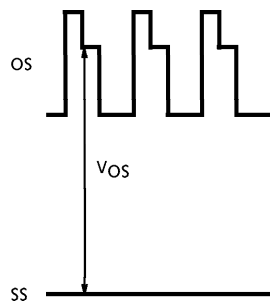
(Note 7)  $V_{DRK}$  is defined as average dark signal voltage of all effective pixels.  
 $DSNU$  is defined as different voltage between  $V_{DRK}$  and  $V_{MDK}$  when  $V_{MDK}$  is maximum dark signal voltage.



(Note 8) Definition of DR :  $DR = \frac{V_{SAT}}{V_{DRK}}$

$V_{DRK}$  is proportional to  $t_{INT}$  (Integration Time).  
 So the shorter  $t_{INT}$  condition makes wider DR value.

(Note 9) DC signal output voltage (Channel 1, 2).



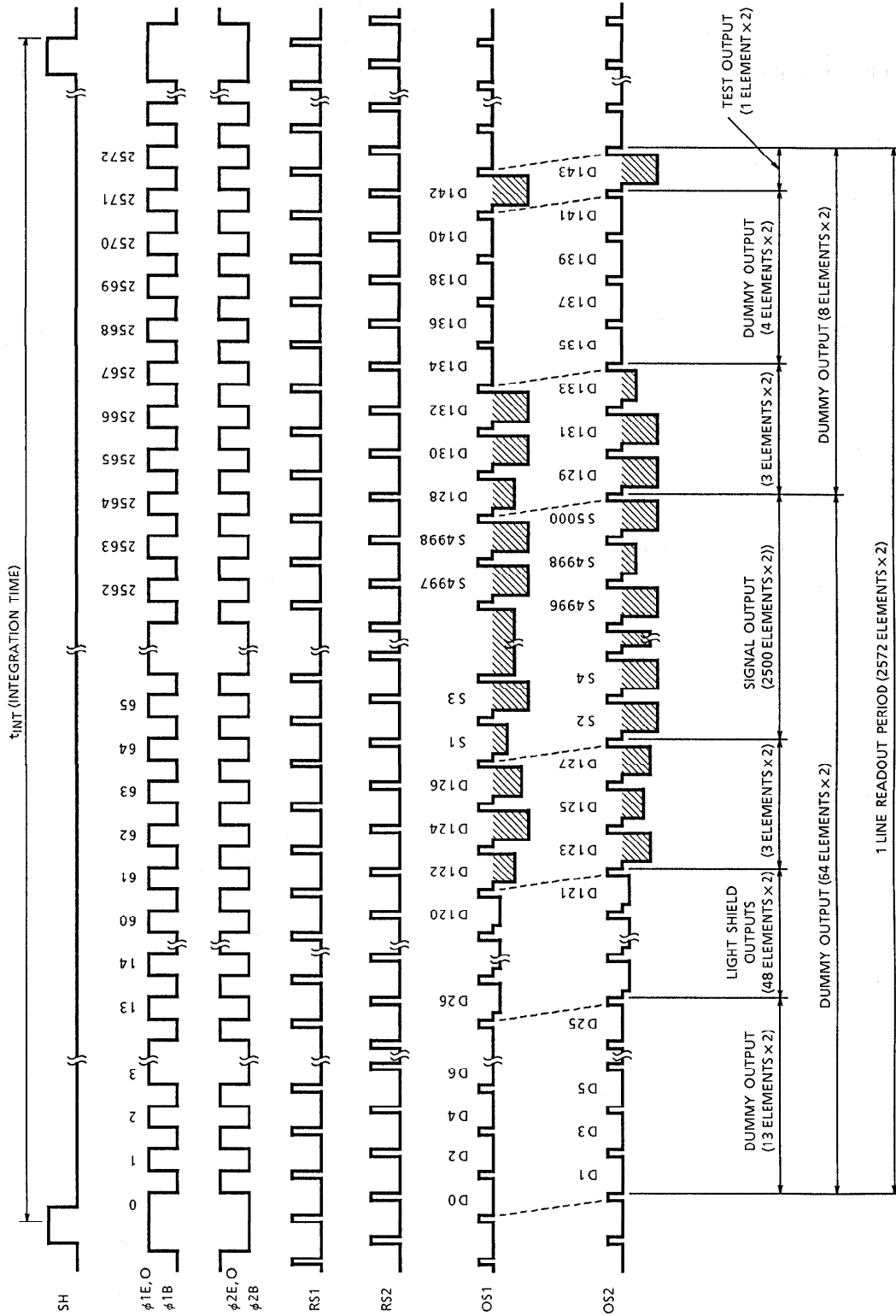
## OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	$V_{\phi 1E, O}$	$V_{OD} - 1$	$V_{OD}$	$V_{OD}$	V
	"L" Level	$V_{\phi 2E, O}$	0	0.5	0.8	
Final Stage Clock Pulse Voltage	"H" Level	$V_{\phi 1B}$	$V_{OD} - 1$	$V_{OD}$	$V_{OD}$	V
	"L" Level	$V_{\phi 2B}$	0	0.5	0.8	
Shift Pulse Voltage	"H" Level	$V_{SH}$	$V_{OD} - 1$	$V_{OD}$	$V_{OD}$	V
	"L" Level		0	0.5	0.8	
Reset Pulse Voltage	"H" Level	$V_{RS1}$	$V_{OD} - 1$	$V_{OD}$	$V_{OD}$	V
	"L" Level	$V_{RS2}$	0	0.5	0.8	
Power Supply Voltage		$V_{OD}$	11.4	12	13	V

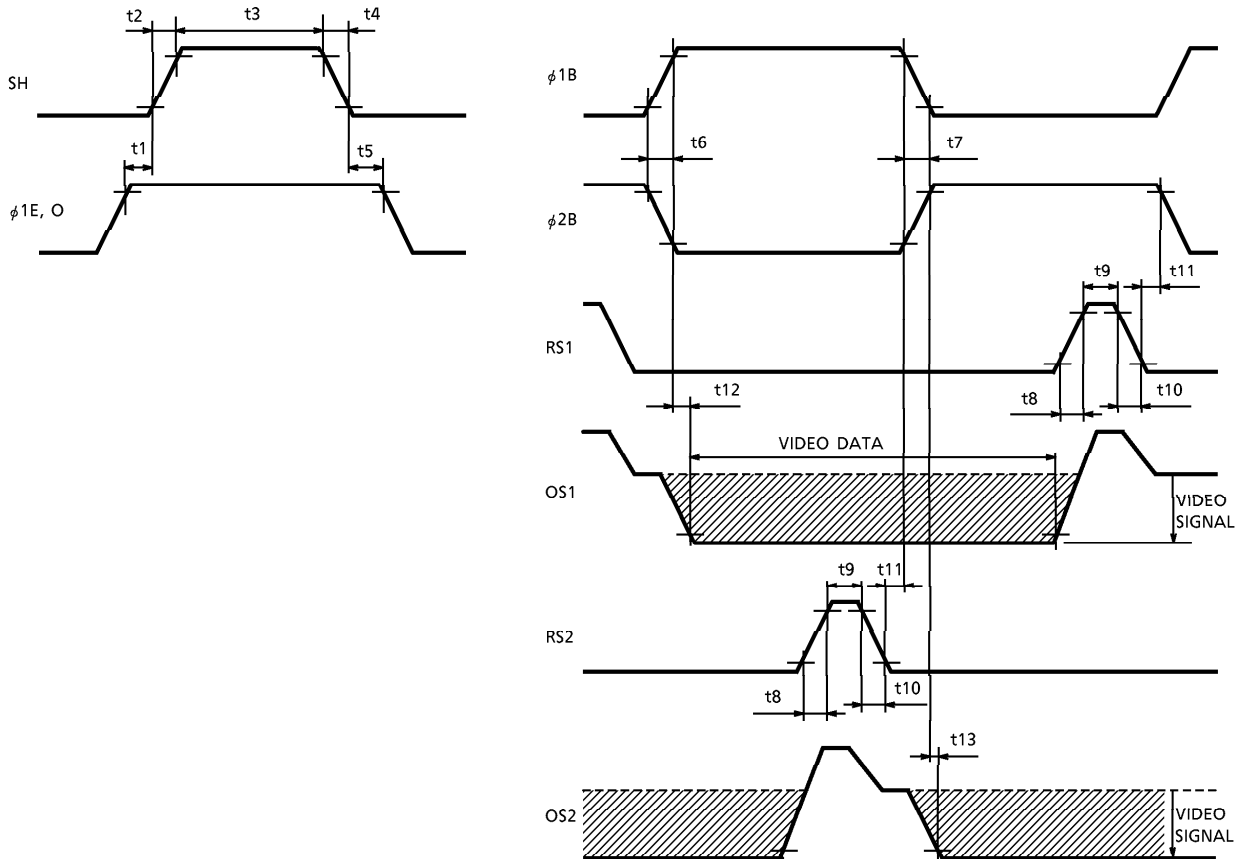
## CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	$f_{\phi}$	—	1	10	MHz
Reset Pulse Frequency	$f_{RS}$	—	1	10	MHz
Clock Capacitance	$C_{\phi E, O}$	—	450	550	pF
Final Stage Clock Capacitance	$C_{\phi B}$	—	10	20	pF
Shift Gate Capacitance	$C_{SH}$	—	250	350	pF
Reset Gate Capacitance	$C_{RS}$	—	10	20	pF

TIMING CHART



TIMING REQUIREMENTS

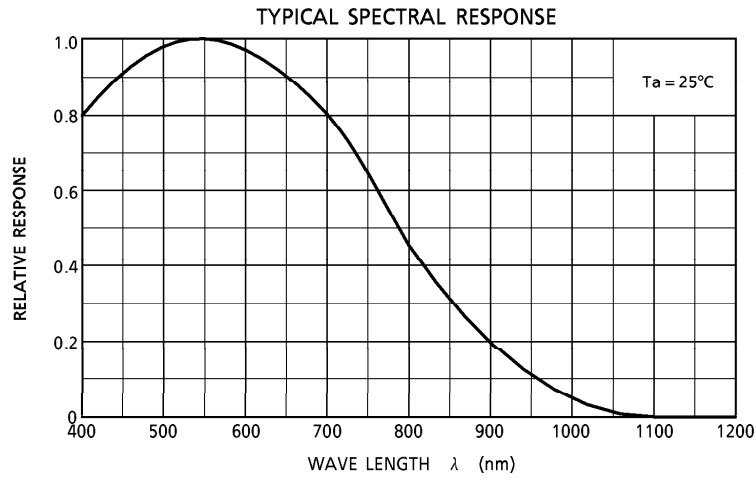


CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and $\phi 1E, O$	$t_1, t_5$	0	100	—	ns
SH Pulse Rise Time, Fall Time	$t_2, t_4$	0	50	—	ns
SH Pulse Width	$t_3$	300	1000	—	ns
$\phi 1B, \phi 2B$ Pulse Rise Time, Fall Time	$t_6, t_7$	0	100	—	ns
RS Pulse Rise Time, Fall Time	$t_8, t_{10}$	0	20	—	ns
RS Pulse Width	$t_9$	20	250	—	ns
Pulse Timing of $\phi 1B, \phi 2B, RS$	$t_{11}$	0	250	—	ns
Video Data Delay Timing (Note 11)	$t_{12}, t_{13}$	—	30	—	ns

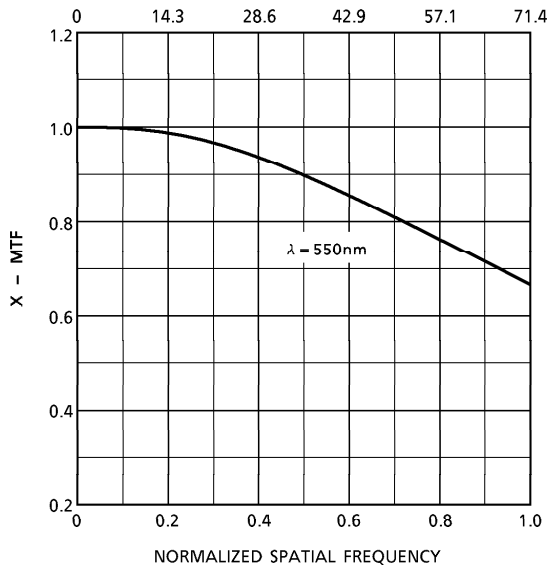
(Note 10) TYP, is the case of  $f_{RS} = 1\text{MHz}$ .

(Note 11) Load Resistance is  $100\text{k}\Omega$ .

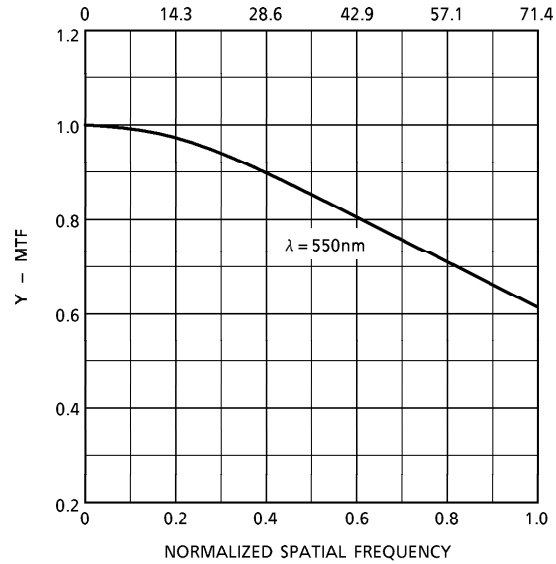
**TYPICAL PERFORMANCE CURVES**



**MODULATION TRANSFER FUNCTION OF X-DIRECTION**  
 SPATIAL FREQUENCY (Cycles/mm)

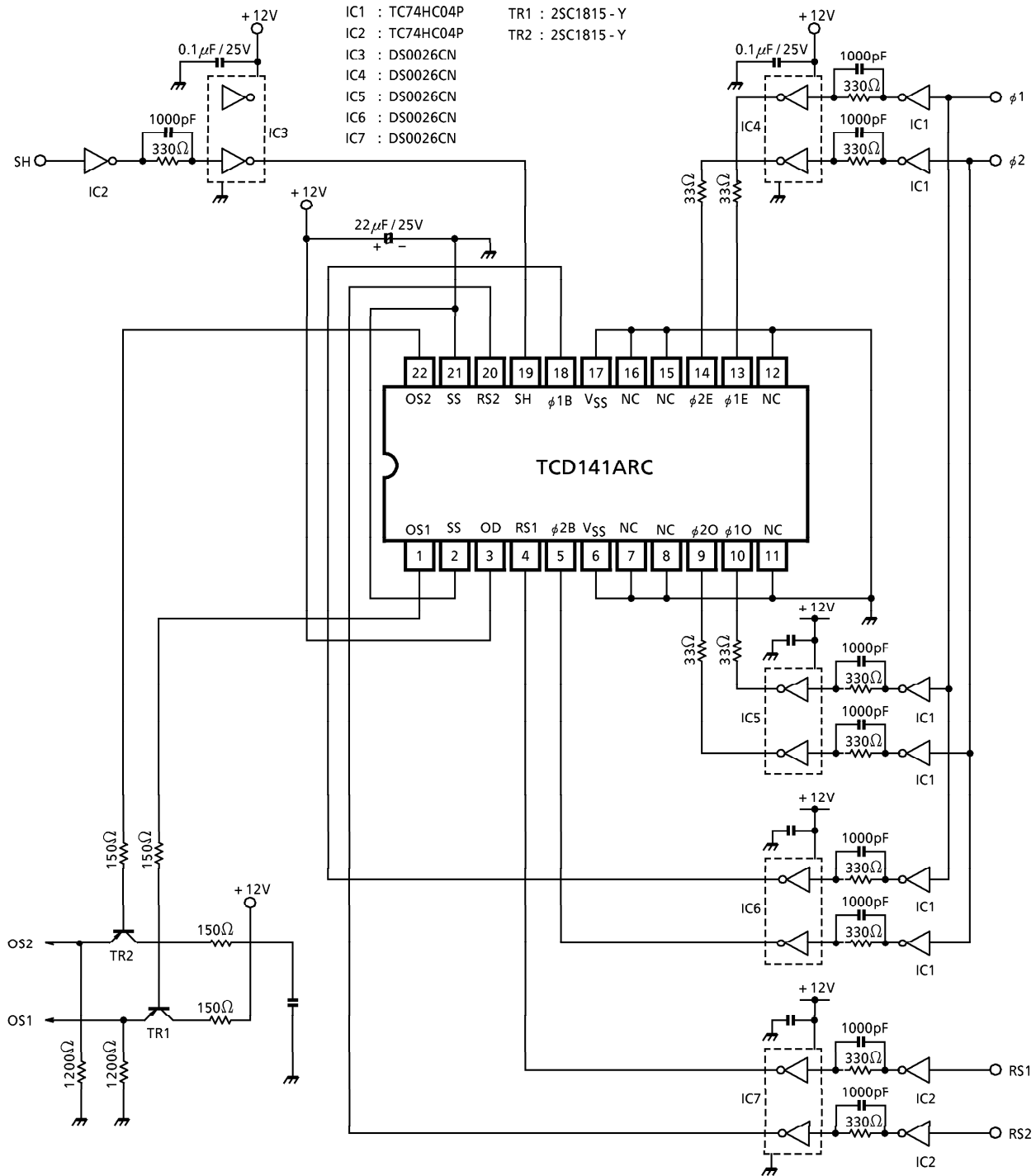


**MODULATION TRANSFER FUNCTION OF Y-DIRECTION**  
 SPATIAL FREQUENCY (Cycles/mm)





TYPICAL DRIVE CIRCUIT



**CAUTION****1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N<sub>2</sub>.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

**2. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

**3. Incident Light**

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

**4. Lead Frame Forming**

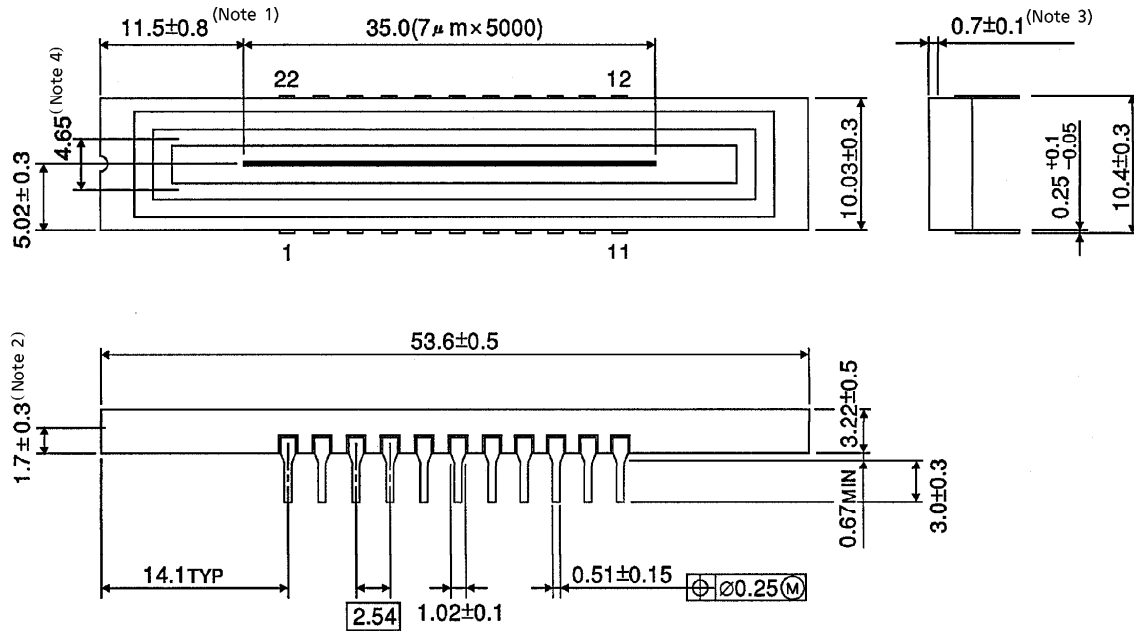
Since this package is not stout against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

PACKAGE OUTLINE

WDIP22-C-400-2.54B (B)

Unit in mm



- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)
- (Note 4) ANTIREFECTED COATING AREA.

Weight : 5.4g (Typ.)