MOTOROLA

TCF6000

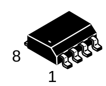
Peripheral Clamping Array

The TCF6000 was designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods

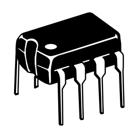
PERIPHERAL CLAMPING ARRAY

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

NO SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS

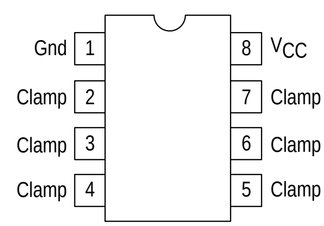
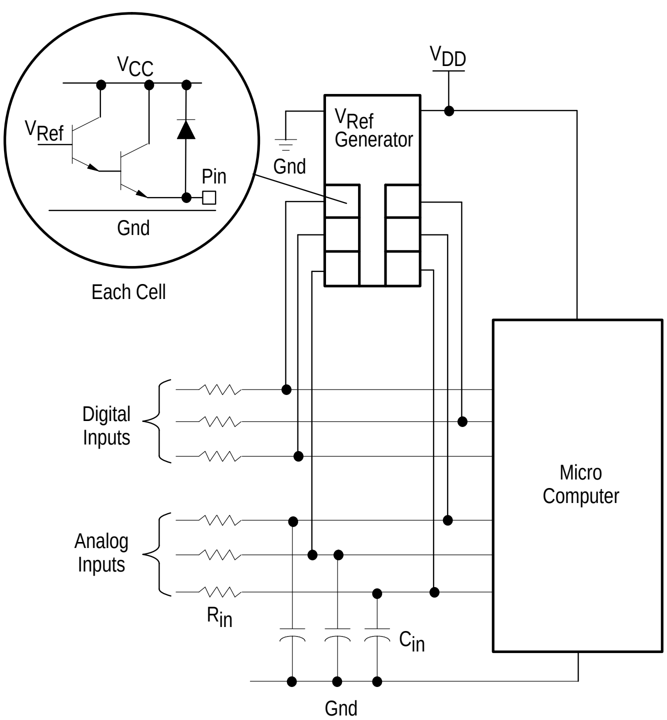


Figure 1. Representative Block Diagram and Simplified Application



ORDERING INFORMATION

Device	Operating Temperature Range	Package
TCF6000D	T_A = – 40° to +85°C	SO–8
TCF6000		Plastic DIP

 Rev 0

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Supply Current	I_i	300	mA
Clamping Current	I_{IK}	±50	mA
Junction Temperature	T_J	150	°C
Power Dissipation (T_A = + 85°C)	P_D	400	m/W
Thermal Resistance (Junction–Ambient)	θ_{JA}	100	°C/W
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to + 150	°C

NOTE: 1. Values beyond which damage may occur.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 4.5 ≤ V_{CC} ≤ 5.5 V, unless otherwise noted.)

Characteristics	Symbol	Min	Max	Unit
Positive Clamping Voltage (Note 2) (I_{IK} = 10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	–	V_{CC} + 1.0	V
Positive Peak Clamping Current	$I_{IK(P)}$	–	20	mA
Negative Peak Clamping Voltage (I_{IK} = –10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	–0.3	–	V
Negative Peak Clamping Current	$I_{IK(P)}$	–20	–	mA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC}) (0 V ≤ V_{in} ≤ V_{CC}, –40°C ≤ T_A ≤ + 85°C)	 I_L I_{LT}	 – –	 1.0 5.0	µA
Channel Crosstalk (A_{CT} = 20 log I_L/I_{IK})	A_{CT}	100	–	dB
Quiescent Current (Package)	I_B	–	2.0	mA

NOTE: 2. The device might not give 100% protection in CMOS applications.

CIRCUIT DESCRIPTION

To ensure the reliable operation of any integrated circuit based electronics system, care has been taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch–up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is –0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown if Figure 2b lies mainly with the high current drain through the biassing devices R_1 and D_3. A second problem exists if the input line carries an analog signal. When V_{in} is close to the ground potential, currents arising from leakage and mismatch between D_3 and D_2 can be sourced into the input line, thus disturbing the reading.

Figure 2. Classical Protection Circuits

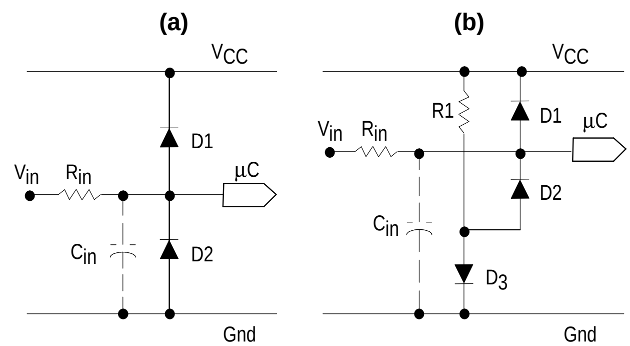
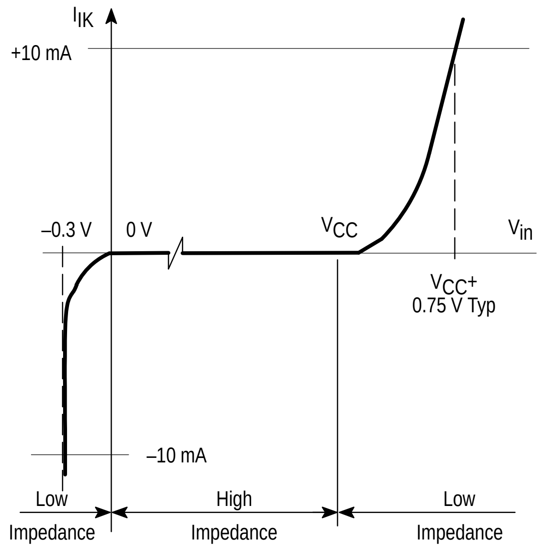


Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the V_{CC} supply line.

Figure 3. Clamping Characteristics



APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

The value of the input resistors, R_{in}, is determined by the clamping current and the anticipated value of the spikes.

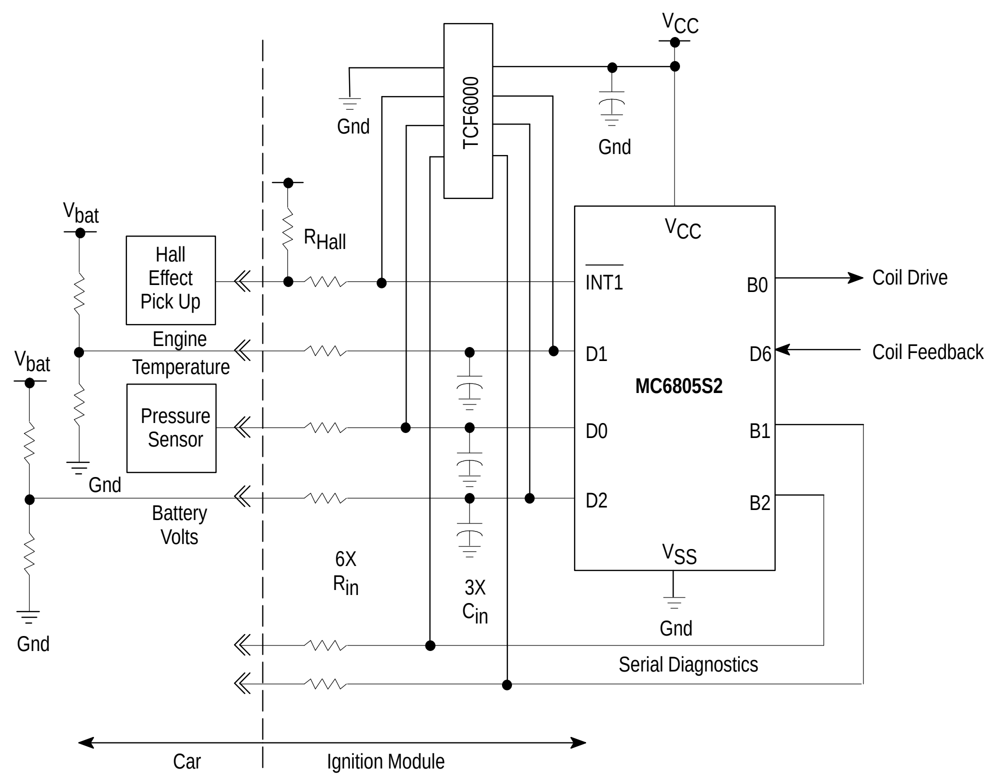
Thus:

$$R_{in} = \frac{V}{I_{IK}}\ \Omega$$

where:	V	= Peak Volts (V)
	I_{IK}	= Clamping current (A)
So, taking,	V	= 300 V typically (SAE J1211)
	I_{IK}	= 10 mA (recommended)
gives,	R_{in}	= 30 k

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for Bipolar systems.

Figure 4. Typical Automotive Application



The use of C_{in} is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 pF to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor C_{in} is necessary for devices such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for C_{in} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_{in}.

Thus for a resistive input A/D connector where:

T_S = Sample time (seconds)
R_D = Device input resistance (Ω)
V_{in} = Input voltage (V)
k = Required accuracy (%)
Q_1 = Charge on capacitor before sampling
Q_2 = Charge on capacitor after sampling
I_D = Device input current (A)

Thus: $Q_1 – Q_2 = \frac{k \times Q_1}{100}$

but, $Q_1 = C_{in} V_{in}$
and, $Q_1 – Q_2 = I_D \bullet T_S$

so that, $I_D T_S = \frac{k \bullet C_{in} – V_{in}}{100}$

and, $C_{in} \text{ (min)} = \frac{I_D \bullet T_S}{V_{in} \bullet k}$ Farad

so, $C_{in} \text{ (min)} = \frac{100 \bullet T_S}{k \bullet R_D}$ Farad

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)
C_H = Hold capacitor (Farad)

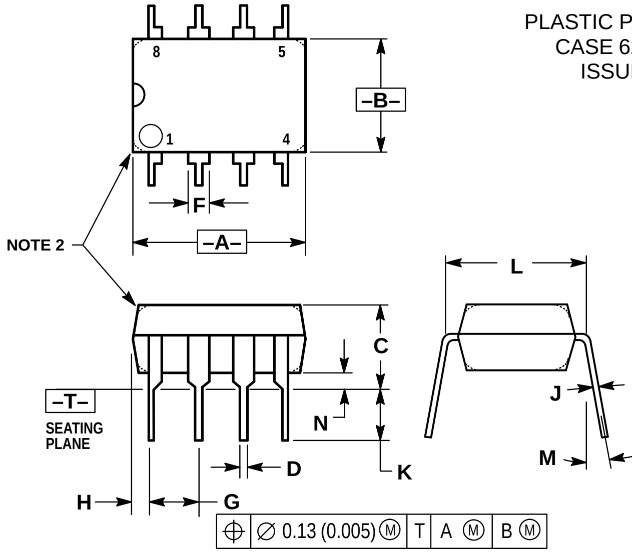
$C_{in} \text{ (min)} = \frac{100 \bullet C_H}{k}$ Farad

For the MC6805S2 this comes out at:

$C_{in} \text{ (min)} = \frac{100.25 \text{ pF}}{0.25}$ = 10 nF for 1/4% accuracy

OUTLINE DIMENSIONS

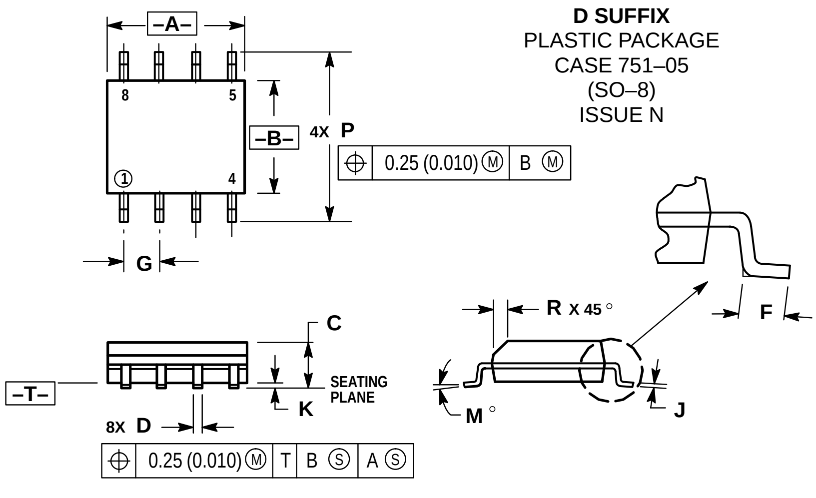
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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