SPECIFICATION

For

TCM—A1172

Q clock / KS3000 用

This specifcation consists of two documents as follows.

1.LCD Specification	SC-011043600
2.LCD QA Standard	S4-00301

Customer's Approval	
Date by	Date: Presented by
	SEIKO EPSON CORPORATION LCD Division Quality Assurance Department

ORIGINAL

SPEC CODE: SC-900117200

SPECIFICATION

TCM-A1172

SEIKO EPSON CORPORATION
LCD DIVISION

LCD Design department		

P/N	Rev.	Revision Item	Date
TCM-A1172	0	New	1999/06/30

1.BASIC SPECIFICATIONS

1.1.Display Specifications

1) LCD Mode : FTN *1 :Positive : Transflective
2) Display Color *2
   - Display Color : Display Data "1": Black
   - Background Color : Display Data "0": White
3) Viewing Angle : 6 0'clock Direction
4) Driving Duty and Bias : 1/65 Duty, 1/7Bias

*1 Color tone is slightly changed by temperature and driving voltage.

1.2. Mechanical Specifications

1) Outline Dimension : Refer to attached outline dimensions figure TD-270455
2) Pixels Matrix : 128pixels × 64 pixels
3) Pixel Size : 0.34 × 0.38 (mm)
4) Pixel Pitch : 0.37 × 0.41 (mm)
5) Weight : Approx. 10 (g)

1.3. Terminal Functions

No	Symbol	I/O	Function
1	NC	-	No Connection
2	FR	-	No use. Setting Open.
3	CL	-	This is the display clock input terminal The following table is true depending on the M/S and CLS status. M/S: H — CLS: H — Oscillator Circuit: Enabled — Power Supply Circuit: Enabled — CL: Output M/S: — CLS: L — Oscillator Circuit: Disabled — Power Supply Circuit: Enabled — CL: Input
4	/DOF	-	No use. Setting Open.
5	/CS1	I	This is the chip select signal. When /CS1 = "L", the chip select becomes active, and data/command I/O is enabled.
6	CS2	I	This is the chip select signal. When /CS1 = "L", the chip select becomes active, and data/command I/O is enabled.
7	/RES	I	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level.
8	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
9	/WR (R/W)	I	When connected to 80**-Series MPU, this terminal is active "L". This terminal connects to the 80**-Series MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to 6800 Series MPU; This is the read / write control signal input terminal. R/W = "H" : Read R/W = "L" : Write
10	/RD (E)	I	When connected to 80**-Series MPU, this terminal is active "L". This terminal is connected to the 80**-Series MPU /RD signal. The data bus is in an output status when this signal is "L". When connected to 6800 Series MPU , this terminal is active "H". This is the 6800 Series MPU enable clock input
11~18	D0~D7	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S ="L"), then D7(SI) serves as the serial data input and D6(SCL) serves as the serial clock input terminal. At this time, D0 to D5 terminals are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
19	V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.
20	V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.
21	V_{SS2}	Power Supply	This is a reference power supply for the step-up voltage circuit for the liquid crystal drive.
22	V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.
23	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
24	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
25	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.

No.	Symbol	I/O	Function
26	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
27	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
28	V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.
29	VRS	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. This function is not used. Please "Open " this terminal.
30	V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.
31~35	V1~ V5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an operating amplifier. The voltage levels are determined based on V_{DD}, and must maintain the relative magnitudes shown below. V_{DD} (=V0)≥V1≥V2≥V3≥V4≥V5 Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command. V1 1/7 * V5 or 1/9V5 V2 2/7 * V5 or 2/9V5 V3 5/7 * V5 or 7/9V5 V4 6/7 * V5 or 8/9V5
36	VR	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V5 through a resistive voltage divider. When IRS terminal is "L", these are only enabled when the V5 voltage regulator internal resistors are not used. When IRS terminal is "H", these cannot be used when the V5 voltage regulator internal resistors are used.
37	V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.
38	M/S	I	This is master/slave operation select signal "H" is selected. Master operation

M/S	CLS	Oscillator Circuit	Power Supply Circuit	CL
H	H	Enabled	Enabled	Output
	L	Disabled	Enabled	Input

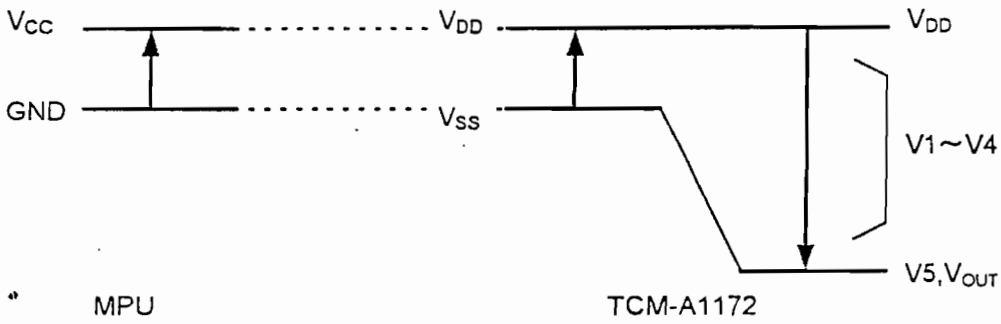
39	CLS	I	Terminal to select whether or enable or disable the display clock internal oscillator circuit. CLS = "H" : Internal oscillator circuit is enabled CLS = "L" : Internal oscillator circuit is disabled (requires external input) When CLS = "L" , input the display clock through the CL terminal.
40	C86	I	This is the MPU interface switch terminal. C86 = "H" : 6800 Series MPU interface. C86 = "L" : 80**-Series MPU interface.

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>41</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = "H" : Parallel data input.
P/S = "L" : Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>L</td><td>A0</td><td>SI(D7)</td><td>Write Only</td><td>SCL(D6)</td></tr>
</table>
When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. /RD(E) and /WR (R/W) are fixed to either "H" or "L".
With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>42</td><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = "H" : Normal mode
/HPM = "L" : High power mode</td></tr>
<tr><td>43</td><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = "H": Use the internal resistors.
IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.</td></tr>
<tr><td>44</td><td>NC</td><td>-</td><td>No Connection</td></tr>
</table>

2.ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS}=0V(GND)

Item		Symbol	Standard Value		Unit	Condition
			Min.	Max.		
Supply Voltage (1)		V_{DD}	-0.3	+7.0	V	
Power Supply Voltage (2) (V_{DD} standard)		Vss2	-7.0	+0.3		
	With 3×boosting		-6.0	+0.3		
	With 4×boosting		-4.5	+0.3		
Power Supply Voltage (1)	(V_{DD} standard)	V5,V_{OUT}	-18.0	+0.3		
Power Supply Voltage (2)	(V_{DD} standard)	V1,V2,V3,V4	V5	+0.3		
Input Voltage		V_{IN}	-0.3	V_{DD}+0.3		
Output Voltage		V_O	-0.3	V_{DD}+0.3		
Operating Temperature		T_{OP}	-20	+70	°C	No Condensation
Storage Temperature		T_{ST}	-20	+70		No Condensation



Notes and Cautions

1. The V1 to V5 and V_{OUT} are relative to the V_{DD} = 0V standard.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

3.ELECTRICAL CHARACTERISTICS

3.1.DC Characteristics

3.1.1.Module DC Characteristics

V_{SS} = 0V, V_{DD} = 2.7~3.3V, Top = -20~70°C

Item		Symbol	Condition	Standard Value			Units	Applicable Terminals
				Min.	Typ.	Max.		
Operating Voltage(1)	Recommended Voltage	V_{DD}		2.7	3.0	3.3	V	V_{DD} *1
	Possible Operating Voltage			1.8		5.5		V_{DD} *1
Operating Voltage(2)	Recommended Voltage	Vss2		-3.3		-2.7		Vss2
	Possible Operating Voltage	Vss2		-6.0		-1.8		Vss2
Operating Voltage(2)	Possible Operating Voltage	V5	V_{DD}=0	--16	-	-4.5		V5 *2
	Possible Operating Voltage	V1, V2	V_{DD}=0	0.4xV_5	-	V_{DD}		V1,V2
	Possible Operating Voltage	V3, V4	V_{DD}=0	V5	-	0.6xV5		V3,V4
High-level Input Voltage		V_{IHC}		0.8xV_{DD}	-	V_{DD}		*3
Low-level Input Voltage		V_{ILC}		V_{SS}	-	0.2xV_{DD}		*3
High-level Output Voltage		V_{OHC}	I_{OH}=-0.5mA	0.8xV_{DD}	-	V_{DD}		*4
Low-level Output Voltage		V_{OLC}	I_{OH}=0.5mA	V_{SS}	-	0.2xV_{DD}		*4
Input leakage current		I_{LI}	V_{IN}= V_{DD} or V_{SS}	-1.0	-	1.0	μA	*5
Output leakage current		I_{LO}		-3.0	-	3.0		*6
Input Terminal Capacitance		C_{IN}	T_{OP}=25°C, f=1MHz	-	5.0	8.0	pF	
Frame Frequency		fFR	T_{OP}=25°C	69	85	100	Hz	

V_{DD} = 0V, Top = -20~70°C

Item		Symbol	Standard Value			Units	Applicable Terminals
			Min.	Typ.	Max.		
Internal Power Supply Circuit	Input voltage With 3x boosting	V_{SS2}	-6.0	-	-1.8	V	
	Input voltage With 4x boosting	V_{ss2}	-4.5	-	-1.8		
	Booster output voltage	V_{OUT}	-18.0	-	-6.0		V_{OUT}
	Voltage Follower Circuit Operating Voltage	V5	-16.0	-	-4.5		V5 *7
	Base Voltage	V_{REG}	-2.16	-2.10	-2.04		

T_{OP}=25[illegible]

■ Dynamic Consumption Current, During Display, with the Internal Power Supply OFF

Top = 25°C

Item	Symbol	Parameters	Standard Value			Units	Applicable Terminals
			Min.	Typ.	Max.		
Dynamic Consumption Current	I_{DD}	V_{DD}=5.0V, V_{DD}-V5=8.5V	-	30	70	μA	V_{DD}
		V_{DD}=3.0V, V_{DD}-V5=8.5V	-	30	70		

■ Dynamic Consumption Current, During Display, with the Internal Power Supply ON

Top = 25°C

Item	Symbol	Parameters		Standard Value			Units	Applicable Terminals
				Min.	Typ.	Max.		
Dynamic Consumption Current	I_{DD}	V_{DD}=5.0V, 3 x Booster Voltage V_{DD}-V5=8.5V *8	Normal Mode	-	150	700	μA	V_{DD}
			High-Power Mode	-	200	700		
		V_{DD}=5.0V, 3 x Booster Voltage V_{DD}-V5=8.5V *8	Normal Mode	-	190	800		
			High-Power Mode	-	250	900		

■ Consumption Current at Power Saver Mode

Top = 25°C

Item	Symbol	Parameters	Standard Value			Units	Applicable Terminals
			Min.	Typ.	Max.		
Sleep Mode	I_{DDS1}		-	0.01	5	μA	V_{DD}
Standby Mode	I_{DDS2}		-	4	8		

References for items marked with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 When the external power supply is being used, the operating voltage range for the V_{DD} system and the V5 system is shown in below figure.

*3 The A0, D0 to D5, D6(SCL), D7(SI), /RD(E), /WR(R/W), /CS1, CLS, CL,C86, P/S, /RES, IRS, and /HPM terminals.

*4 The D0 to D5, D6(SCL), CL terminals.

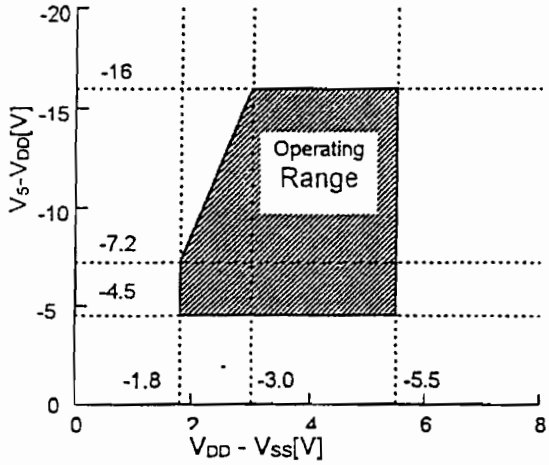
*5 The A0, /RD(E), /WR(R/W), /CS1, CLS, M/S, C86, P/S, /RES, IRS and /HPM terminals.

*6 Applies when the D0 to D5, D6(SCL), D7(SI), CL, terminals are in a high impedance state.

*7 The V5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

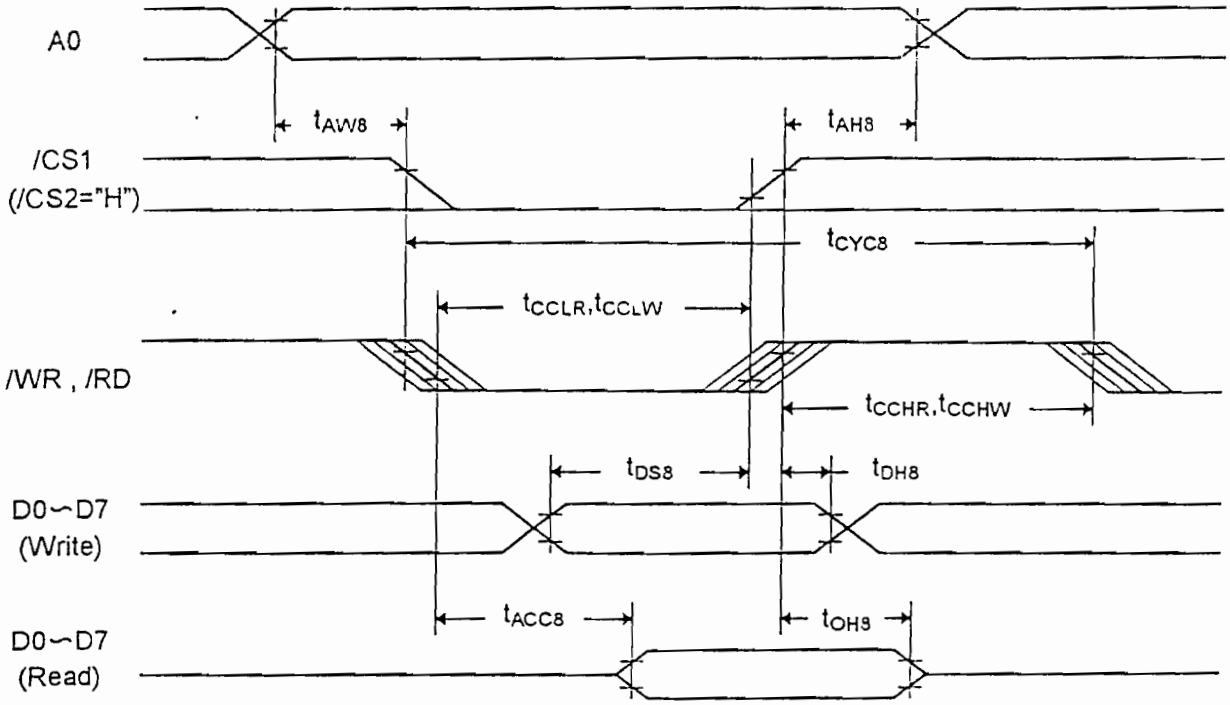
*8 Refer to 26Page <Reference Circuit Examples>.

Operating voltage range of VSS and V5 systems (Power supply for LCD panel is external)



3.2.Timing Characteristics

3.2.1.System Bus Read/Write Characteristics 1 (80**- Series MPU)



V_{DD} = 4.5~5.5V, Top = -20~70°C

Item	Applicable Terminal	Symbol	Condition	Standard Value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		166		ns
Control L pulse width (/WR)	/WR	t_{CCLW}		30	-	ns
Control L pulse width (/RD)	/RD	t_{CCLR}		70	-	ns
Control H pulse width (/WR)	/WR	t_{CCHW}		30	-	ns
Control H pulse width (/RD)	/RD	t_{CCHR}		30	-	ns
Data setup time	D0~D7	t_{DS8}		30	-	ns
Data hold time		t_{DH8}		10	-	ns
/RD access time		t_{ACC8}	C_L=100pF	-	70	ns
Output disable time		t_{OH8}		5	50	ns

V_{DD} = 2.7~4.5V, Top = -20~70°C

Item	Applicable Terminal	Symbol	Condition	Standard Value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		300		ns
Control L pulse width (/WR)	/WR	t_{CCLW}		60	-	ns
Control L pulse width (/RD)	/RD	t_{CCLR}		120	-	ns
Control H pulse width (/WR)	/WR	t_{CCHW}		60	-	ns
Control H pulse width (/RD)	/RD	t_{CCHR}		60	-	ns
Data setup time	D0~D7	t_{DS8}		40	-	ns
Data hold time		t_{DH8}		15	-	ns
/RD access time		t_{ACC8}	C_L=100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

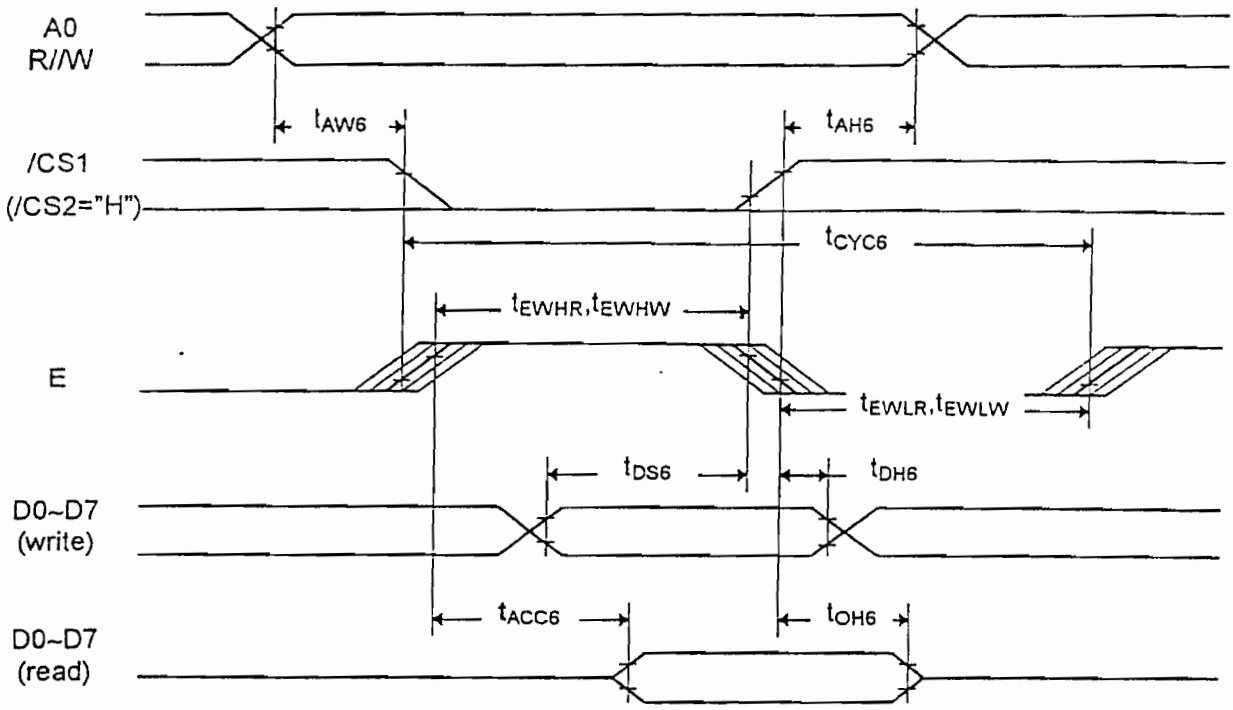
V_{DD} = 1.8~2.7V, Top = -20~70°C

Item	Applicable Terminal	Symbol	Condition	Standard Value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		1000		ns
Control L pulse width (/WR)	/WR	t_{CCLW}		120	-	ns
Control L pulse width (/RD)	/RD	t_{CCLR}		240	-	ns
Control H pulse width (/WR)	/WR	t_{CCHW}		120	-	ns
Control H pulse width (/RD)	/RD	t_{CCHR}		120	-	ns
Data setup time	D0~D7	t_{DS8}		80	-	ns
Data hold time		t_{DH8}		30	-	ns
/RD access time		t_{ACC8}	C_L=100pF	-	280	ns
Output disable time		t_{OH8}		10	200	ns

Notes:

* 1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (t_{CYC8} - t_{CCLW} - t_{CCHW}) for (tr + tf) ≤ (t_{CYC8} - t_{CCLR} - t_{CCHR}) are specified.
* 2 All timing is specified using 20% and 80% of V_{DD} as the reference.
* 3 t_{CCLR} and t_{CCLW} are specified as the overlap between /CS1 being "L" and /WR and /RD being at the "L" level.

3.2.2.System Bus Read/Write Characteristics 2 (6800 Series MPU)



V_{DD} = 4.5~5.5V, T_{OP} = -20~70°C

Item		Signal	Symbol	Condition	Standard Value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	
System cycle time		A0	t_{CYC6}		166	-	
Data setup time		D0~D7	t_{DS6}		30	-	
Data hold time			t_{DH6}		10	-	
Access time			t_{ACC6}	CL=100pF	-	70	
Output disable time			t_{OH6}		10	50	
Enable H pulse time	read	E	t_{EWHR}		70	-	
	write		t_{EWHW}		30	-	
Enable L pulse time	read	E	t_{EWLR}		30	-	
	write		t_{EWLW}		30	-	

V_{DD} = 2.7~4.5V, T_{OP} = -20~70°C

Item		Signal	Symbol	Condition	Standard Value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	
System cycle time		A0	t_{CYC6}		300	-	
Data setup time		D0~D7	t_{DS6}		40	-	
Data hold time			t_{DH6}		15	-	
Access time			t_{ACC6}	CL=100pF	-	140	
Output disable time			t_{OH6}		10	100	
Enable H pulse time	read	E	t_{EWHR}		120	-	
	write		t_{EWHW}		60	-	
Enable L pulse time	read	E	t_{EWLR}		60	-	
	write		t_{EWLW}		60	-	

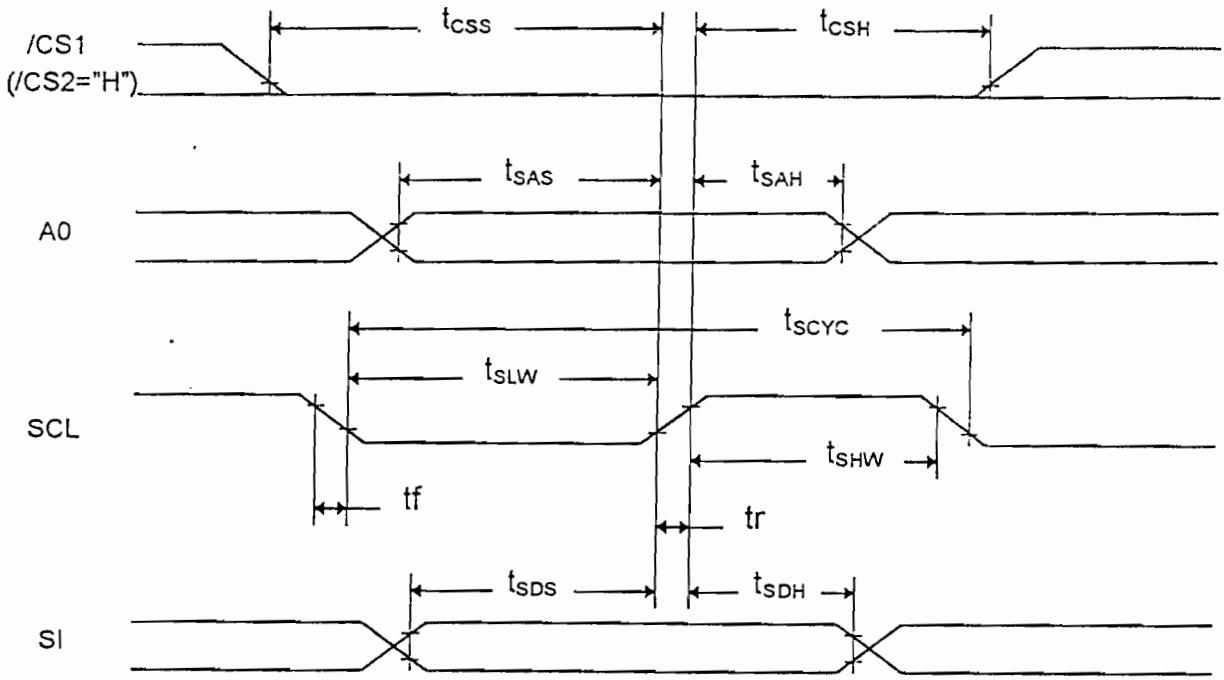
V_{DD} = 1.8~2.7V, T_{OP} = -20~70°C

Item		Signal	Symbol	Condition	Standard Value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	
System cycle time		A0	t_{CYC6}		1000	-	
Data setup time		D0~D7	t_{DS6}		80	-	
Data hold time			t_{DH6}		30	-	
Access time			t_{ACC6}	CL=100pF	-	280	
Output disable time			t_{OH6}		10	200	
Enable H pulse time	read	E	t_{EWHR}		240	-	
	write		t_{EWHW}		120	-	
Enable L pulse time	read	E	t_{EWLR}		120	-	
	write		t_{EWLW}		120	-	

Notes:

* 1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (t_{CYC6} - t_{EWLW} - t_{EWHW}) or (tr + tf) ≤ (t_{CYC6} - t_{EWLR} - t_{EWHR}) are specified.
* 2 All timing is specified using 20% and 80% of V_{DD} as the reference.
* 3 t_{EWLW} and t_{EWLR} are specified as the overlap between /CS1 being "L" and E being at the "L" level.

3.2.3.The Serial Interface



V_{DD} = 4.5~5.5V, T_{OP} = -20~70°C

Item	Applicable Terminal	Symbol	Standard Value		Unit
			Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	200	-	ns
SCL "H" pulse width		t_{SHW}	75	-	
SCL "L" pulse width		t_{SLW}	75	-	
Address setup time	A0	t_{SAS}	50	-	
Address hold time		t_{SAH}	100	-	
Data setup time	SI	t_{SDS}	50	-	
Data hold time		t_{SDH}	50	-	
CS-SCL time	CS	t_{CSS}	100	-	
		t_{CSH}	100	-	

V_{DD} = 2.7~3.6V, T_{OP} = -20~70°C

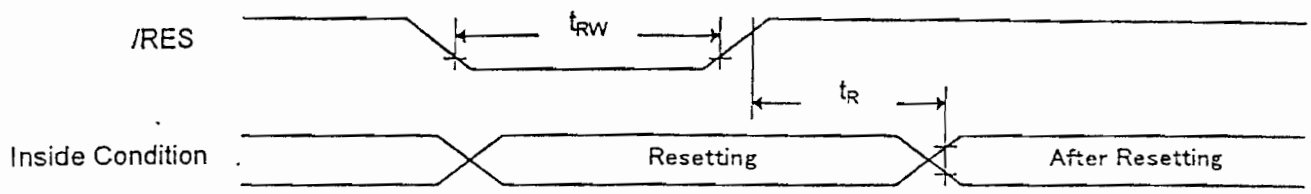
Item	Applicable Terminal	Symbol	Standard Value		Unit
			Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	250	-	ns
SCL "H" pulse width		t_{SHW}	100	-	
SCL "L" pulse width		t_{SLW}	100	-	
Address setup time	A0	t_{SAS}	150	-	
Address hold time		t_{SAH}	150	-	
Data setup time	SI	t_{SDS}	100	-	
Data hold time		t_{SDH}	100	-	
CS-SCL time	CS	t_{CSS}	150	-	
		t_{CSH}	150	-	

V_{DD} = 1.8~2.7V, T_{OP} = -20~70°C

Item	Applicable Terminal	Symbol	Standard Value		Unit
			Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	400	-	ns
SCL "H" pulse width		t_{SHW}	150	-	
SCL "L" pulse width		t_{SLW}	150	-	
Address setup time	A0	t_{SAS}	250	-	
Address hold time		t_{SAH}	250	-	
Data setup time	SI	t_{SDS}	150	-	
Data hold time		t_{SDH}	150	-	
CS-SCL time	CS	t_{CSS}	250	-	
		t_{CSH}	250	-	

Notes:
*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

3.2.4.Reset Timing



Top = -20~70°C

Item	Applicable Terminal	Symbol	Condition	Standard Value		Unit
				Min.	Max.	
Reset time		t_R	V_{DD}4.5V~ 3.6V	-	0.5	µs
Reset "L" pulse width	/RES	t_{RW}		0.5	-	µs
Reset time		t_R	V_{DD}2.7V~ 4.5V	-	1	µs
Reset "L" pulse width	/RES	t_{RW}		1	-	µs
Reset time		t_R	V_{DD}1.8V~ 2.7V	-	1.5	µs
Reset "L" pulse width	/RES	t_{RW}		1.5	-	µs

Note:
*1 All timing is specified using 20% and 80% of V_{DD} as the standard.

4.FUNCTION SPECIFICATIONS

4.1.Description of Functions

4.1.1.Function Specifications

4.1.1.1.Selecting the Interface Type

With the TCM-A1172, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input.

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	-	-	-	SI	SCL	(HZ)

"-" indicates fixed to either "H" or to "L" HZ : High Impedance

4.1.1.2.The Parallel Interface

When the parallel interface has been selected (P/S = "H"), then it is possible to connect directly to either an 80**-Series MPU or a 6800 Series MPU by selecting the C86 terminal to either "H" or to "L".

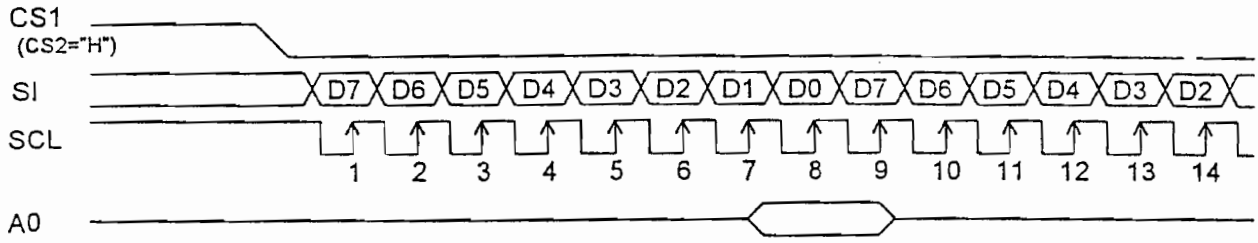
P/S	/CS1	CS2	A0	/RD	/WR	D7~D0
H: 6800 Series MPU Bus	/CS1	CS2	A0	E	R/W	D7~D0
L: 80**-Series MPU Bus	/CS1	CS2	A0	/RD	/WR	D7~D0

Data bus signals are recognized by a combination of A0, /RD(E), /WR(R/W) signals.

Shared	6800 Series	80**-Series		
A0	R/W	/RD	/WR	Function
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

4.1.1.3. The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state (/CS1 = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial interface is structured from an 8-bit shift register and a 3-bit counter; and the serial data is read on the rising edge of the serial clock in the D7, D6, . . . D0 order, being processed in 8-bit units.
The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.



* When the chip is not active, the shift registers and the counter are reset to their initial status.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

4.1.1.4. Accessing the Display Data RAM and the Internal Registers

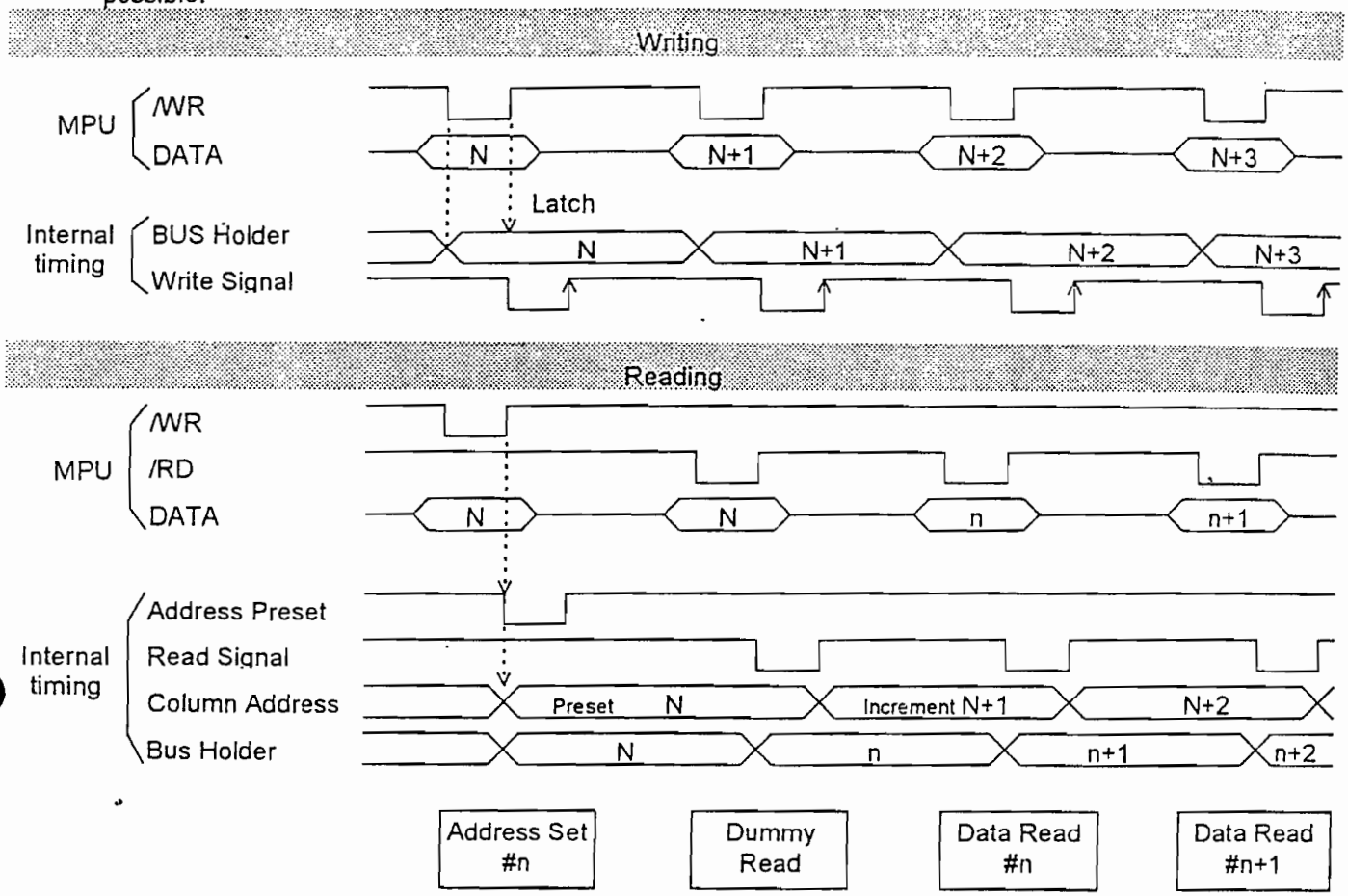
Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the TCM-A1172. Wait time may not be considered.
And in the TCM-A1172, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.

For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

4.1.1.5. The Busy Flag

When the busy flag is "1" it indicates that the TCM-A1172 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is output to D7 terminal with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.



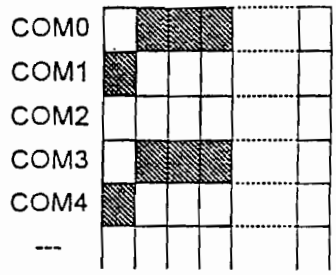
4.1.2.Display Data RAM

4.1.2.1.Display Data RAM

The display data RAM is a RAM that stores the pixel data for the display. It has a 65 (8 page x 8 bit +1) x 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few restriction at the time of display data transfer when multiple TCM-A1172 is used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed synchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

D0	0	1	1	1	.....	
D1	1	0	0	0	.....	
D2	0	0	0	0	.....	
D3	0	1	1	1	.....	
D4	1	0	0	0	.....	
---					.....	

Display data RAM



Liquid crystal display

4.1.2.2.The Page Address Circuit

The page address of the display data RAM is specified through the Page address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

4.1.2.3.The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.
Moreover, the increment of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address again.
Ordinary the ADC command (segment driver direction select command) is used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the restriction on the IC layout when the LCD module is assembled can be minimized.

SEG Output	SEG02		SEG 129
ADC "0"	02(H) →	Column Address	→ 81(H)
(D0) "1"	81(H) ←	Column Address	← 02(H)

4.1.2.4.The Line Address Circuit

The line address circuit, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output when the common output mode is reversed). The display area is a 65 line area from the display start line address in the direction of increasing line addresses.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

4.1.2.5.The Display Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all point ON/OFF command control only the data within the latch, they do not charge the data within the display data RAM itself.

4.1.3.The Oscillator Circuit

TCM-A1172 has an internal oscillator. This is a CR-type oscillator that produces the display clock.

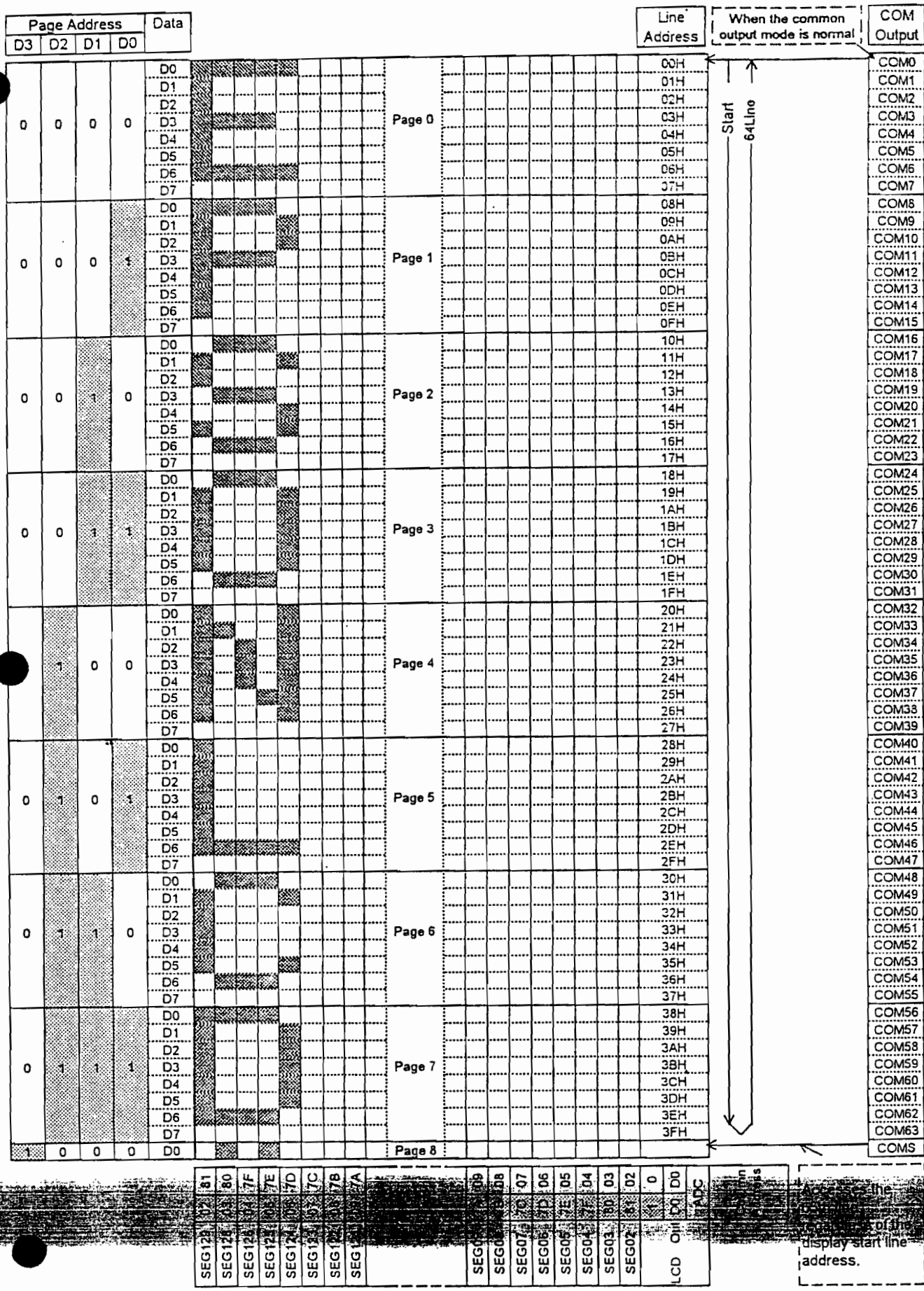
4.1.4.Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed synchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

4.1.5.The Common Output Status Select Circuit

In the TCM-A1172, the COM output scan direction can be selected by the common output status select command. Ordinary "Normal Status" is selected.

Status	COM Scan Direction
Normal	COM0 → COM63
Reverse	COM63 → COM0


Page Address
D3 D2 D1 D0
Data
Line Address
When the common output mode is normal
COM Output
Start
64Line
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
00H 01H 02H 03H 04H 05H 06H 07H
08H 09H 0AH 0BH 0CH 0DH 0EH 0FH
10H 11H 12H 13H 14H 15H 16H 17H
18H 19H 1AH 1BH 1CH 1DH 1EH 1FH
20H 21H 22H 23H 24H 25H 26H 27H
28H 29H 2AH 2BH 2CH 2DH 2EH 2FH
30H 31H 32H 33H 34H 35H 36H 37H
38H 39H 3AH 3BH 3CH 3DH 3EH 3FH
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7
COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15
COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23
COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31
COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39
COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47
COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55
COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63
COMS
SEG128 SEG127 SEG126 SEG125 SEG124 SEG123 SEG122 SEG121
SEG0 SEG01 SEG02 SEG03 SEG04 SEG05 SEG06 SEG07 SEG08 SEG09
LCD Output
ADC
Common Address
Access the contents of the display start line address.

4.1.6.The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise booster circuits, voltage regulator circuits, and voltage follower circuits.
The power supply circuits can turn the booster circuits, the voltage regulator circuits, and the voltage follower circuits ON of OFF independently through the use of the Power Control Set command.

The Control Details of Each Bit of the Power Control Set Command

Item	Status	
	"1"	"0"
D2 : Booster circuit control bit	ON	OFF
D1 : Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 : Voltage follower circuit (V/F circuit) control bit	ON	OFF

<Reference Combinations>

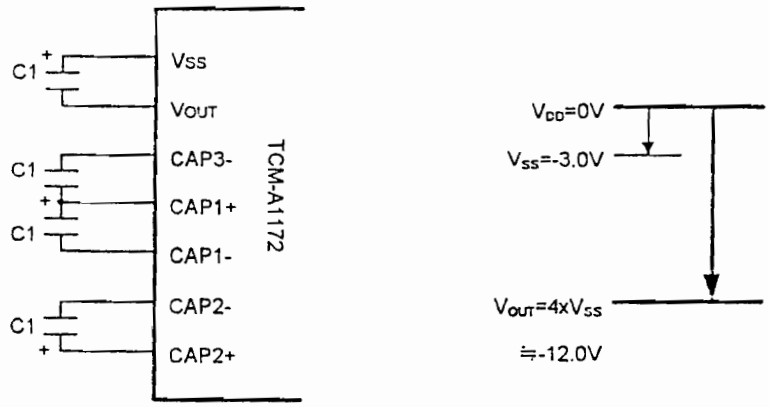
Use Settings	D2	D1	D0	Booster circuit	V regulator circuit	V/F circuit	External voltage input	Booster voltage system terminal
Only the internal power supply is used	1	1	1	O	O	O	V_{SS}	Use

* The "booster system terminals" refer CAP1+, CAP1-, CAP2+, CAP2-, and CAP3-.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

4.1.6.1.The Booster Voltage Circuits

Using the booster voltage circuits equipped within the TCM-A1172 it is possible to product a 4x booster of the VDD – VSS voltage levels.

4x booster: Connect capacitor C1 between CAP1+ and CAP1-, between CAP2+ and CAP2-, between CAP1+ and CAP3-, and between V_{SS} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS}.



* The V_{SS} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

8.3.Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of fluorescent lamps) and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped from our company.
2) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high-humidity environment.

8.4.Design Precautions

1) The absolute maximum ratings represents the rated value beyond which LCD module can not exceed. When the LCD module are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values including taking the precaution of using signal cables that are short.
3) The LCD exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) We recommended that power supply lines (V_{DD}) have overcurrent protection line. (Fuse etc. Recommend Value : 0.5 A)
5) Sufficiently notice the mutual noise interference occurred by peripheral devices.
6) To cope with EMI, take measures basically on outputting side.
7) When installing an LCD module, fasten it at the LCD panel. If the module is fastened to a part other than the LCD panel, various stresses may cause disconnection at the TAB.
8) The display panel is made of general float glass which is not guaranteed for strength. So please consider about following.
   - Do not subject panel to a mechanical shock by dropping directly.
   - Do not let case to touch to panel directly.
9) This LCD module have TCP. TCP structure is more sensitive to the light than flat package structure. Make the IC chip prevent from the light. This module will malfunction, if the IC has no prevention from the light.

8.5.Others

1) Liquid crystal solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD module have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimized the performance degradation of the LCD module's resulting from destruction caused by static electricity, etc. Exercise care to avoid touching the following sections when handling this module.
   ① LCD's Terminal electrode sections.
   ② Part of TAB
4) Optimum voltage to obtain best contrast value depending on products.
   Therefore voltage adjustment with electric volume is required in each display.
5) Precaution for disposal of LCD module.
   When disposal of LCD module, ask specialization company of industrial waste which is permitted by the government.
   When burn up LCD module, obey the law of environmental hygienics.

4.1.6.2. The Voltage Regulator Circuit

The booster voltage generated at V_{OUT} outputs the liquid crystal driver voltage V5 through the voltage regulator circuit.
Because the TCM-A1172 has an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.
The V_{REG} thermal gradients of the TCM-A1172 is approximately -0.05%/°C.

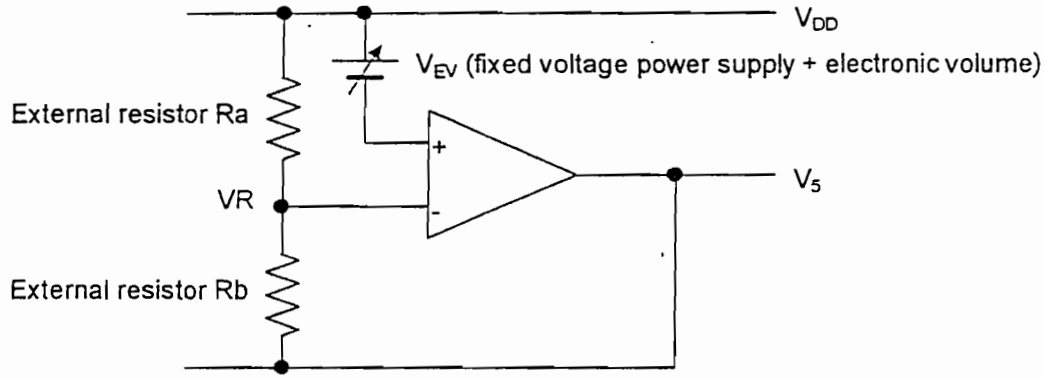
<When an External Resistance is Used>
(The V5 Voltage Regulator Internal Resistors Are Not Used)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra and Rb between V_{DD} and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands.
In the range where $|V5| < |V_{OUT}|$, the V5 voltage can be calculated using equation A-1 based on the external resistances Ra and Rb.

$$V5 = \left(1+\frac{Rb}{Ra}\right) \times VEV$$

$$= \left(1+\frac{Rb}{Ra}\right) \times \left(1-\frac{\alpha}{162}\right) \times VREG \qquad \text{(Equation A-1)}$$

$$\left[VEV = \left(1-\frac{\alpha}{162}\right) \times VREG\right]$$



4.1.6.3.The Liquid Crystal Voltage Generator Circuit

The V5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit. The bias ratio can be selected by the LCD bias set command to 1/9 bias or 1/7 bias. The default status is 1/9 bias.

4.1.6.4.High Power Mode

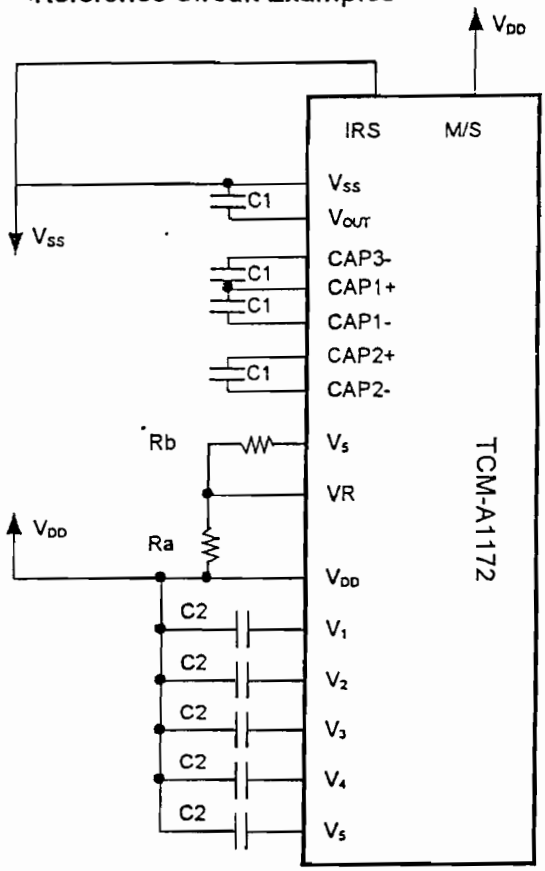
The TCM-A1172 has two level internal power supply circuit (Normal mode and High power mode). The TCM-A1172 is evaluation model, it runs normally "Normal mode". When LCD size is bigger than this model, normal mode may cause display quality to degrade. Please compare normal mode power consumption with high power mode.

4.1.6.5.The Internal Power Supply Shutdown Command Sequence

The sequence is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	Command address D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (Compound)
	↓									
Step2	Display all points ON	1	0	1	0	0	1	0	1	
	↓									
End	Internal power supply OFF									

<Reference Circuit Examples>



When the internal power supply and the V5 voltage regulator internal resistors are not used.
(Example with 4x step-up voltage)

Examples of shared reference settings

When V5 can vary between -11.7 and -7.1V

Item	Set value	Units
C1	4.7(B class)	μ F
C2	1.0(B class)	μ F
Ra	180(±0.5%)	k Ω
Rb	820(±0.5%)	k Ω

* 1 Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2 The TCM-A1172 is evaluation model. This LCD module's setting is C1 = 1.0μF and C2 = 0.1μF. When the custom LCD module size is bigger than this model, C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

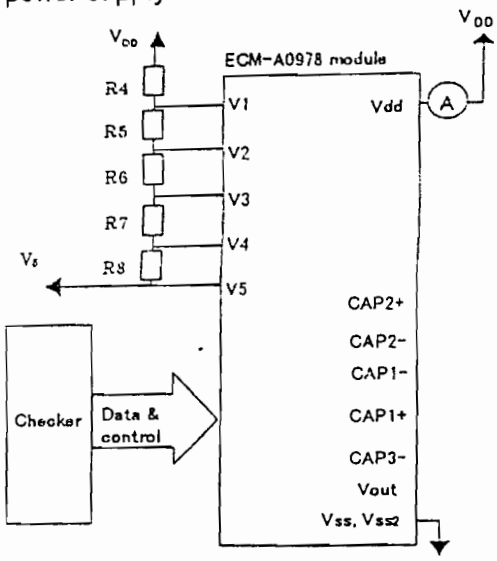
<Example of the process by which to determine the settings>

Step1 Turn the voltage regulator circuit and voltage follower circuit on. Supply a voltage to V_{OUT} from external power supply.

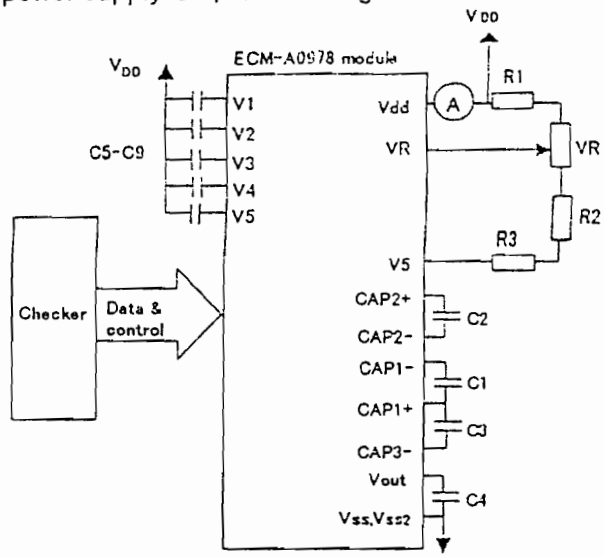
Step2 Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the LCD drive voltages (V1 to V5). Note that all capacitor must have the same capacitance value.

Step3 Turn all the internal power supplies on. Determine C1.

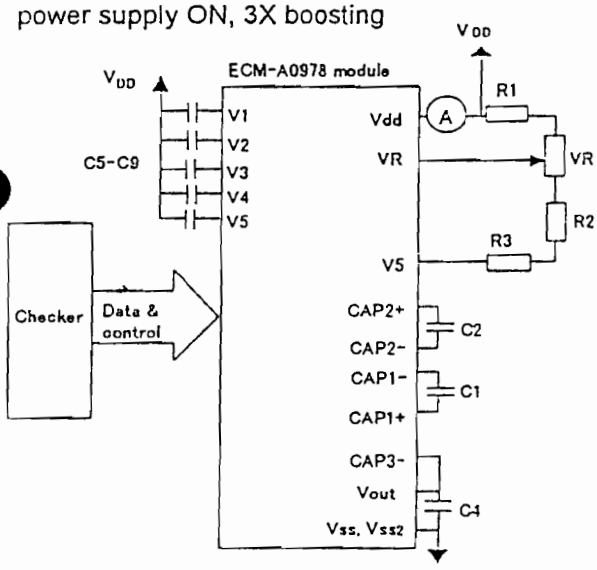
Measurement circuit for internal power supply OFF



Measurement circuit for internal power supply ON, 4X boosting.



Measurement circuit for internal power supply ON, 3X boosting



Parts setting:

R1 = 390Ω, R2 = R3 = 1MΩ, VR = 200kΩ
C1 = C2 = C3 = C4 = 4.7μF
C5 = C6 = C7 = C8 = C9 = 1μF
R4 = R5 = R7 = R8 = 10kΩ, R6 = 30kΩ (for internal
power supply OFF only),
V_{DD}- V_5 = 8.5V

4.1.7.The Reset Circuit

When the /RES input falls to "L", TCM-A1172 reenters their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = "L")
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias ratio: 1/9 bias
7. Display all points OFF
8. Power saving clear
9. V5 voltage regulator internal resistors Ra, Rb Cut Off
   (The internal resistors are connected to between V_{DD} and V_5 through /RES="L".)
10. SEG outputs are non-selective potentials V_2 and V_3
    COM outputs are non-selective potentials V_1 and V_4
    (SEG and COM outputs are V_{DD} level through /RES="L".)
11. Read modify write OFF
12. Static indicator OFF
    Static indicator resistor: (D2,D1)=(0,0)
13. Display start line set to first line
14. Column address set to Address 0
15. Page address set to Page 0
16. Common output status normal
17. V_5 voltage regulator internal power supply ratio set mode clear
18. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
19. Test mode clear

On the other hand, when the reset command is used only default settings 11 to 19 above are put into effect.
The /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal.
Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition to the IC. After applying a current, it is necessary to take measures to prevent the input terminal from entering a high impedance state.
In the TCM-A1172, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply a "L" signal to the /RES terminal when the external liquid crystal power supply is applied.
Even though the oscillator circuit operates while the /RES terminal is "L," the display timing generator circuit is stopped and CL terminal status is "H". There is no influence on the D0 to D7 terminals.

4.2.Commands

TCM-A1172 identify the data bus signals by a combination of A0, /RD(E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 80**-Series MPU interface, commands are launched by inputting a low pulse to the /RD terminal for reading, and inputting a low pulse to the /WR terminal for writing.
In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. (See "3.2. Timing Characteristics" regarding the timing.) Consequently, the 6800 Series MPU interface is different than the 80**-Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD(E) becomes "1(H)". In the explanations of section 4.2.3. Description of Command, the commands are explained using the 80**-Series MPU interface as the example.

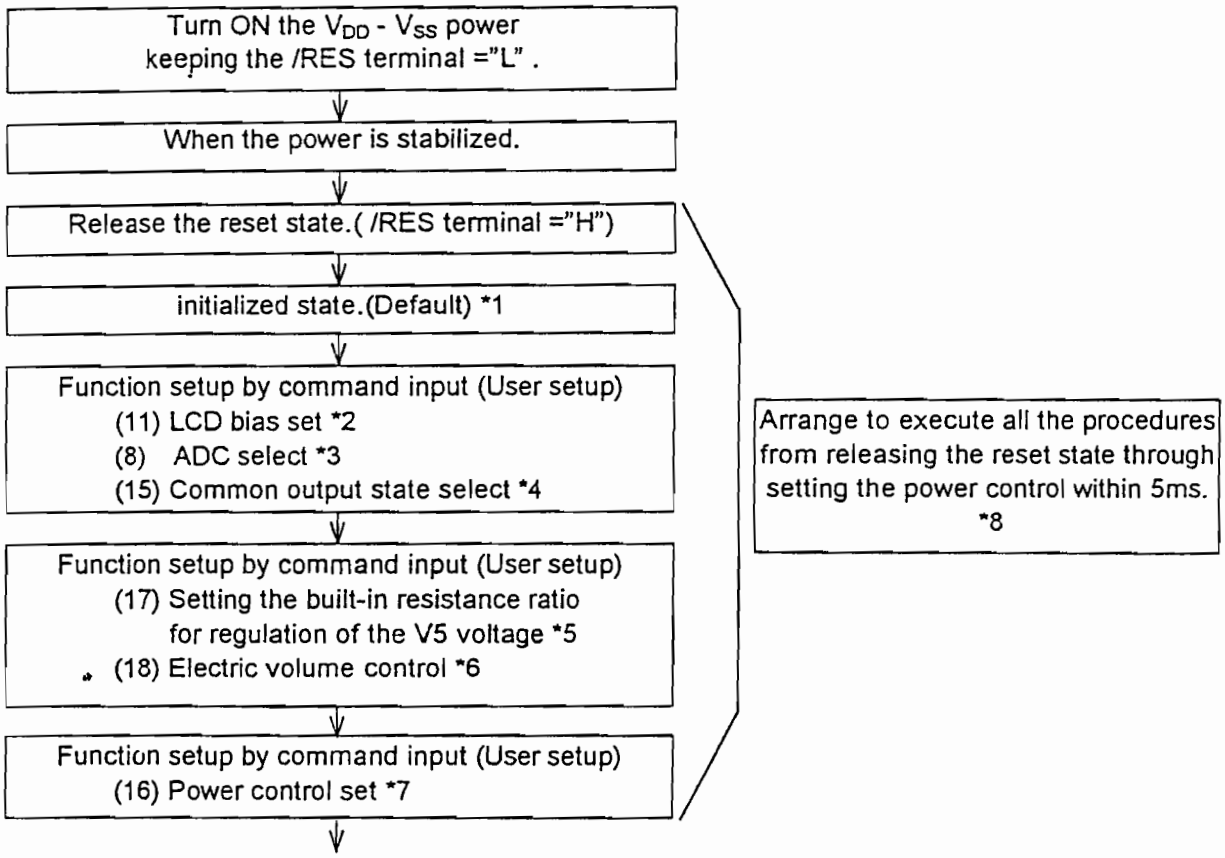
When the serial interface is selected, the data is input in sequence starting with D7.

4.2.1.Command Instruction

4.2.1.1.Initialization(Reference)

Note : When the power is applied, LCD driving non-selective potentials V2 and V3 (SEG) and V1 and V4 (COM) are output through the LCD driving output SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving output terminals (V1 ~ V5) and VDD terminal, the picture on the display may become totally dark instantaneously and other failures when the power is turn on .To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

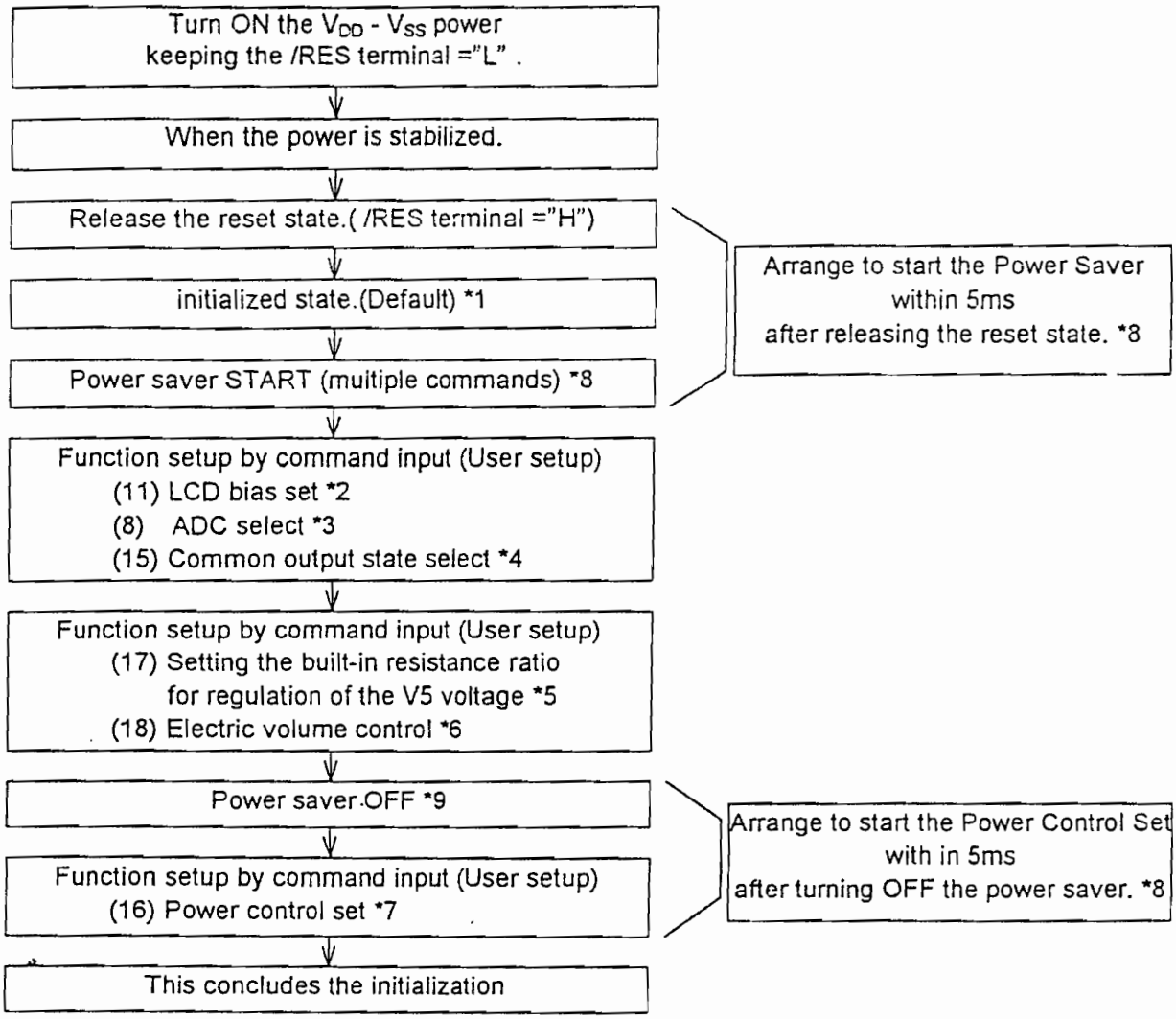
① When the built-in power is being immediately after turning on the power:



Notes : References

*1 4.1.7. The Reset Circuit
*2 4.2.3.11. LCD bias set
*3 4.2.3.8. ADC select
*4 4.2.3.15. Common output mode select
*5 4.1.6.The Power Supply Circuits, 4.2.3.17. V5 voltage regulator internal resistor ratio set
*6 4.1.6. The Power Supply Circuits, 4.2.3.18. Electronic volume
*7 4.1.6. The Power Supply Circuits, 4.2.3.16. Power control set
*8 The target time of 5ms will result to vary depending on the capacitance of smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

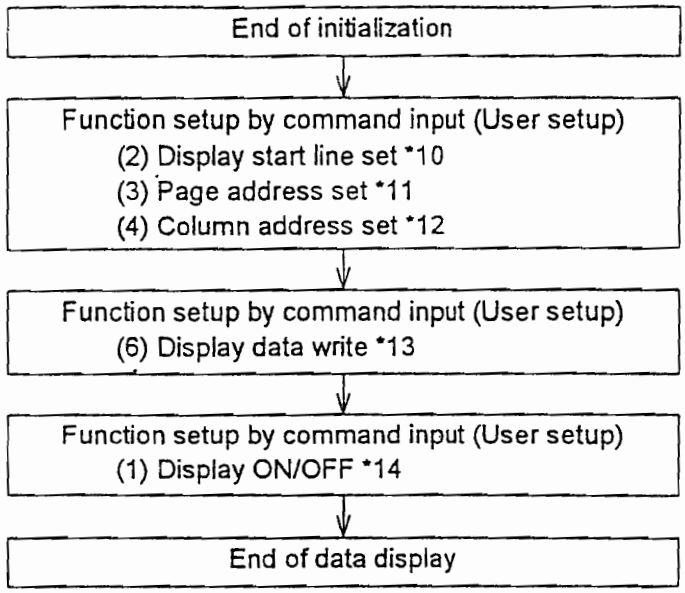
② When the built-in power is not being used immediately after turning on the power:



Notes : References

*1: 4.1.7 The Reset Circuit
*2: 4.2.3.11 LCD bias set
*3: 4.2.3.8. ADC select
*4: 4.2.3.15. Common output mode select
*5: 4.1.6.The Power Supply Circuits, 4.2.3.17. V5 voltage regulator internal resistor ratio set
*6: 4.1.6.The Power Supply Circuits, 4.2.3.18. Electronic volume
*7: 4.1.6.The Power Supply Circuits, 4.2.3.16. Power control set
*8: The target time of 5ms will result to vary depending on the capacitance of smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.
*9: 4.2.3.20. Power Saver : The Power Saver ON state can either be in "Sleep" or "Stand-by" state.

4.2.1.2.Data Display

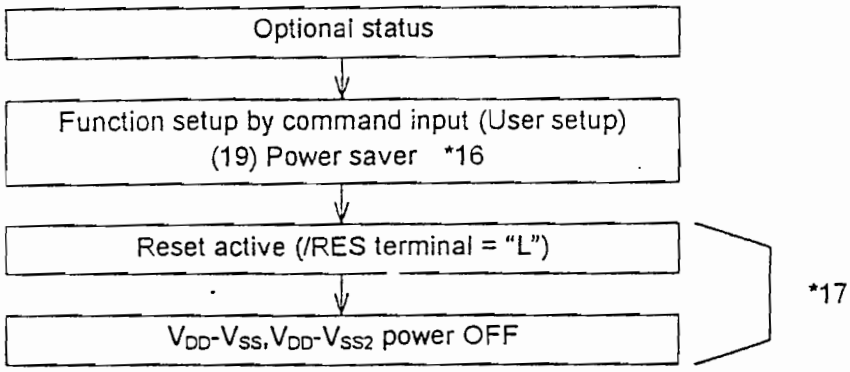


Notes : References

*10: 4.2.3.2. Display start line set
*11: 4.2.3.3. Page address set
*12: 4.2.3.4. Column address set
*13: 4.2.3.6. Display data write
*14: 4.2.3.1. Display ON/OFF

Avoid displaying all the data at the data display start (when the display is ON) in white.

4.2.1.3.Power OFF *15



Notes : References

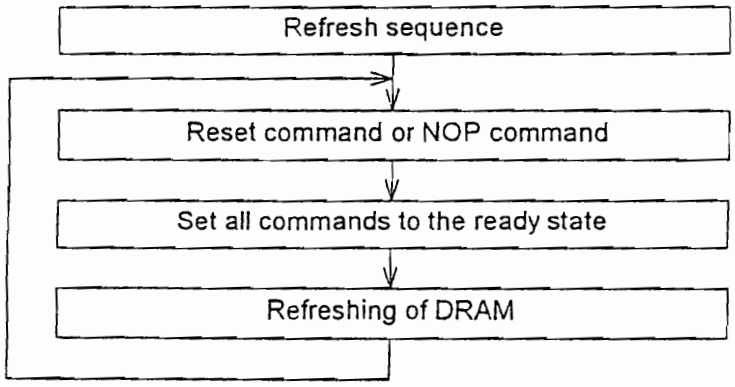
*15: After turning the internal power supply OFF, turn the power supply of the IC OFF.(4.1.6.The Power Supply Circuits)
When turning the power supply of the IC OFF with the internal power supply is held in the ON status, since the status where the voltage is supplied, even though an only little, to the internal LCD drive circuit is still continued, it is feared to ill affect display of the LCD panel. To avoid this be sure to observe the power OFF sequence strictly.

*16: Do not input the /RES to "L" between inputting power saver command and turning the power supply (V_{DD}-V_{SS}) off.
4.2.3.20. Command Table (20) Power saver

*17: "tL" must be set longer than "tH".
tL : The time between power save command ON and the logical power supply OFF.
tH : The period that the internal LCD's multi-level (V5 to V1) status is less than LCD's Vth level.

4.2.1.4.Refresh

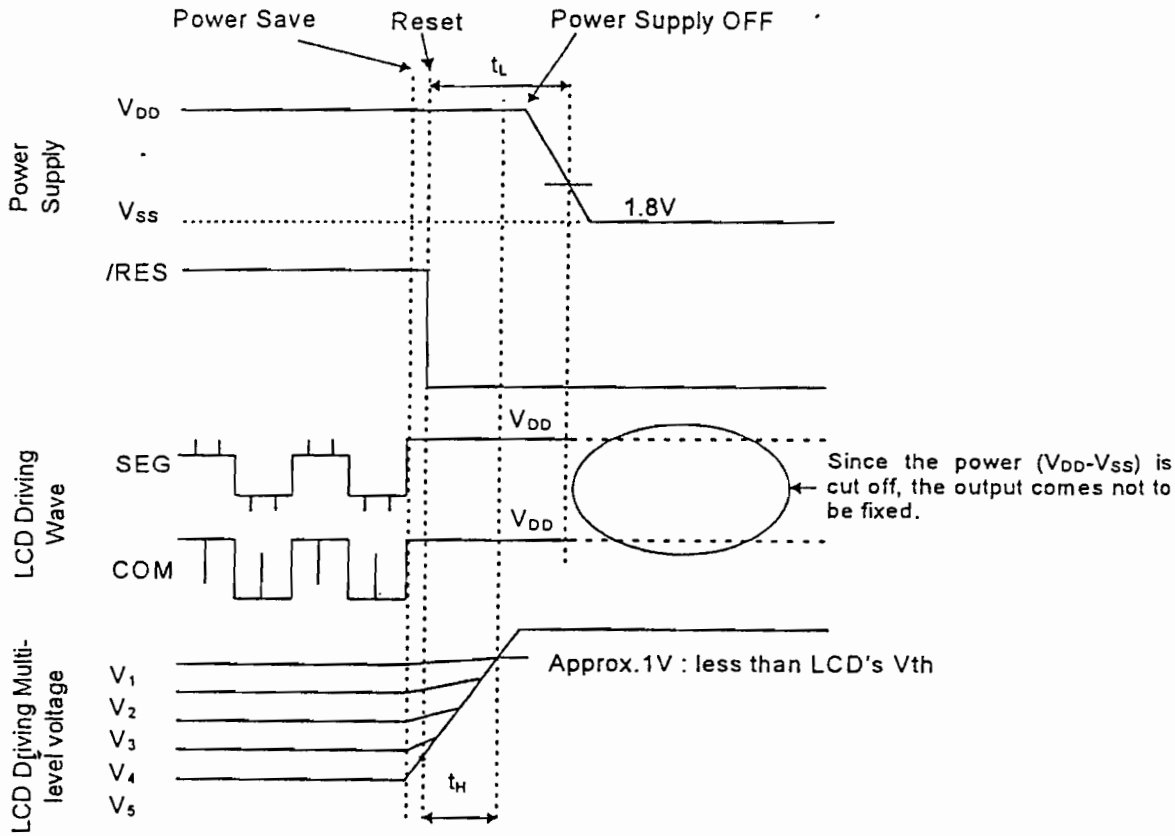
It is recommended to turn on the refresh sequence regularly at a specified interval.



4.2.1.5.Precautions on Turning off the power

<Turning the power (V_{DD}-V_{SS}) off>

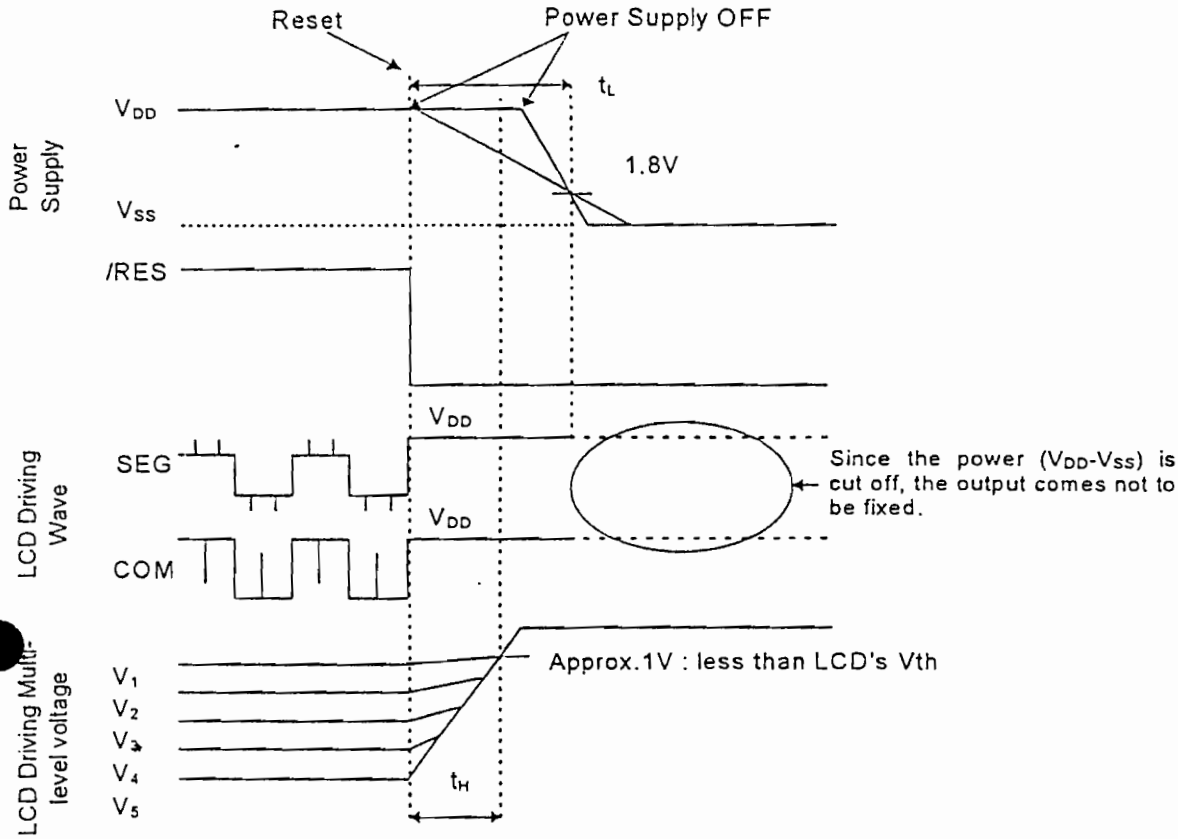
1) Power Save (The LCD powers (V_{DD}-V_5) are off.) → Reset input → Power (V_{DD}-V_{SS}) OFF
   - Observe $t_L > t_H$
   - When $t_L < t_H$, an irregular display may occur.
     Set t_L on the MPU according to the software. t_H is determined according to the external capacity C2 (smoothing capacity of $V_5 \sim V_1$) and the driver's discharging capacity.



Note : For t_H, see next page figure

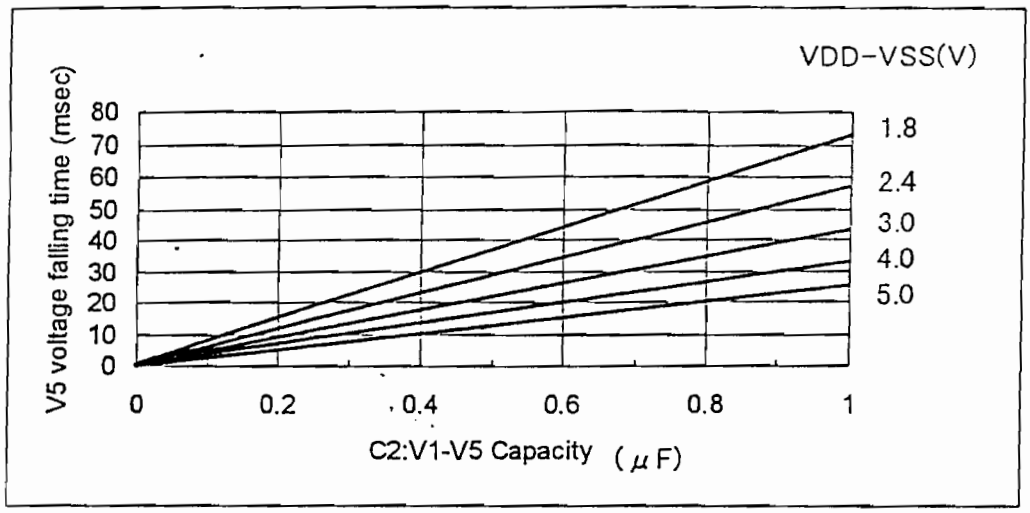
<Turning the power (V_{DD}-V_{SS}) off : When command control is not possible>

2) Reset (The LCD powers (V_{DD}-V_5) are off.) → Power (V_{DD}-V_{SS}) OFF
   - Observe $t_L > t_H$
   - When $t_L < t_H$, an irregular display may occur.
     For t_L, make the power (V_{DD}-V_{SS}) falling characteristics longer or consider any other method. t_H is determined according to the external capacity C2 (smoothing capacity of V_5 to V_1) and the driver's discharging capacity.



Note : For t_H, see the following figure.

<Reference Data>
V5 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.
V5 voltage falling (discharge) time (t_H) after the process of operation → reset.



4.2.2.Command Table

Command	Command Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9, 1: 1/7
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V5 output voltage electronic volume register
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20) Power saver												Display OFF and display all points ON compound command
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) * : disable data

4.2.3.Description of Commands

4.2.3.1.Display ON/OFF

This command turns the display ON and OFF.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

4.2.3.2.Display Start Line Set

This command is used to specify the display start line address of the display data RAM. For further details see the explanation of this function in Section 4.1.2.4, "The Line Address Circuit" .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
								↓			↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

4.2.3.3.Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM Specifying the page address and column address enable to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the explanation of this function in Section 4.1.2.2, "The Page Address Circuit" for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

4.2.3.4.Column Address Set

This command specifies the column address of the display data RAM. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. See the function explanation in Section 4.1.2.3, "The Column Address Circuit," for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
High bits→	0	1	0	0	0	0	1	A7	A6	A5	A4
Low bits→							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

4.2.3.5.Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

4.2.3.6.Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

4.2.3.7.Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the MPU can continuously read multiple-word data.
One dummy read is required immediately after the column address has been set. See the function explanation in Section 4.1.1.4, "Accessing the Data RAM and the Internal Registers" for details.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

4.2.3.8.ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output signals may be reversed by this command. See the explanation of the function in Section 4.1.2.3, "Column Address Circuit" for details. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Rotate right (normal)
										1	Rotate left (reverse)

4.2.3.9.Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

4.2.3.10.Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode.

4.2.3.11. LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

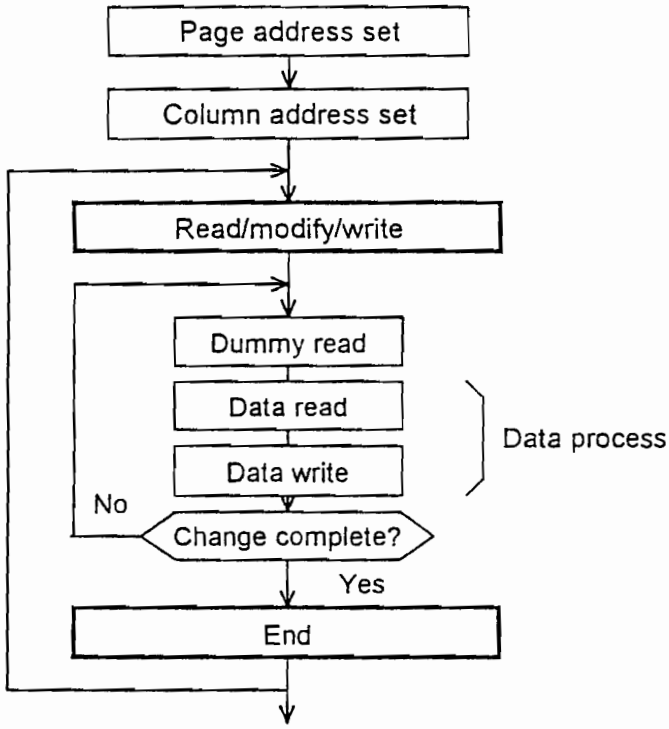
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

4.2.3.12.Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blinking cursor.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

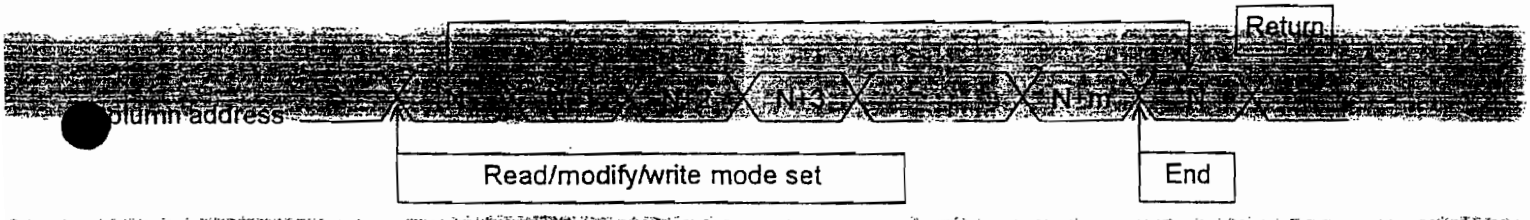
* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.
- The sequence for cursor display



4.2.3.13.End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



4.2.3.14.Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in Section 4.1.7, "Reset" for details.
The reset operation is performed after the reset command is entered.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

4.2.3.15.Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in Section 4.1.5, "The Common Output Status Select Circuit."

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	1	1	0	0	0	*	*	*	Normal: COM0 → COM63
							1				Reverse: COM63 → COM0

* Disabled bit

4.2.3.16.Power Controller Set

This command sets the power supply circuit functions. See the function explanation in Section 4.1.6, "The Power Supply Circuits," for details.

	E	R/W									
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Step-up circuit: OFF
								1			Step-up circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

4.2.3.17.V5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V5 voltage regulator internal resistor ratio.

	E	R/W									
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
								1	1	1	Large

4.2.3.18.The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply.
This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

< The Electronic Volume Mode Set >
When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

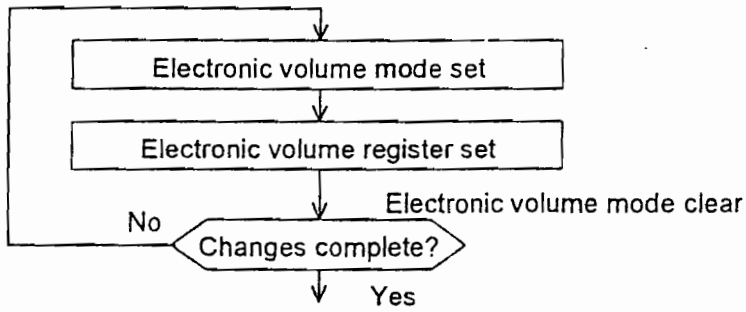
< Electronic Volume Register Set >
By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	|V5|	α
0	1	0	*	*	0	0	0	0	0	1	Small	63
0	1	0	*	*	0	0	0	0	1	0		62
0	1	0	*	*	0	0	0	0	1	1		61
↓							↓				↓	↓
0	1	0	*	*	1	1	1	1	1	0		1
0	1	0	*	*	1	1	1	1	1	1	Large	0

* Disabled bit

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

< The Electronic Volume Register Set Sequence >



4.2.3.19.Static Indicator (Double Byte Command)

This command is used by Power Save command.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one **must** execute one after the other. (The static indicator OFF command is a single byte command.)

<Static Indicator ON/OFF>
When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

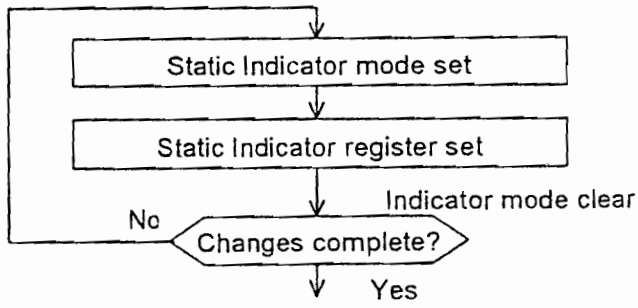
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

<Static Indicator Register Set>
This command sets two bits of data into the static indicator register.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON
									1	0	ON
									1	1	ON

* Disabled bit

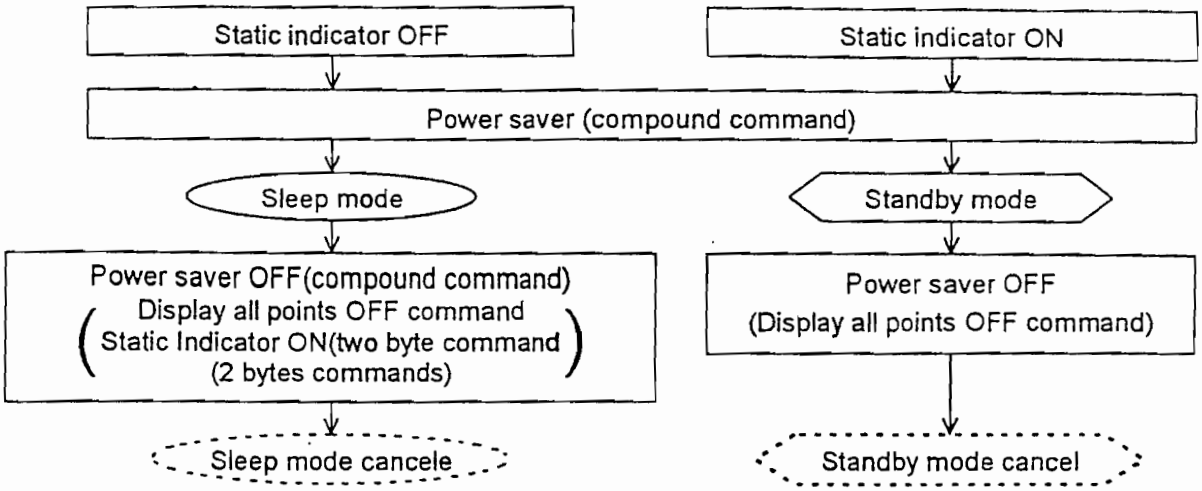
<Static Indicator Register Set Sequence>



Note: The TCM-A1172 has no "Static Indicator".

4.2.3.20.Power Saver (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
The power saver mode is cleared by the display all points OFF command.



<Sleep Mode>
This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

① The oscillator circuit and the LCD power supply circuit are halted.
② All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

<Standby Mode>
The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.
② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

(Note) : When turning on the TCM-A1172, the internal oscillator is running. Only "Sleep Mode" can stop this oscillating circuit.

4.2.3.21.NOP

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

4.2.3.22.Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the /RES input by the reset command or by using an NOP.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

(Note): TCM-A1172 maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the TCM-A1172. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

5.OPTICAL CHARACTERISTICS

5.1.Optical Characteristics

5.1.1.TCM-A1172

Item	Symbol	Temp (°C)	Standard Value			Unit	Condition *3
			Min.	Typ.	Max.		
Driving Voltage	Vop *1	-20	8.4	8.9	9.4	V	
		25	8.0	8.5	9.0		
		70	7.7	8.2	8.7		
Response Time	tr	-20	-	3500	5300	ms	Refer to 5.2.3
		25	-	90	140		
	tf	-20	-	8900	13400		
		25	-	350	530		
Contrast Ratio	K	25	3.5	6.5	-		*2

*1 Vop = LCD Driving Voltage getting maximum contrast = VDD-V5
(Due to the manufacturing variations, each LCD module have its own unique value which is within the specified range. LCD driving voltage should be adjusted by each LCD module.)

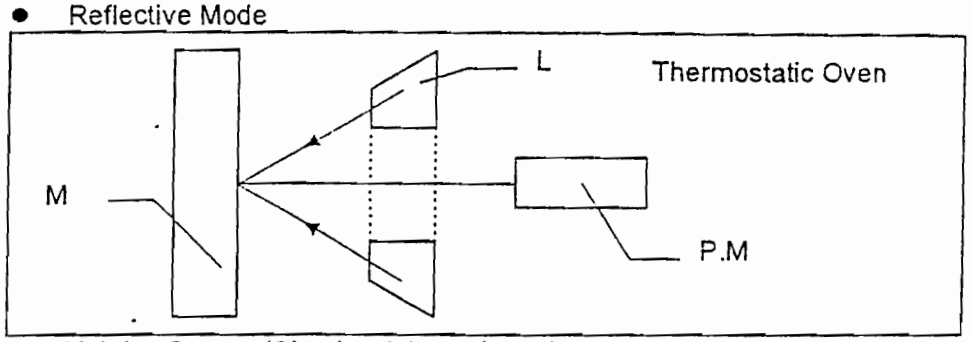
*2 Viewing Angle : (θX1,2 , θY1,2) = 0°

*3 The LCD driving condition is 1/7 Bias.

5.2.Definition of Optical Characteristics

5.2.1.Optical Measuring Equipment

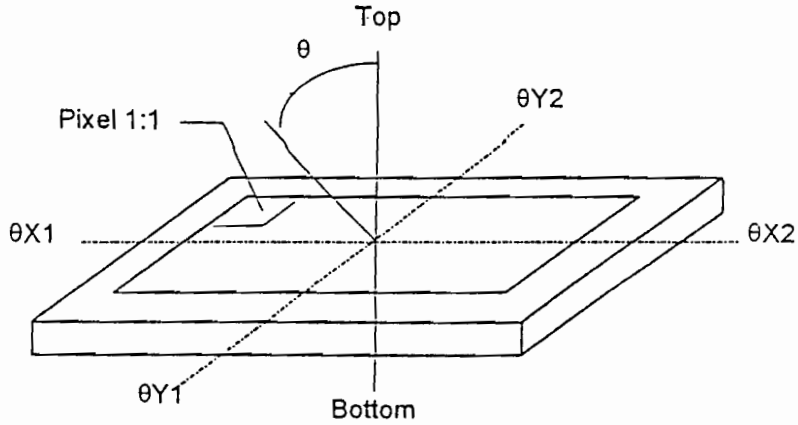
- Reflective Mode



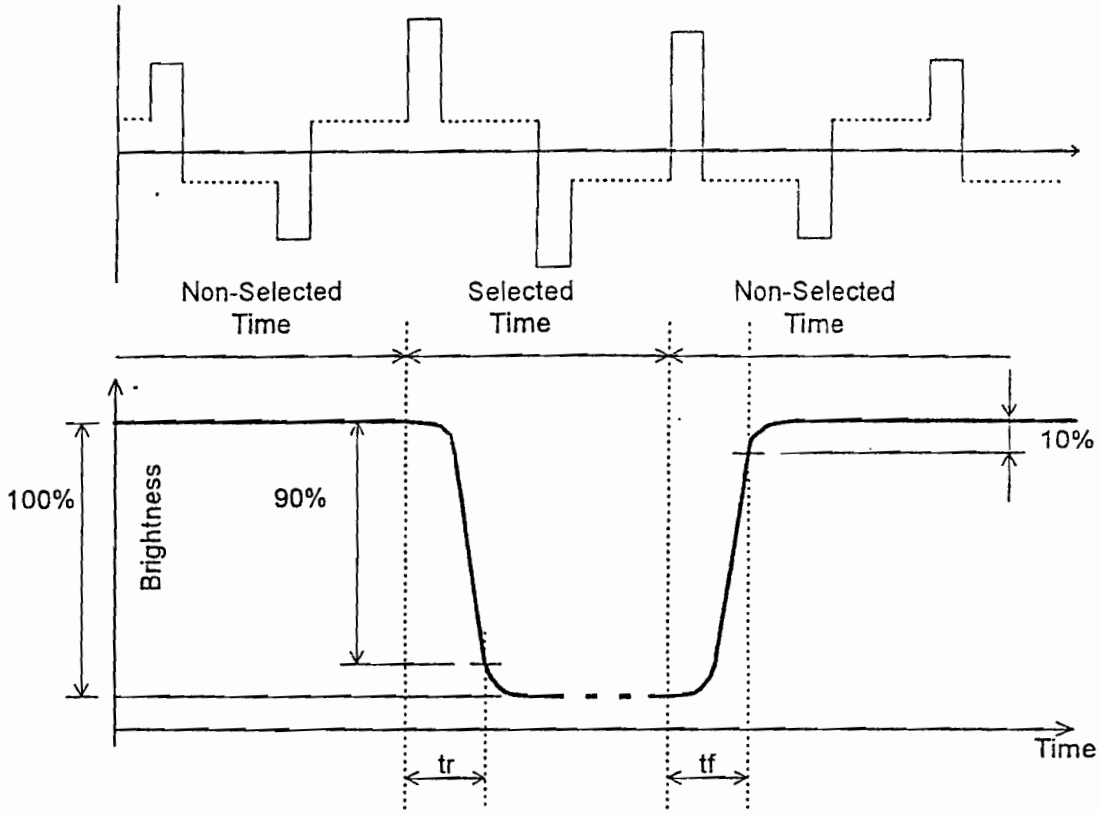
L : Lighting Source (Circular Halogen Lamp)
P.M : Lighting Sensor
M : Module
[Specification of Equipment and Measuring Condition]

- Luxmeter : Canon LC-3S
- Brightness Measurement Spot Diameter: ϕ2mm
- Measuring Point : Pixels

5.2.2.Definition of Viewing Angle



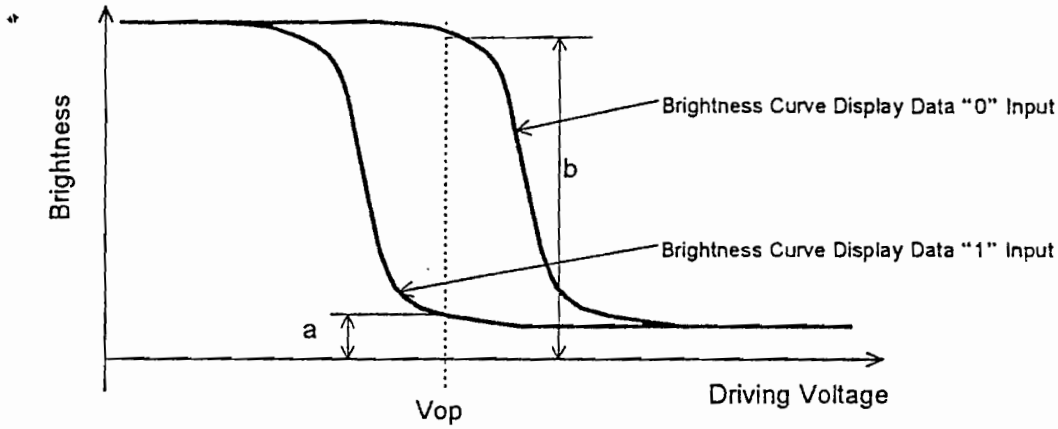
5.2.3.Definition of Response Time



[Measuring Condition]

- Vop = Typ. Value at Operating Temperature
- θX = θY = 0°

5.2.4.Definition of Contrast Ratio



$$\text{Contrast Ratio} = \frac{\text{Brightness Curve Display Data "0" Input : b}}{\text{Brightness Curve Display Data "1" Input : a}}$$

[Measuring Condition]

- Vop = Typ. value at 25°C
- θX = θY = 0°

6.RELIABILITY TEST

6.1.Content of Reliability Test

	No	Test Item	Content of Test	Test Condition
Environmental Test	1	High Temperature Storage	Endurance test of high temperature for a long time.	70°C 200 H
	2	Low Temperature storage	Endurance test of low temperature for a long time.	-20°C *1 200 H
	3	High temperature Operation	Endurance test of electrical stress (Voltage & Current) and the thermal stress to the element.	70°C *2 200 H
	4	High Temperature/ Humidity Storage	Endurance test of high temperature and high humidity for a long time.	50°C 90 %RH 200 H *1
	5	High Temperature/ Humidity operation	Endurance Test of electrical stress (Voltage & Current) and high temperature and high humidity for a long time.	40°C *1 *2 90 %RH 200 H
	6	Thermal Shock	Endurance test of low and high temperature cycles. (air to air) -20°C ⟷ 25°C⟷ 70°C⟷ 25°C (30min)(within 10sec)(30min)(within 10sec) ⟷ 1cycle ⟷	-20°C / 70°C 10 cycle
Mechanical Test	7	Vibration (Package state)	Endurance test applying the vibration during transportation.	10~55 Hz 1.5mmp-pmax. 2.0Gmax X,Y,Z direction Total 2.0H
	8	Shock (Package state)	Endurance test applying the shock during transportation.	Drop the packing box from 80 cm height onto solid. 1 corner/ 3 ridges/6 surfaces 1 time per each direction

*1 Not to dewy
*2 Driving condition for operating test.
Power Supply Voltage for Logic System (V_{DD}) = 3.0V

6.2.Failure Judgment Criterion

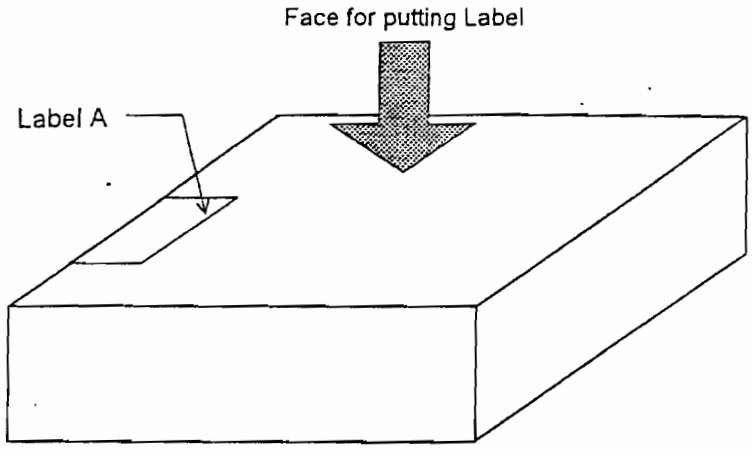
After the above-mentioned test.
(For Environmental Test, after 2 hours in room temperature.)

1) There should not exist conspicuous failure of display quality and appearance.
2) Contrast ratio should be 50% of the initial contrast ratio.
3) There should not have any abnormality of functions.

7.PACKAGE SPECIFICATIONS

7.1.Inner Carton Box

Each LCD module is placed on the antistatic tray, and put into the inner carton box for containing 132 pcs of LCD module.



Model	TCM-A1172
Q'ty	132 pcs.
Lot	Lot No.
EPSON SEIKO EPSON CORP LIQUID CRYSTAL DISPLAY DIVISION	

Detail of label A

7.2.Master Carton Box

The master carton box is for sending to each user.
The master carton box contains 2 pcs of inner carton box.
The indications are applied to four faces A, B, C and D of the master carton box as shown Fig.1 below.

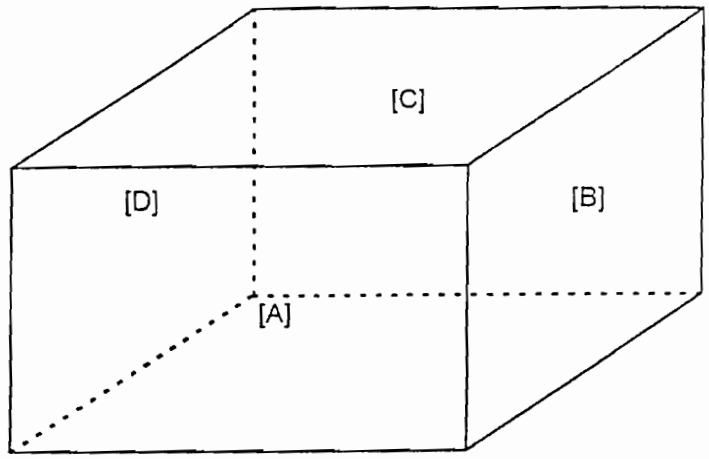
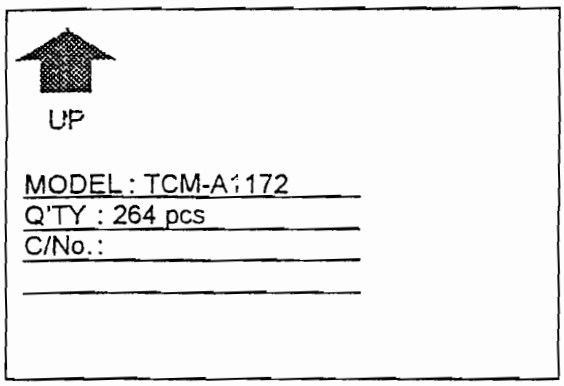
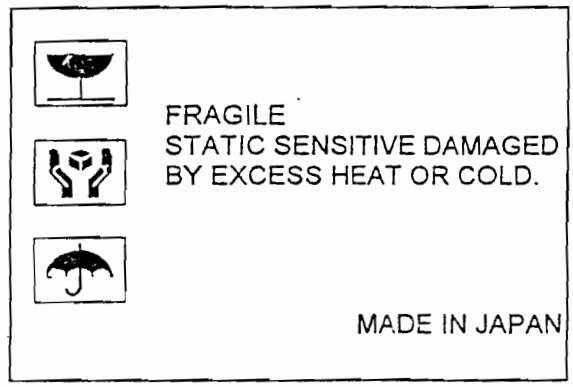


Fig.1 Outline of Master Carton Box.

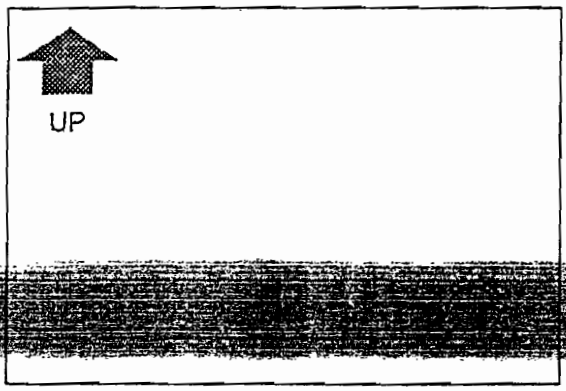
Face A



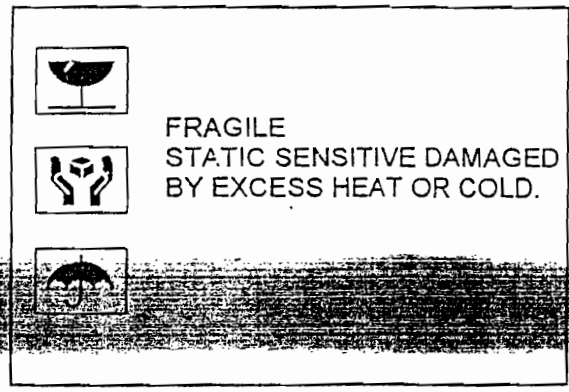
Face B

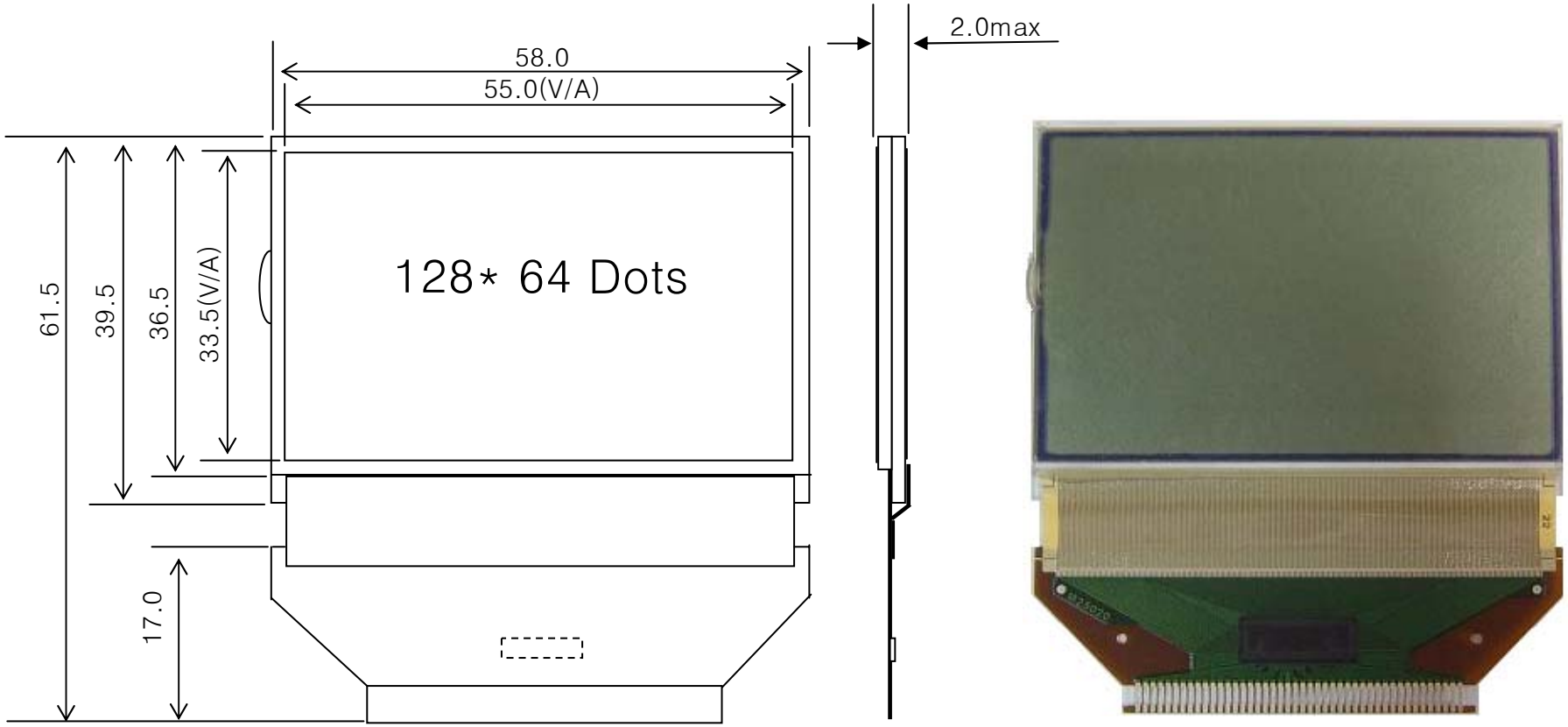


Face C



Face D




58.0
55.0(V/A)
2.0max
128* 64 Dots
61.5
39.5
36.5
33.5(V/A)
17.0