"C²MOS" DIGITAL INTEGRATED CIRCUIT

TCP4600AC

SILICON MONOLITHIC

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

GENERAL DESCRIPTION

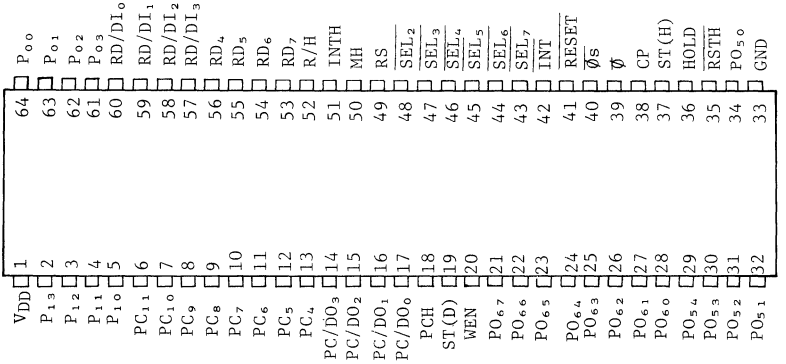
TCP4600AC is a system development evaluator of TLCS-46A family, and makes it possible to configure a system equal to TCP4620AP/TCP4630AP by program memory (ROM) and the external circuits relative to mask options.

Since this technical data mainly makes mention of the function of an evaluator of TCP4600AC, it is recommended that instruction and detail be referred to the technical data of TCP4620AP/TCP4630AP.

FEATURES

- o External ROM 4K x 8 Max.
- o Internal RAM 160 x 4
- o Single 5V Supply
  Wide Operating Range: 4V to 6V
- o Wide Operating Temperature Range: -10°C to 70°C
- o Terminals for System Debugging
- ° External-Circuit Terminal for Realization of all the Mask Option of TLCS-46A

PIN CONNECTIONS (TOP VIEW)

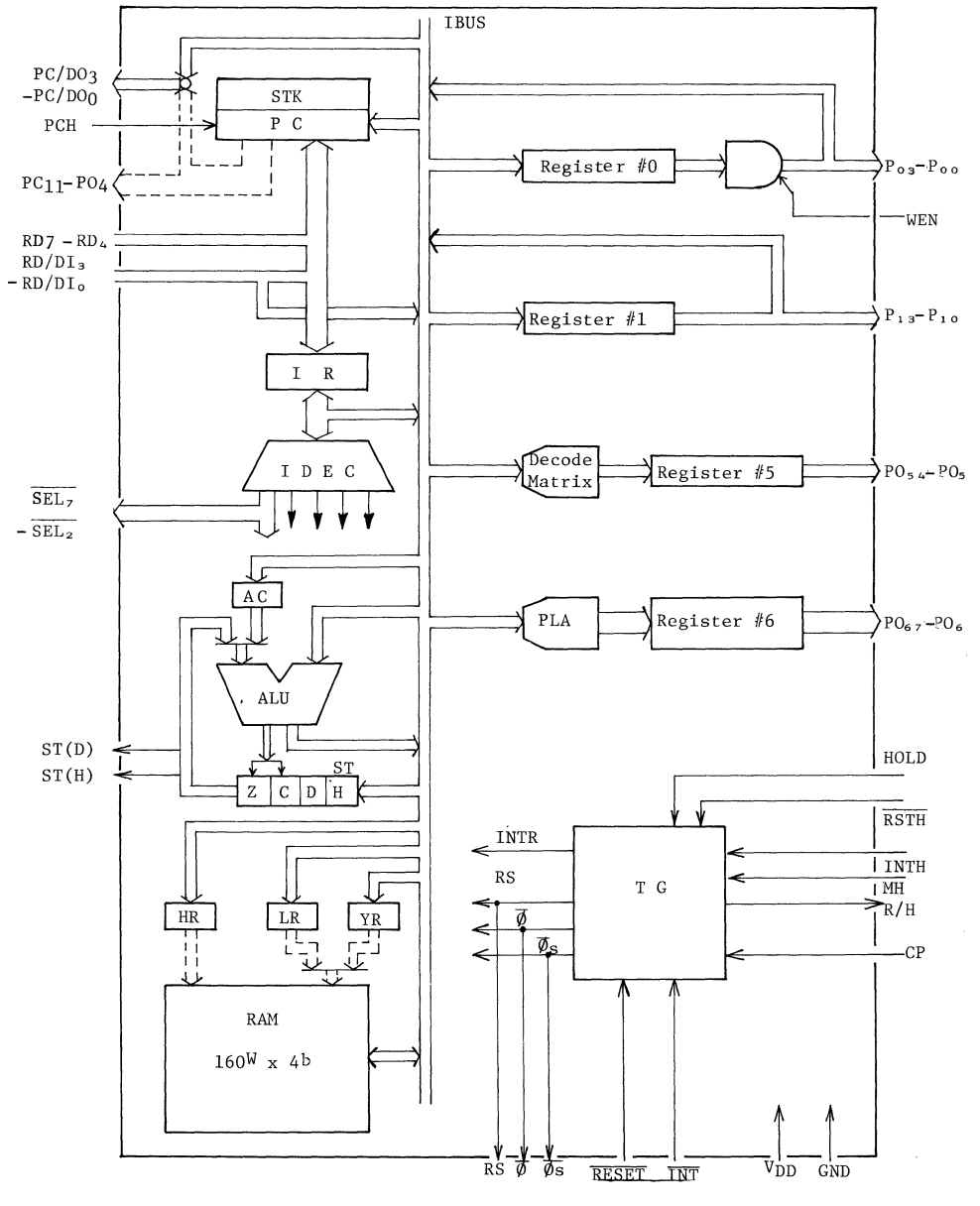


PIN NAMES & PIN DESCRIPTION

Pin Name	Input/Output	Function
P_{03}- P_{00}	Input/Output	4-bit general purpose I/O port State of input/output is designated by WEN terminal input. (common to TLCS-46A family)
P_{13}- P_{10}	Output	4-bit general purpose output port (common to TLCS-46A family)
PO_{54}- PO_{50}	Output	5-digit output port for display Content of built-in decode matrix is already designated (common to TLCS-46A family)
PO_{67}- PO_{60}	Output	8-segment output port for display Built-in PLA is already designated (common to TLCS-46A family)
$\overline{RESET}$	Input	Initialize Signal Input (without Schmitt circuit) (common to TLCS-46A family)
$\overline{INT}$	Input	Interrupt request signal input (without Schmitt circuit) (common to TLCS-46A family)
PC_{11}- PC_4	Output	The higher order 8-bit address output to external ROM
PC/DO_3- PC/DO_0	Output	The lower order 4-bit address output to external ROM/Port data output
RD_7- RD_4	Input	The higher order 4-bit data input from external ROM
RD/DI_3- RD/DI_0	Input	The lower order 4-bit data input from external ROM/Input port
$\overline{SEL_7}$ - $\overline{SEL_2}$	Output	Selection signal output for external port register and input port

Pin Name	Input/Output	Function
WEN	Input	Designate signal input for Input/Output of port 0
HOLD	Input	Hold operation control signal input
$\overline{RSTH}$	Input	Restart control signal input at time of hold operation
ST(D)	Output	D flag output
ST(H)	Output	H flag output
CP	Input	Internal basic clock input
$\overline{\phi}_S$, $\overline{\phi}$	Output	Basic timing output
RS	Output	Internal reset signal output
MH	Input	Monitor hold control signal input (for system debug)
R/H	Output	Run/Hold status signal output (for system debug)
PCH	Input	Program counter hold control signal input (for system debug)
INTH	Input	Interrupt hold control signal input (for system debug)
V_{DD}		Power supply
GND		GND

BLOCK DIAGRAM



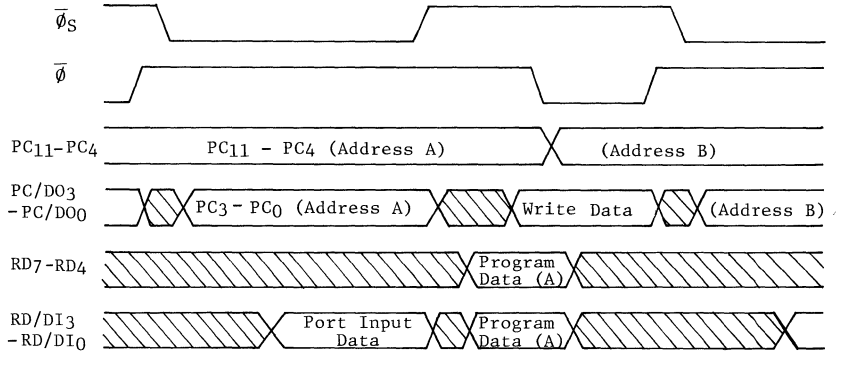
FUNCTIONAL DESCRIPTION

TCP4600AC is a system development evaluator which is used for developing TLCS-46A application system (program) and for confirming its operation. This makes it possible to form a configuration equal to TCP4620AP/TCP4630AP by program memory (hereinafter called ROM) and the external circuits relative to mask options.

1. Connection of Program Memory

Program counter (PC, 12 bits) output is used as address signal of external ROM (maximum capacity is 4096 words x 8 bits). Since the lower order 4 bits of address signal is multiplexed with the output of port data, it is necessary that they are externally separated.

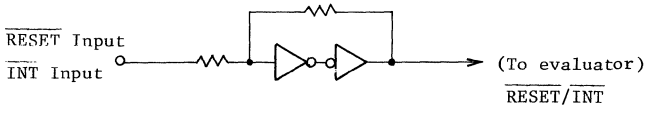
The data (8 bits) read out of ROM is read as instruction code in TCP4600AC. At this time, the data line of the lower order 4 bits is also used as port input data, so that it is necessary that data line is externally multiplexed.



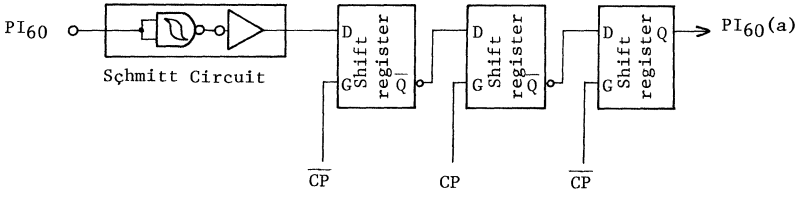
2. Schmitt Circuit

Each terminal of $\overline{\text{RESET}}$, $\overline{\text{INT}}$, and PI_{60} of TCP4620AP/TC4630AP are input terminals with Schmitt circuit. However, since no Schmitt circuit is contained in TCP4600AC, the circuit must be externally configured.

It is necessary to add shift register for timing shaping to PI_{60} terminal.



Schmitt Circuit



3. Oscillator and Divider

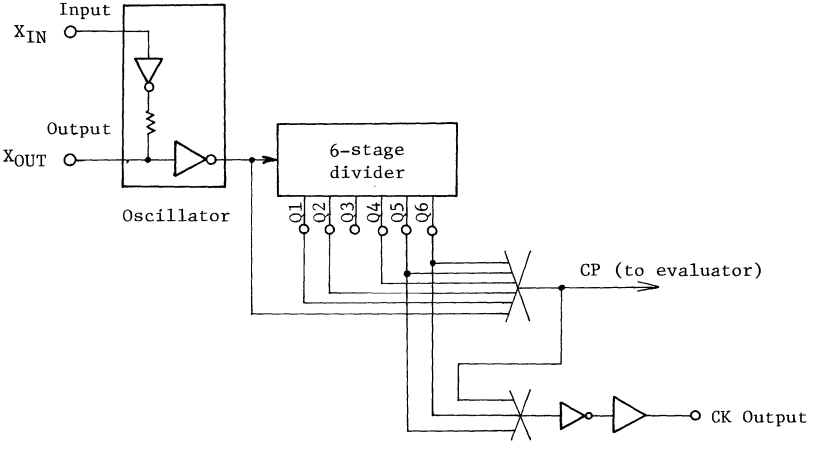
The mask options, which relate to the oscillator and divider of TCP4620AP/TCP4630AP, differ according to an oscillator to be used. For TCP4600AP these mask options are composed of external circuits.

(1) Oscillator

The basic clock (CP) of TCP4600AC is externally supplied. In this case, the divider forming the basic clock as well as the oscillation circuits of the oscillator to be used are externally composed, and the output of a divider suitable for oscillation frequency is supplied, as a basic clock, to the CP terminal of TCP4600AC.

Since TCP4600AC is not provided with the CK terminal for external timing, a signal equivalent to the CK terminal must be also composed of external circuit.

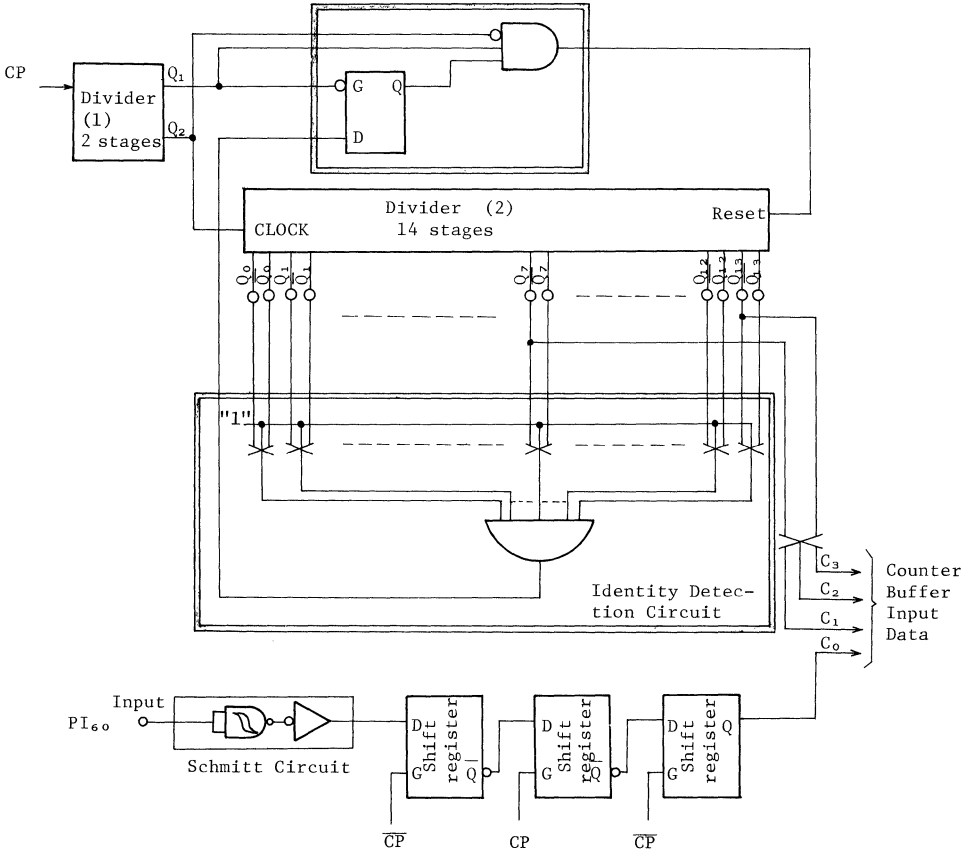
While the power is being supplied to the evaluator chip, the clock must be being supplied to the CP terminal at all times.



(Note) " ⫗ " means that either is connected.
(So with the following figures.)

(2) Divider

An example of cricuit configuration around a divider is shown as follows:



The portion of ▭ is required only when 100K Xtal is designated by mask options of mass production chip, and further 14-stage divider (2) is used as a resettable divider of count value "12500".

4. Input Port and Output Port

The input port and output port in TCP4620AP/TCP4630AP have plentiful mask options. In TCP4600AC, such mask options are composed of external circuits.

(1) Input port

The data of input port is input from RD/DI terminal.
When the data of input port (port No. i) is input to RD/DI terminal during the period of time when the equation,

$$SEL_i \cdot \phi_S = 1 \quad (i : \text{port No.}),$$

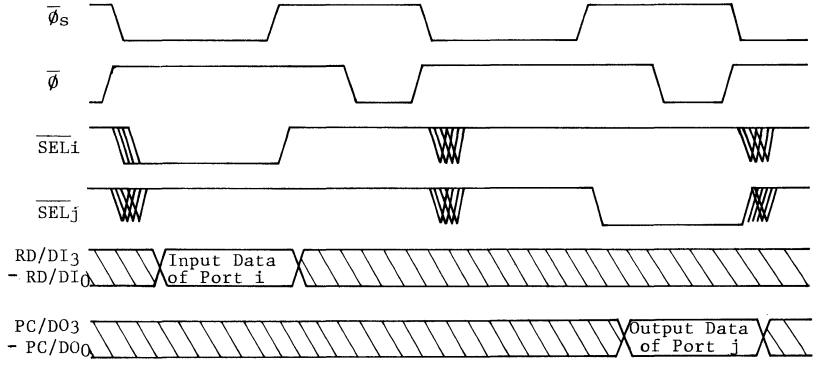
holds, TCP4600AC starts reading it as input port data.

(2) Output port

The data of output port is output from PC/DO terminal.
Since TCP4600AC outputs the data of output port (port No. i) from PC/DO terminal during the period of time when the equation,

$$\overline{SEL_i} \cdot \phi = 1 \quad (i : \text{port No.}),$$

hold, this data is written in the externally installed register. Further, since at time of system reset an internal initialize signal is output from RS terminal, it is necessary to clear (all "0") the port register by use of this signal and to initialize it.



(3) Port 0

Prot 0 is a port that can make switching of input/output by program (D flag of ST), and can be designated to a port exclusivelly used for output by mask options.

In TCP4600AC, the mask option of this port can be realized by use of each terminal of WEN and ST(D).

WEN terminal is an input line that defines whether port 0 is placed in an output mode or an input mode. When the terminal is at "1" level, it places port 0 in an output mode and when it is at "0" level, it places port 0 in an input mode.

A state of D flag of status register is output from ST (D) terminal.

- o When input and output are switched by use of program,
  WEN = ST(D)
  WEN terminal is externally connected to ST(D) terminal.
- o When port 0 is used as port exclusivelly for output,
  WEN = "1"
  WEN terminal is fixed to "1" level.

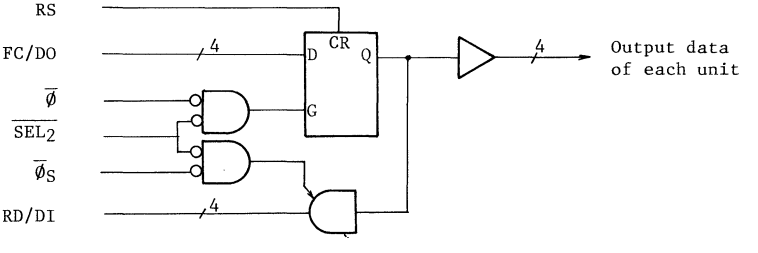
(4) Port 2 and Port 4

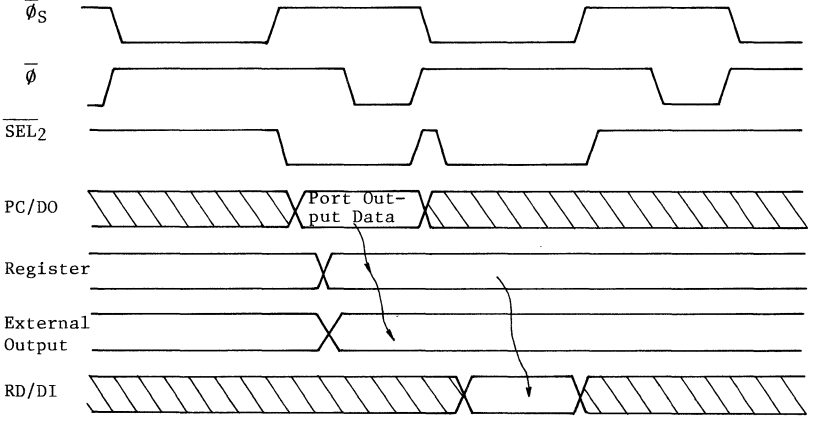
Port 2 and Port 4 are input/output selectable ports by use of mask options.
When these ports are used as input ports, the external input data is input to RD/DI terminal during the period when each of the following equations holds: $SEL_2 \cdot \phi_S = 1$ and $SEL_4 \cdot \phi_S = 1$.

On the other hand, when these prots are used as output ports, output data are output to PC/DO terminal during the period when each of the following equations holds:

$SEL_2 \cdot \phi = 1$ and $SEL_4 \cdot \phi = 1$.

Therfore, this data is written in the register externally installed, and is output to the outside through a buffer. And, at the time when the equations, such as $SEL_2 \cdot \phi_S = 1$ and $SEL_4 \cdot \phi_S = 1$, hold, the outputs of respective registers are input to RD/DI terminal. The externally installed register must be cleared (all "0") by the internal initialize signal from RS. terminal.





(5) Port 3

Port 3 is I/O port exclusively used for TCP4600AC. The function of port 3 is the same as the function of other ports.

This port is designated as register No. "3" even in case where it is used as either of input port or output port.

(6) Output port 5 and output port 6 (output port 7)

For TCP4600AC, each output terminal of PO_5 and PO_6 is available as output for display. However, when it is used as general output port or when it is used after changing the contents of decode matrix or PLA, it is configured by external circuit.

The contents of decode matrix and PLA built in TCP4600AC are as follows:

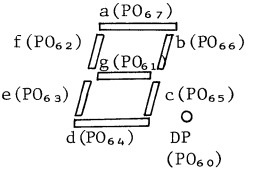
Contents of Decode Matrix

Write Data		F-6	5	4	3	2	1	0
Output State	PO_{54}	0	1	0	0	0	0	0
	PO_{53}	0	0	1	0	0	0	0
	PO_{52}	0	0	0	1	0	0	0
	PO_{51}	0	0	0	0	1	0	0
	PO_{50}	0	0	0	0	0	1	0

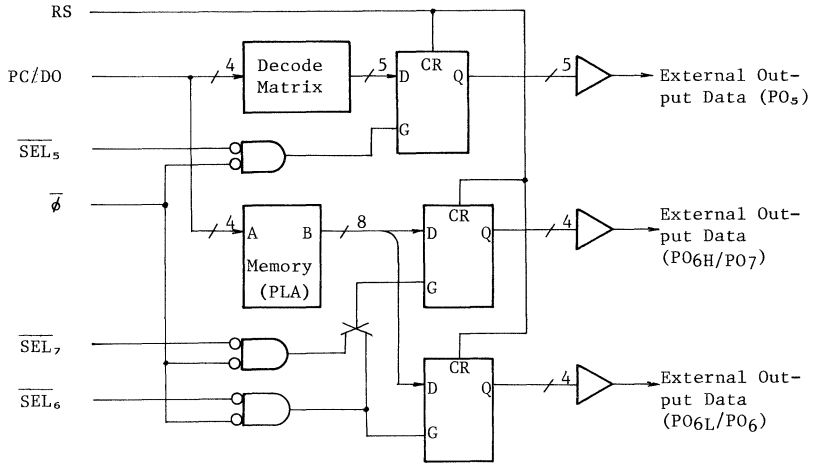
PLA

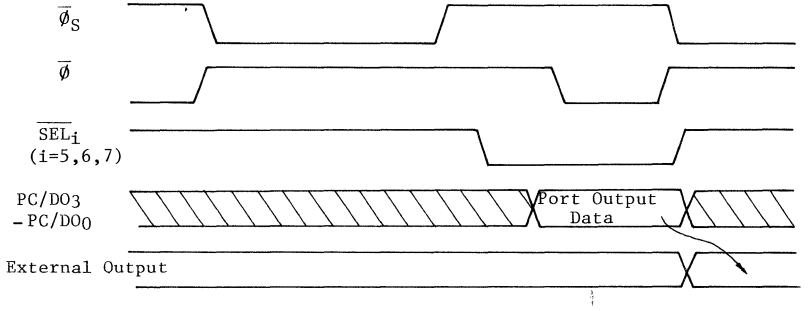
PLA can be expressed as memory of 16 words x 8 bits. The 4-bit write data for port 6 is the address of PLA, and the 8-bit data read out from PLA comes to the output data of the output port. When the data of 8 bits output at this time is expressed by hexadecimal 2 digits, PLA built-in TCP4600AC is as follows:

Address	Data	Form of Character
0	FC	0
1	60	1
2	DA	2
3	F2	3
4	66	4
5	B6	5
6	BE	6
7	E4	7
8	FE	8
9	F6	9
A	FD	0.
B	00	(Blank)
C	02	-
D	CE	P
E	9E	E
F	8E	F



When the built-in decode matrix and PLA are used changing their contents or are used as general output ports, they are externally configured by use of data output PC/DO, select signals $\overline{SEL_5}$, $\overline{SEL_6}$ and $\overline{SEL_7}$ and timing signal $\overline{\phi}$.





Output Timing of PO_5, PO_6 (PO_7)

5. Hold Operation

TCP4620AP/TCP4630AP is provided with hold function. In TCP4600AC, this function is configured by each terminal of HOLD, $\overline{RSTH}$ and ST(H), and the siganl of C_3 which is MSB of counter buffer input configured by external circuits. (For C_3, refer to the figure of divider.)

In case hold operation is performed:

HOLD = ST(H) : Designation of hold operation application

$\overline{RSTH}$ = C_3 : Designation of hold operation release signal

Each terminal of HOLD and ST(H) is externally connected. C_3 signal that is MSB of counter buffer is input to $\overline{RSTH}$ terminal.

In case hold operation is not performed:

HOLD = "0" : Designation of no use of hold operation

$\overline{RSTH}$ = "0" : Designation of no use of hold operation

Each terminal of HOLD and $\overline{RSTH}$ is fixed to the "0" level.

CONTROL TERMINALS FOR DEBUG

There are some functions and terminals to make easy the development of TLCS-46A application system (program).

(1) MH terminal (Monitor hold control input)

Monitor hold function stops the operation of TCP4600AC by unit of execution instruction.

The operation stops after completion of current excecution instruction by inputting "1" level into MH terminal. However, during "1" period of Y register flag (EYR = 1), the operation does not stop. When the system enters into the interrupt service routine, if stop request is made, the system stops after having jumped to the interrupt service routine.

In the stop state, program counter output the next address. Restart is made by inputting "0" level into MH terminal, and the first cycle makes instruction fetch and at the same time executes NOP instruction internally.

(2) R/H terminal (Run/Hold status output)

Run/Hold monitor function is the response singnal of monitor hold function. During stop of operation by monitor hold function,"0" level is output from R/H terminal (which is reset by the instruction cycle just short of stopping by MH signal), and during normal operation "1" level is output from R/H terminal.

(3) PCH terminal (Program counter hold control input)

Program counter hold function holds the previous state without updating the value of program counter. This function is operated by inputting "1" level into PCH terminal.

(4) INTH terminal (Interupt hold control input)

Interrupt hold function is a function to make interrupt request waiting. Even if interrupt latch is set by inputting "1" level into INTH terminal, jump to interrupt routine is not performed. In this case, interrupt request is kept waiting until "0" level is input into INTH terminal.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Supply Voltage	-0.3V to +7.0V
V_{IN}	Input Voltage	-0.3V to V_{DD}+0.3V
V_{OUT}	Output Volatage	-0.3V to V_{DD}+0.3V
P_D	Power Dissipation	600 mW
T_{sol}	Soldering Temperature & Time	260°C (10 SEC)
T_{stg}	Storage Temperature	-55°C to +125°C
T_{opr}	Operating Temperature	-10°C to +70°C

ALLOWABLE OPERATING CONDITIONS

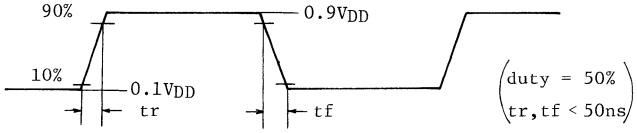
SYMBOL	PARAMETER	RATING
T_a	Ambient Temperature	-10°C to +70°C
V_{DD}	Supply Voltage	4V to 6V
V_{OH}	Output High Voltage	Min. V_{DD}-3.5V ($\geq$1.5V)
V_{OL}	Output Low Voltage	Max. 3V
fcp	Basic Clock Frequency	20KHz to 200KHz

DC CHARACTERISTICS (Ta=-10°C to 70°C, V_{DD}=4V to 6V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (Note1)	MAX.	UNIT
V_{IH}	Input High Voltage		V_{DD}x0.7	V_{DD}x0.55	V_{DD}	V
V_{IL}	Input Low Voltage		0	V_{DD}x0.45	V_{DD}x0.3	
I_{IH}	Input High Current	V_{DD}=6V, V_{IN}=6V	-	-	20	µA
I_{IL}	Input Low Current	V_{DD}=6V, V_{IN}=0V	-	-	-20	
V_{OH}	Output High Voltage	V_{DD}=5V, Output Open	4.7	4.9	-	V
V_{OL}	Output Low Voltage		-	0.1	0.3	
I_{OH}	Output High Current	V_{DD}=4.5V, V_{OH}=2.4V	-0.7	-2	-	mA
I_{OHI}	Output High Current (P05, P06)		-2.5	-6	-	
		V_{DD}=5V, V_{OH}=4.2V	-1.1	-2.5	-	
I_{OL}	Output Low Current	V_{DD}=4.5V, V_{OL}=0.45V	1.6	4	-	
I_{OL1}	Output Low Current (P05, P06)		3.2	8	-	
I_{DDO}	V_{DD} Supply Current in Normal Operation	V_{DD}=6V, fcp=100KHz Output Open V_{IN}=5.9V/0.1V (Note 2)	-	150	450	µA
I_{DDH}	V_{DD} Supply Current in Hold Operation		-	40	120	

Note1: Typical values are at Ta=25°C and V_{DD}=5V.

Note 2: CP input waveform at the time of V_{DD} Supply Current

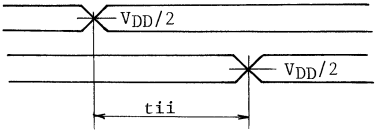


AC CHARACTERISTICS (Ta=-10°C to +70°C, V_{DD}=4V to 6V)

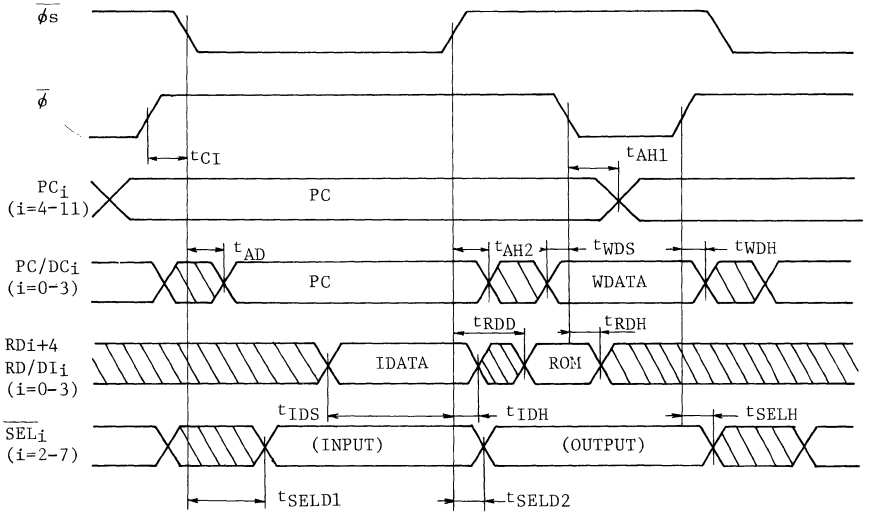
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP. (NOTE 1)	MAX.	UNIT
t_{CI}	Timing Signal Inhibit Time	CL = 50 pF (Note 2)	150	-	1500	ns
t_{AD}	Address Delay Time		-	-	2000	ns
t_{AH1}	Address Hold Time		80	-	-	ns
t_{AH2}	" "		200	-	-	ns
t_{RDD}	Data Delay Time		-	-	1000	ns
t_{RDH}	Data Hold Time		80	-	-	ns
t_{SELD1}	SEL Delay Time (for Input)		-	-	1000	ns
t_{SELD2}	SEL Delay Time (for Output)		100	-	500	ns
t_{SELH}	SEL Hold Time		300	-	-	ns
t_{WDS}	Write Data Set Up Time		500	-	-	ns
t_{WDH}	Write Data Hold Time		300	-	-	ns
t_{IDS}	Read Data Set Up Time		1000	-	-	ns
t_{IDH}	Read Data Hold Tiem		100	-	-	ns
t_{MHD}	MH Input Delay Time		-	-	500	ns
t_{MHH}	MH Input Hold Time		100	-	-	ns
t_{PCHD}	PCH Input Delay Time		-	-	500	ns
t_{PCHH}	PCH Input Hold Time		100	-	-	ns
t_{INTHD}	INTH Input Delay Time		-	-	500	ns
t_{INTHH}	INTH Input Hold Time		100	-	-	ns
t_{WCP}	CP Pulse Width	$V_{IN}=V_{IH}/V_{IL}$	$0.4/f_{cp}$	-	$0.6/f_{cp}$	SEC
t_{WRESET}	$\overline{\text{RESET}}$ Pulse Width		2 tcy	-	-	μs
t_{WINT}	$\overline{\text{INT}}$ Pulse Width		2 tcy	-	-	μs

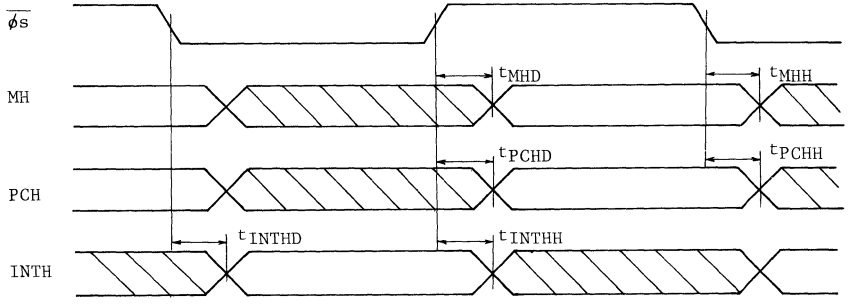
Note 1 : Typical values are at Ta=25°C and V_{DD}=5V.

Note 2 : AC test condition



TIMING WAVEFORMS

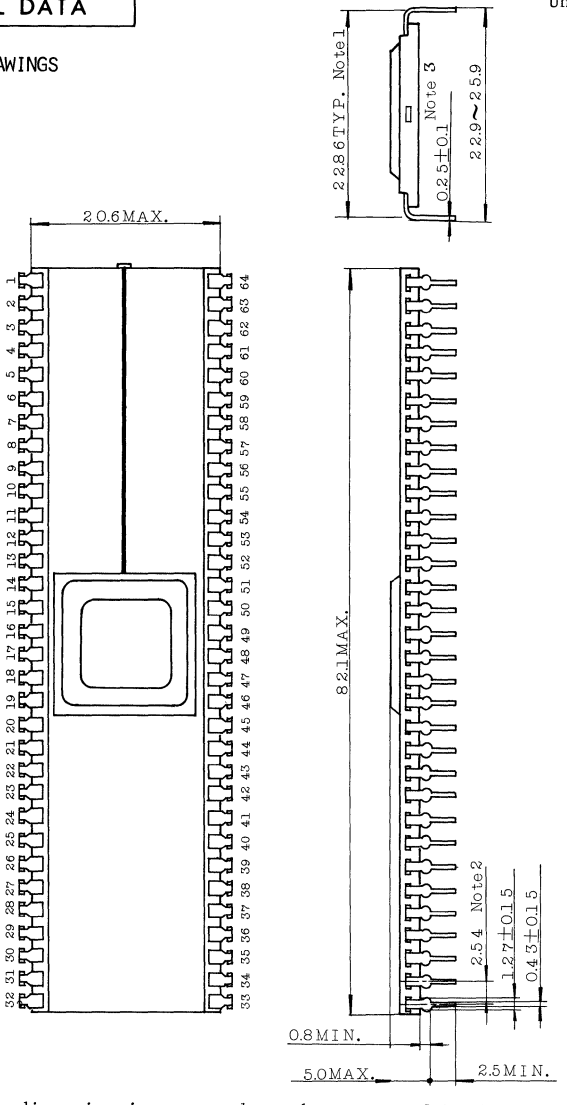




TCP4600AC

Unit in mm

OUTLINE DRAWINGS



Note 1: This dimension is measured at the center of bending point of leads.

Note 2: The lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No. 64 leads.

Note 3; The metal on the side of the package is GND level.

PRECAUTIONS FOR USE

(1) Clock at time of power supplied

When TLCS-46A starts by $\overline{\text{RESET}}$, clock must be always supplied. There is no problem when clock is obtained by externally mounting the oscillator of crystal, celamic or IFT by use of internal clock generator in TCP4620AP/TCP4630AP, but care should be exercised when clock is externally supplied or when TCP4600AC is used.

(2) Control of I/O port

In port 0, Input/Output can be switched by program; therefore, care should be taken not to become driver short between the port and external circuit.

(3) Current capacity of output port

Each of output port 5 and output port 6 has a large current capacity as port for display. However, if the output port is supplied with a large current exceeding its capacity, it may cause destruction or deterrioration in character.

(4) Handling of unused terminal

When an unused input terminal is left open, it may cause malfunction and increase in power dissipation; therefore, insure to connect the terminals to V_{DD} or GND level. (It is the safest method to connect termianl via resistance.)

Further, insure to connect TEST terminal to GND because this terminal is installed for LSI testing.

(5) Electrostatic destruction

In TLCS-46A series, the input circuit is provided with protective resistance and protective diode for preventing electrostatic destruction. However, the surge equivalent weight is small as compared with discrete resistance and diode; therefore, carry TLCS-46A series in a conductive container so as not to add the surge directly into the system, when required.

(6) Latch-up phenomenon

When the voltage lower than GND or the voltage higher than V_{DD} is applied to input terminal and output terminal, a phenomenon called latch-up characteristic of CMOS presents. This phenomenon may cause destruction and degradation of elements; therefore, care should be taken not to apply the voltage exceeding the maximum rating to the input terminal and output terminal.