TCP4632BF

C^2-MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

PRELIMINARY

GENERAL DESCRIPTION

The TCP4632BF is a C^2MOS 4-bit single-chip microcomputer capable of directly driving liquid crystal display provided with 1/3 or 1/4 duty, and is most suitable for use in a wide range of application fields, such as a system requiring low power dissipation.

The TCP4632BF contains the controller and driver for driving the liquid crystal display (hereinafter referred to as LCD) to the TCP4630AP. For the use and study of this device, refer to the technical data for the TCP4630AP in addition to this technical data.

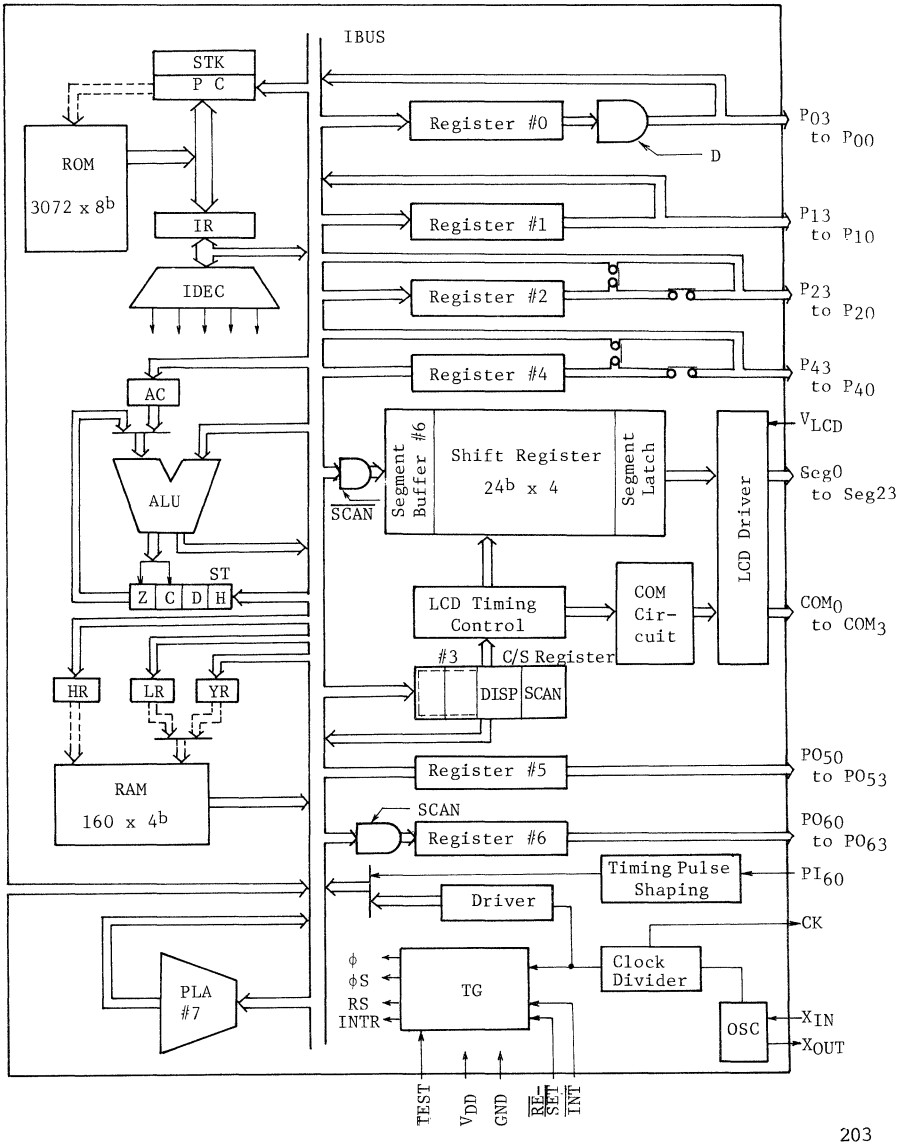
FEATURES

- C^2MOS 4-bit single-chip microcomputer of low power dissipation
- Memory capacity
  - Program region (ROM) 3072 words x 8-bit
  - Data region (RAM) 160 words x 4-bit (including RAM for display)
- Instruction execution time: 10 μs (400kHz ceramic oscillator/IFT)
- 52 instructions
- Built-in LCD controller
  - 1/3 or 1/4 duty (designated by mask options)
- Built-in LCD direct driver
  - Common output 4 pins
  - Segment output 24 pins
- Input/Output port
  - I/O port 1 x 4-bit (I/O can be switched by programs.)
  - 1 x 4-bit (I/O can be designated by mask options.)
  - 1 x 4-bit (I/O can be designated by mask options.)

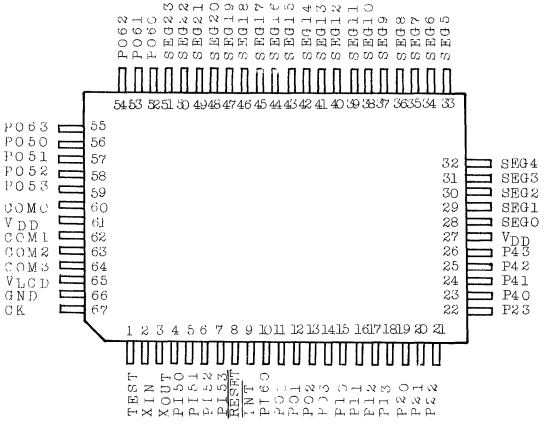
Output port	3 x 4-bit	(General purpose output port)
Input port	1 x 4-bit	(Pull-up/Pull-down resistor with input resistance can be selected.)
	1 x 4-bit	

- o External power supply is available for LCD (V_{LCD})
- o Built-in display decoder (Can be designated by mask options with decoder data.)
- o Blanking operation
- o Hold operation (LCD can be displayed during hold operation.)
- o Power-down mode (Display blanking)
- o 67-pin plastic package

BLOCK DIAGRAM



PIN CONNECTIONS (Top View)



PIN NAMES/PIN DESCRIPTION

Pin Name	Input/ Output	TCP4620AP/30AP		TCP4632BF	
		No.of pins	Function	No.of pins	Function
TEST	Input	1	LSI test input (always kept set at 0.)	1	LSI test input (always kept set at 0.)
X_{IN}	Input	1	Oscillator connecting terminal	1	Oscillator connecting terminal
X_{OUT}	Output	1	Oscillator connecting terminal	1	Oscillator connecting terminal
PI_5	Input	4	General purpose input port	4	General purpose input port
$\overline{RESET}$	Input	1	Reset input	1	Reset input
$\overline{INT}$	Input	1	Interrupt input	1	Interrupt input
PI_6	Input	1	General purpose input	1	General purpose input

Pin Name	Input/ Output	TCP4620AP/30AP		TCP4632BF	
		No.of pins	Function	No.of pins	Function
P_0	I/O	4	I/O port	4	I/O port
P_1	Output	4	General purpose output port	4	General purpose output port
P_2	Input/ Output	4	General purpose input/ output port	4	General purpose input/ output port
P_4	Input/ Output	4	General purpose input/ output port	4	General purpose input/ output port
V_{DD}		1	Power supply	2	Power supply
$SEG_{0\sim23}$	Output			24	LCD segment driver output
PO_6	Output	4	PLA output port	4	General purpose output port
PO_7	Output	4	PLA output port		
PO_5	Output	5	Decode matrix output port	4	General purpose output port
$COM_{0\sim3}$				4	LCD common driver output
V_{LCD}				1	LCD external power supply terminal
GND		1	GND	1	GND
CK	Output	1	External timing output	1	External timing output

CONFIGURATION OF PORT AND REGISTER

	Name	Sym-bol	Pin Name	Reg. No.	Function	Remarks
*	I/O Port	P_0	P_{03} to P_{00}	0	I/O Port	I/O switching is controlled by D flag of ST. This port can be designated as a dedicated output port by mask options.
	Output Port	P_1	P_{13} to P_{10}	1	Output Port	General purpose output port. The contents of register can be referred to by a program.
*	Input/ Output Port	P_2	P_{23} to P_{20}	2	Input/ Output Port	Input/output can be designated by mask options. The contents of register can be referred to by a program.
*	Command Register	C/S	———	3	Command Register	LCD display is controlled by a 2-bit register. The contents of register can be referred to by a program.
*	Input/ Output Port	P_4	P_{43} to P_{40}	4	Input/ Output Port	Input/output can be designated by mask options. The contents of register can be referred to by a program.
	Input Port	PI_5	PI_{53} to PI_{50}	5	Input Port	General purpose input port with 150kΩ (TYP.) resistance. Pull-up/Pull-down designation can be made by mask options.
*	Output Port	PO_5	PO_{53} to PO_{50}		Output Port	General purpose output port. The contents of register can not be referred to by a program.
	Input Port	PI_6	PI_{60}	6	Input Port	1-bit general purpose input port. (Built-in Schmitt circuit).
*	Output Port	PO_6	PO_{63} to PO_{60}		Output Port	General purpose output port. The contents of register can not be referred to by a program.
*	PLA	PLA	———	7	PLA	PLA. PLA can be used as a display data decoder or a data decoder. The contents of decode is designated by mask options.

Note The asterisk (*) indicates the points of difference between TCP 4620AP/TCP4630AP and this device.

(a) Neither command register nor PLA (available for reference by a program) is contained in the TCP4620AP/TCP4630AP.

(b) Since PO_5 and PO_6 contain neither decode matrix nor PLA, the number of output pins of each port is 4.

(c) Care should be taken to the fact that P_0, P_2, P_4, PO_5 and PO_6 of this device are different from those of TCP4620AP/TCP4630AP in electrical characteristics.

LCD CONTROLLER/DRIVER

The TCP4632BF contains a driver circuit capable of directly, dynamically driving the LCD provided with 1/3 or 1/4 duty by the 1/3 bias method.

LCD connection terminals amount to 29 in total as follows:

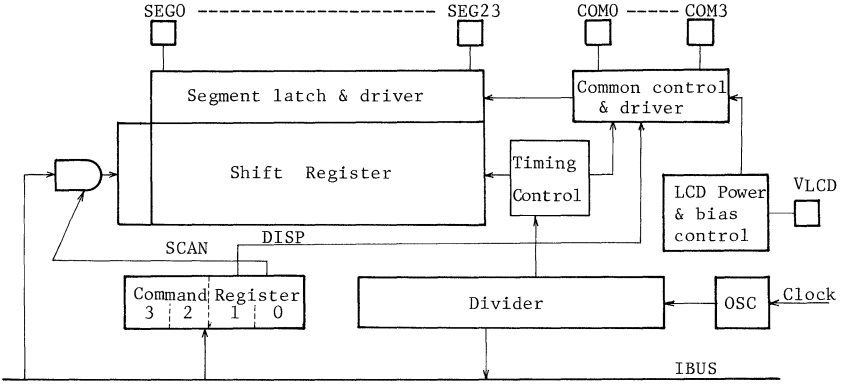
Common driver output	(COM0 to COM3)	4
Segment driver output	(SEG0 to SEG23)	24
V_{LCD} terminal as LCD driving power terminal		1

The display ability makes it possible directly to drive the following LCDs according to the number of time divisions:

(a) 1/4 duty (1/3 bias) LCD
Max. 96 segments (12 digits x 8 segments)

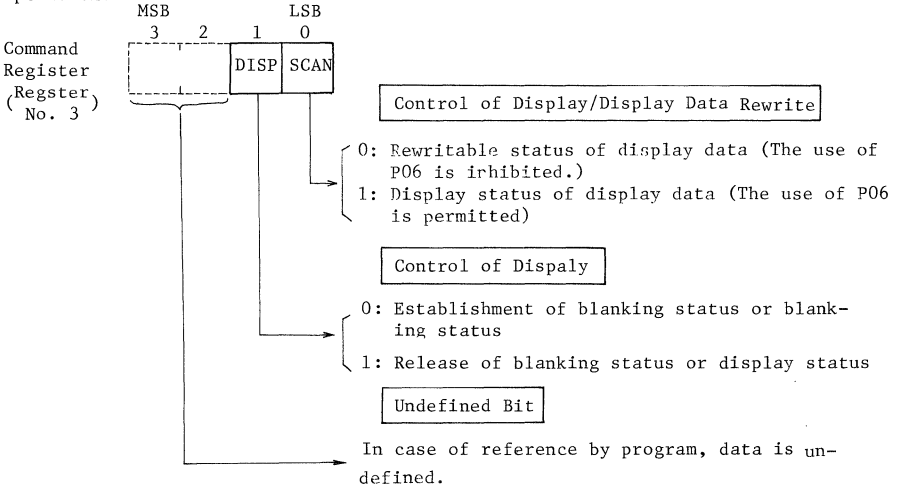
(b) 1/3 duty (1/3 bias) LCD
Max. 72 segments (8 digits x 9 segments)

BLOCK DIAGRAM OF LCD DRIVE CONTROLLER



CONTROL OF DRIVE CIRCUIT

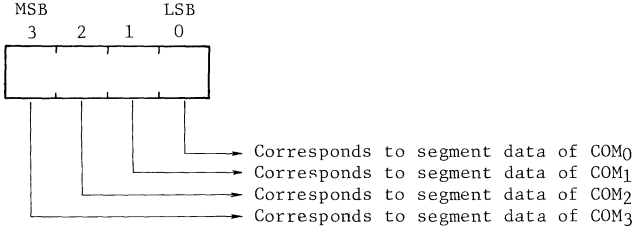
The operation of LCD drive circuit is controlled by the contents of command register. The command register is a 2-bit register and is accessed as register No. '3'. Both of two bits are reset to "0" by an initialize operation.



DISPLAY OPERATION

SETUP OF DISPLAY DATA

The TCP4632BF internal processing data corresponds to LCD drive terminal in such a way as bit 0, bit 1, bit 2 and bit 3 of the processing data correspond to each segment data of COM0, COM1, COM2, and COM3, respectively.

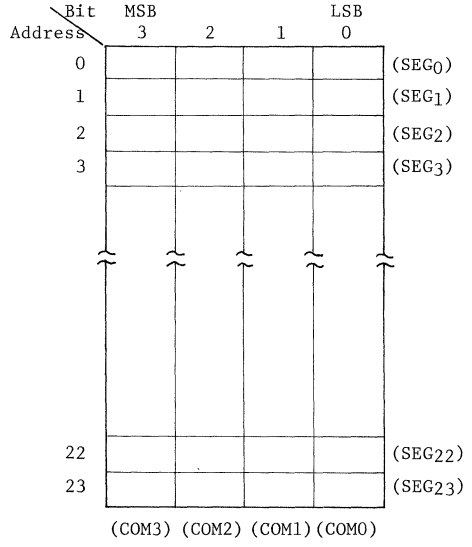


The conversion of LCD display data is arbitrarily set up by a program or by a built-in PLA register (setup of the contents by mask options).

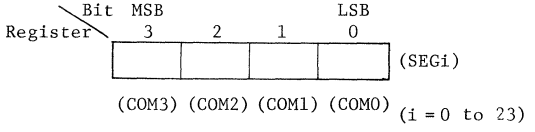
TRANSFER OF DISPLAY DATA

LCD display data setup by a program or PLA register is displayed by transferring it to the shift register of LCD driver by the program.

The transfer method is divided into two categories: one is that the converted data is transferred as it is, and another is that a displaying data region set up in the data memory (RAM) is transferred after it has been once stored. Even by either method, each bit of LCD segment (dot) and TCP4632BF internal processing data corresponds to each other by one to one.



In case data memory is provided with display region



In case processing data intact is transferred

Each bit of display data expresses data of segment (dot) equivalent to (SEGi COMj : $0 \leq i \leq 23$, $0 \leq j \leq 3$). When the data displays "1", the display lights. In case of the use of LCD with 1/3 futy (COM0 to COM2), the data of bit 3 (MSB) has no meaning as a LCD display data.

Transfer and rewrite of display data is made by a program as follows:

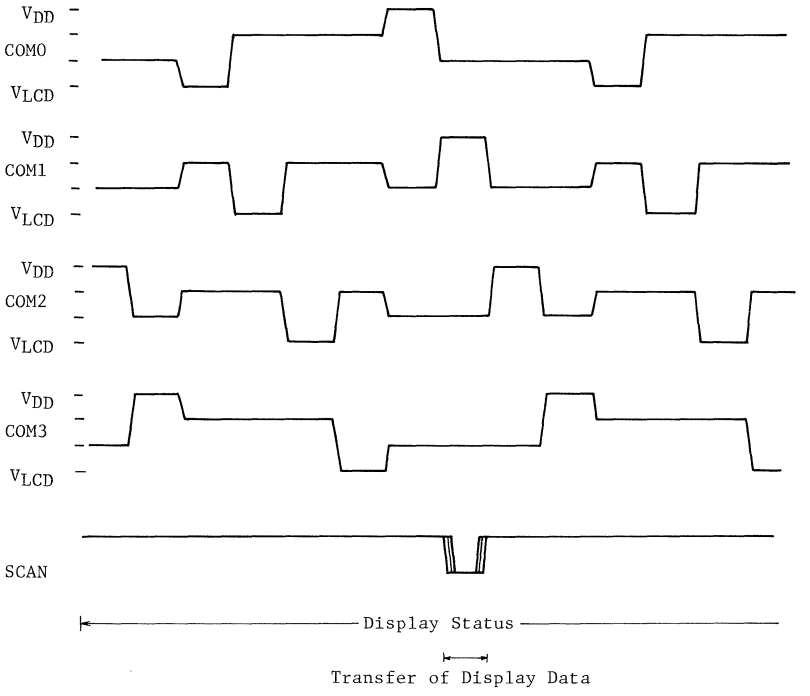
First, clear SCAN bit to '0'. (Immediately after initialization, the bit is at '0'.) Next, transfer 4-bit data equivalent to SEG. 23 to Register No. 6 (SAR 6), and then transfer 4-bit data equivalent to SEG 22. Continuously transfer 4-bit data in sequence by programs until the transfer of data equivalent to SEG. 0 is comleted.

This operation sllows 4×24-bit data to be written into the shift register within LCD drive circuit. After the data transfer of 24 words has been finished, SCAN bit is set to '1'. When SCAN bit goes to '1', writing into the shift register is inhibited, and LCD begins to be driven by the data newly held. Data switching is made from COMj to come next (data output equivalent to bit j to SEGi) and is automatically scanned to the next COMj+1.

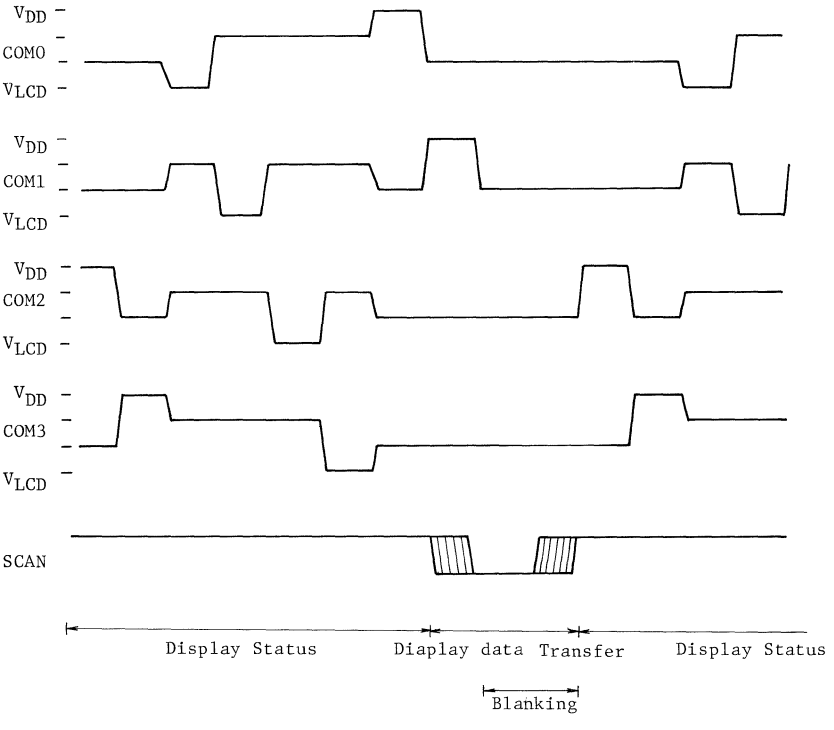
In the case that the period (period of SCAN = 0) of 24-word data transfer by means of a program is within the one COM period (1/4fF), the blank period does not come into the transfer period, and the display contents are switched. However, in the case that the period (period of SCAN = 0) of 24-word data transfer by means of a program crosses switching of COM (this phenomenon presents by timing of data transfer period or it presents when the data transfer period becomes longer than one COM period), no correct display data is secured during the period; thus, a blank is automatically inserted in the period.

When the display data is transferred to a shift register equivalent to Register No.6 during the period of SCAN = 0, all of 24 words must be transferred to the shift register. However, if SEG0 to SEGk-1 outputs only, not all of SEG0 ∿ SEG23 outputs, are used, k word only can be transferred.

In case of SCAN = 0, write in Register No. 6 (SAR = 6) means write in the shift register as a display data. In case of SCAN = 1, however, it means write in output port PO_6.



As the display data transfer period is short, it does not come in the blanking period.



As the display data transfer period is long, it comes in the blanking period.

LCD FRAME FREQUENCY

Frame frequency (LCD drive frequency) is given by the built-in devider. The frame frequency f_F is given from internal clock frequency f_{CP} by the following formula:

$$f_F = f_{CP} \times \frac{1}{2^m \times n}$$

Where, m is the number of divider stages. When fx = 400 kHz and f = 200 kHz, m is set to 9. n is the number of time division. Therefore,

In case of 1/3 duty $f_F \fallingdotseq 130$ Hz

In case of 1/4 duty $f_F \fallingdotseq 98$ Hz

The period equivalent to one COM is

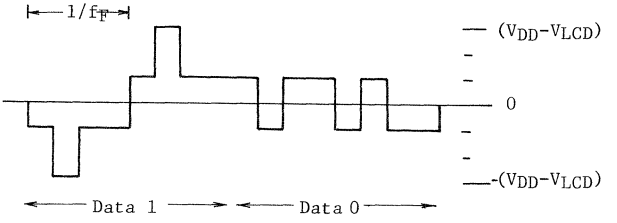
$$\frac{2^m}{f_{CP}} \quad (\fallingdotseq \frac{2^{m-1}}{f_{CY}})$$

therefore, when m = 9, the period is equivalent to 256 steps.

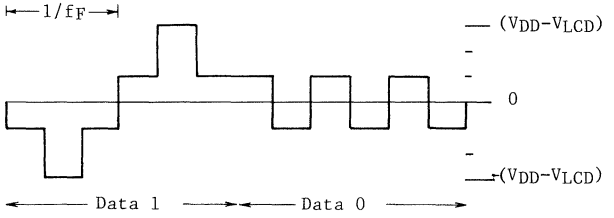
LCD DRIVE WAVEFORM

TCP4632BF is capable of directly, dynamically driving the LCD provided with 1/3 or 1/4 duty by 1/3 bias method.

In case of 1/3 or 1/4 duty, the voltage applied to LCD is + (V_{DD} - V_{LCD}) to -(V_{DD} - V_{LCD}).



1/4 duty (1/3 bias) drive

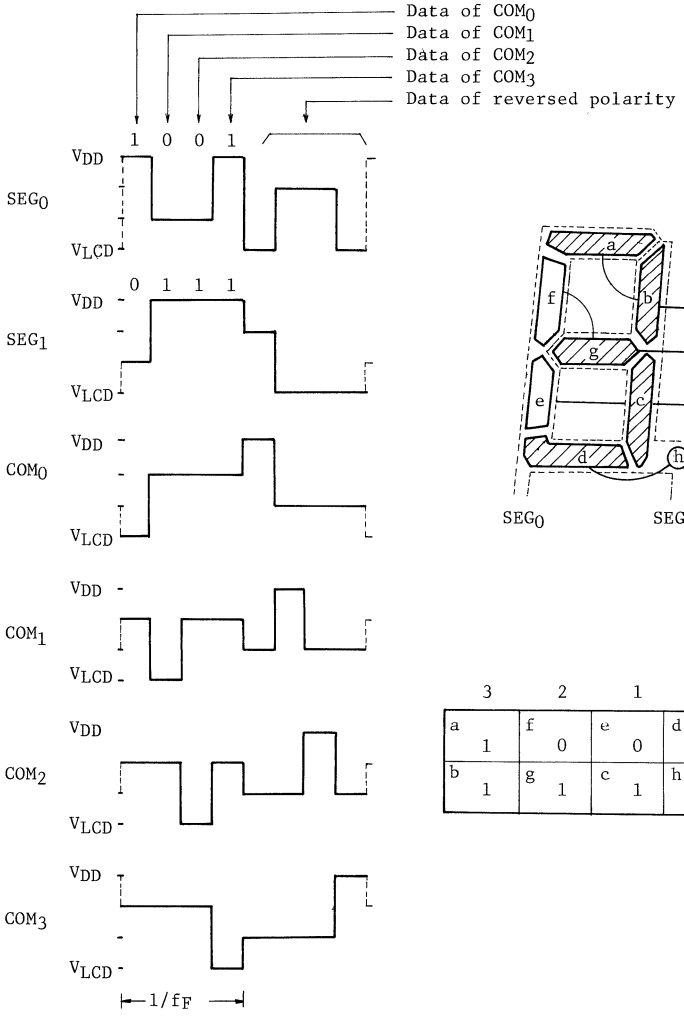


1/2 duty (1/3 bias) drive

(Note) f_F : LCD frame frequency

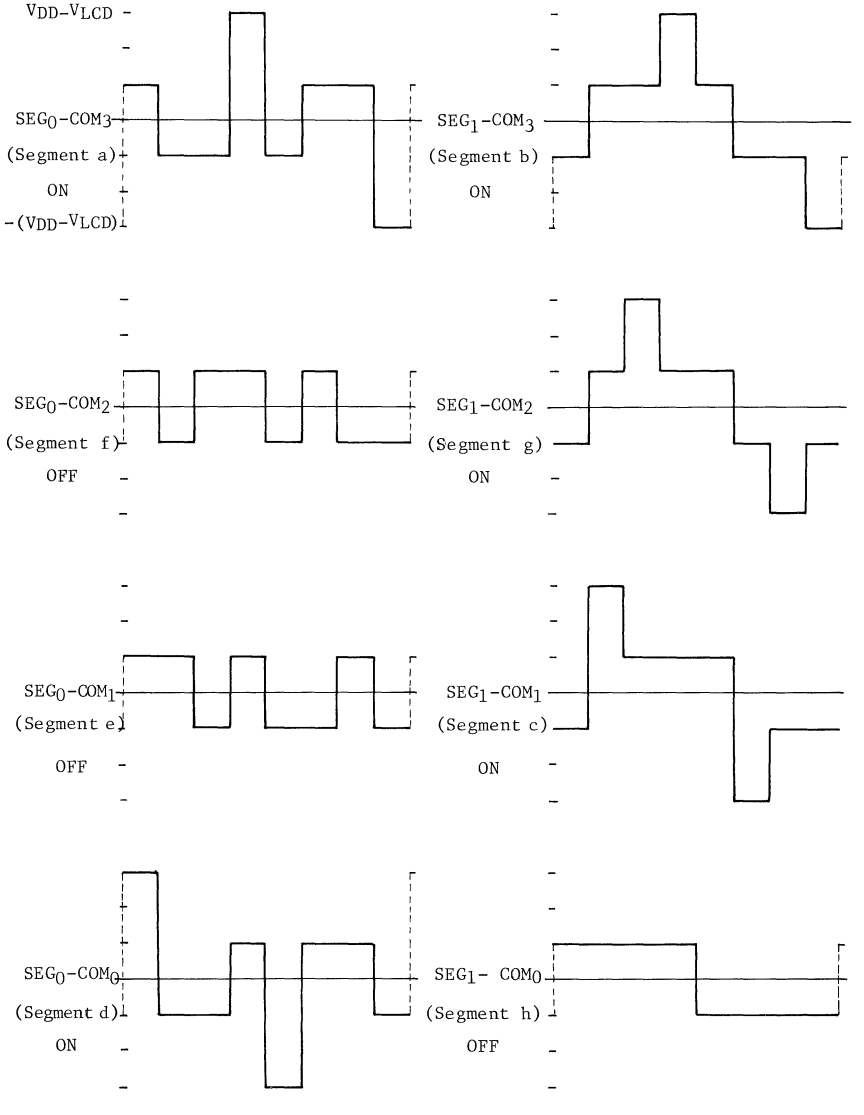
V_{LCD} : V_{LCD} terminal voltage

Each terminal waveform in case of displaying data "3" at 1/4 duty is as follows:



3	2	1	0	
a 1	f 0	e 0	d 1	SEG0
b 1	g 1	c 1	h 0	SEG1

The voltage between each SEG - COM is as follows:



LCD DRIVE VOLTAGE

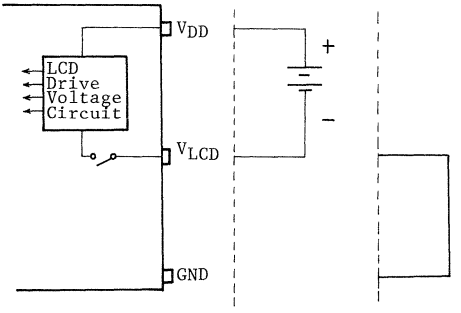
V_{LCD} is an input terminal of LCD driving power. LCD drive voltage is required to be supplied between V_{DD}-V_{LCD}.

If the operation voltage of the TCP4632BF is identical with the LCD drive voltage, V_{LCD} is connected to GND.

The supply of drive voltage generated by LCD drive circuit is controlled within this device according to the operating status of CPU. In the following cases that there is a possibility of keeping LCD drive circuit stationary for a long period of time, the supply of LCD drive voltage is cut with the built-in switch.

① Initialize operation

② SCAN = 0 and H = 1



The switch turned off by initialize operation is turned on by setting the SCAN bit of command register to '1', thus resulting in the supply of LCD drive voltage. After that, even if the SCAN bit of command register is reset to '0', LCD drive voltage is kept supplied.

For performing hold operation, H must be set to '1' in a state of SCAN = 1 and at time of normal LCD display because rewrite of display data has been already finished. In this case, LCD drive circuit is still in operation to continue display. However, while display data is being rewritten, if H is set to '1' at time of SCAN = 0, the supply of LCD drive voltage is cut.

When the supply of LCD drive voltage is cut with the built-in switch, all of SEG and COM outputs attain V_{DD} lelvel.

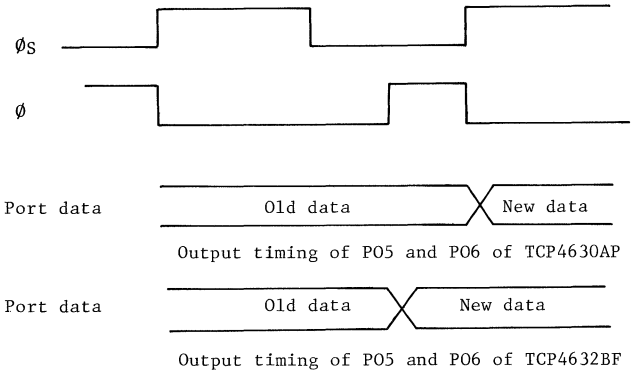
OUTPUT PORT (PO5, PO6)

PO5 and PO6 are 4-bit general purpose output ports. Each port is provided with a latch, and its contents are held until they are rewritten by a program. Each bit is reset to "0" by initialize operation, but the contents being held cannot be referred to by the program.

The authorization/inhibit of content rewrite by the program of PO6 is controlled by SCAN bit of command register.

Command register SCAN	Object of content rewrite by program
0	Output to shift register (LCD segment data)
1	Output to PO6

Unlike PO5 and PO6 of TCP4630AP, those of TCP4632BF do not contain decode matrix, and PLA; therefore, there is difference between them in output timing.



PLA

A program can make reference of PLA by use of a decoder for display data or the like. If 4-bit BCD data is written in PLA (Register No.7) by a program, one of sixteen addresses is selected by 4-to-16 decoder within PLA, and the corresponding 8-bit data is written in PLA register.

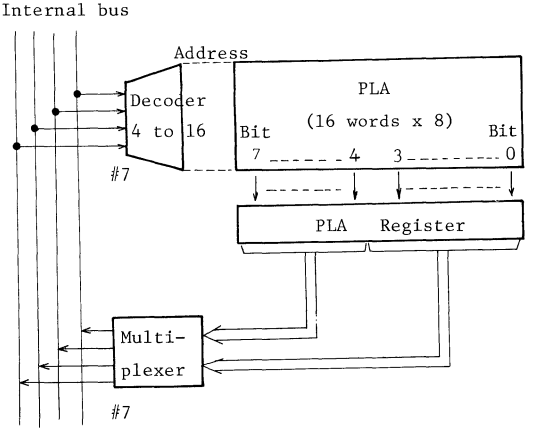
PLA contents of PLA register can be read out by executing the instruction for making reference of PLA. How to read out 8-bit data of PLA register varies with option designation of 1/3 duty or 1/4 duty. PLA register is not affected by reset operations.

(a) Designating 1/4 duty by options

The 8-bit data can be read out by executing the instruction for making reference of PLA register two times. In other words, 4-bit (bit 3 to 0) data on the lower level can be read out by the first execution of the instruction (LAR 7) for making reference of PLA

after BCD data has been written in PLA (SAR 7), and similarly 4-bit (bit 7 to 4) data on the higher level can be read out by the second execution of the same instruction.

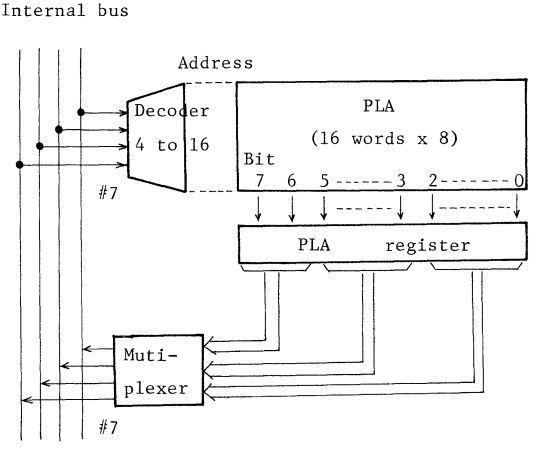
When the same data is read out again, and when PLA register is required to be updated, the reabout must be performed after BCD data has been written in the PLA over again.



(b) Designating 1/3 duty by options

The 8-bit data can be read out by executing the instruction for making reference of PLA register three times. In other words, 3-bit (bit 2 to 0) data on the lower level can be read out by the first execution of the instruction (LAR 7) for making reference of PAL after BCD data has been written in PLA (SAR 7), and similarly 3-bit (bit 5 to 3) data on the intermediate level can be read out by the second execution of the same instruction, and also 2-bit (bit 7 to 6) data on the higher level by the third execution of the same instruction, respectively.

While the reference instruction above mentioned is being executed, 1 bit (bit 3) on MSB side of the lower or intermediate level and 2 bits (bit 3 and 2) on MSB side of the higher level are always read out as zero. When the same data is read out again, and when PLA register is required to be updated, the readout is performed after BCD data has been written in the PLA over again.

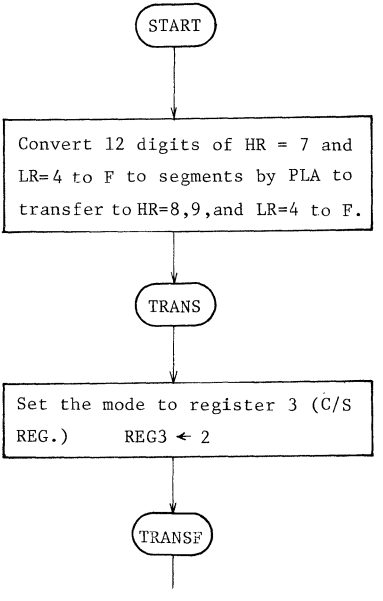


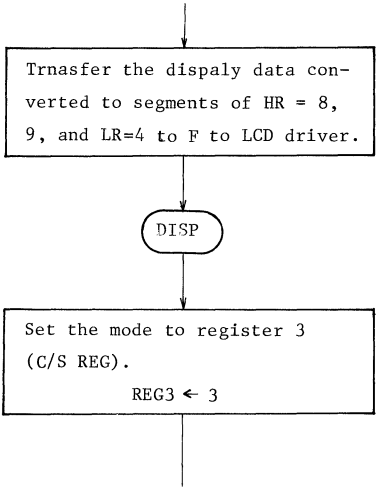
LCD DATA TRANSFER PROGRAM - EXAMPLE

LR / HR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7					1 Digit	2	3	4	5	6	7	8	9	10	11	12-digit
8					SEG23	21	19	17	15	13	11	9	7	5	3	SEG 1
9					SEG22	20	18	16	14	12	10	8	6	4	2	SEG 0

Example of a program which the data of HR = 7 and LR = 4 to F are displayed on LCD through segment conversion

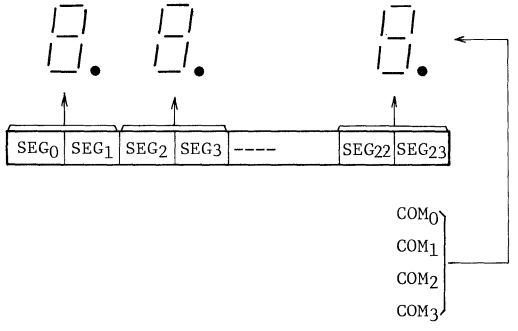
LCD: 1/4 duty, 12 digits (24 Seg.)





Setting of display mode

```
                    10   ;   ***   TCP4632BF LCD DATA TRANSFER PROGRAM
                    20   ;
0100                30               ORG   100H
0100  64            40   START:      LLI   4
0101  77            50   NEXT:       LHI   7
0102  04            60               LAM
0103  2F            70               SAR   7
0104  78            80               LHI   8
0105  17            90               LAR   7
0106  0C            100              SAM
0107  79            110              LHI   9
0108  17            120              LAR   7
0109  0C            130              SAM
010A  02            140              ICL
010B  06            150              LAL
010C  90            160              ADI   0
010D  D110          170              BCC   NEXT
010F  42            180  TRANS:      LAI   2
0110  2B            190              SAR   3     ;  DISP=1,SCAN=0  SET
0111  64            200              LLI   4
0112  78            210  TRANSF:     LHI   8
0113  04            220              LAM
0114  2E            230              SAR   6
0115  79            240              LHI   9
0116  04            250              LAM
0117  2E            260              SAR   6
0118  02            270              ICL
0119  06            280              LAL
011A  90            290              ADI   0
011B  D211          300              BCC   TRANSF
011D  43            310  DISP:       LAI   3
011E  2B            320              SAR   3     ;  DISP=SCAN=1  SET
                    330  ;
                    340  ;
```



TCP4632BF MASK OPTIONS

Oscillation frequency			OSC	TYP032 050 400K ceramic IFT					
Dividing ratio for internal clock			CP	02					
External timing output			CK	C1					
Counter	Divider 1 Input		PD	CP					
	Divider 3 Input		COUNTER PDR	PD2					
	Reset timing		PDR	N					
Counter Buffer	Buffer 0 Input		CO	PI60					
	Buffer 1 Input		COUNTER C1	RD7					
	Buffer 2 Input		BUFFER C2	RDA					
	Buffer 3 Input		C3	RDD					
H flag			HOLD	H					
Restart condition			RSTH	C3					
Input/Output port	Port 0		STD	D(PROG)	1 (OUT)				
Input/Output port	Port 2		P2	/F/(OUT)	/F/(OUT)	/0/(IN)	/0/(IN)	/0/(IN)	
	Port 4		P4	/F/(OUT)	/3/(IN/OUT)	/F/(OUT)	/3/(IN/OUT)	/0/(IN)	
Input resistance (Input port 5)			P15	0 (UP)	1 (DOWN)				
PLA (#7)	Line 0		PLA	PLA0	/ /				
	Line 1			PLA1	/ /				
	Line 2			PLA2	/ /				
	Line 3			PLA3	/ /				
	Line 4			PLA4	/ /				
	Line 5			PLA5	/ /				
	Line 6			PLA6	/ /				
	Line 7			PLA7	/ /				
	Line 8			PLA8	/ /				
	Line 9			PLA9	/ /				
	Line A			PLAA	/ /				
	Line B			PLAB	/ /				
	Line C			PLAC	/ /				
	Line D			PLAD	/ /				
	Line E			PLAE	/ /				
	Line F			PLAF	/ /				
Oscillation Stop Control	PI60		RSTX	N					
LCD Duty			DUT	4	3				

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V_{IN}	Input Voltage	-0.3 to V_{DD} +0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{DD} +0.3	V
P_D	Power Dissipation	400	mW
T_{sol}	Soldering Temperature·Time	260 (10 SEC)	°C
T_{slg}	Storage Temperature	-55 to +125	°C
T_{opr}	Operating Temperature	-20 to +70	°C

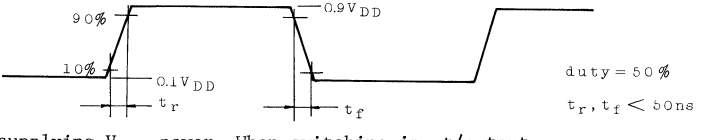
ALLOWABLE OPERATING CONDITIONS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	4 to 6	V
Ta	Ambient Temperature	-20 to +70	°C
I_{OUT}	Max. Output Current	±3	mA
f_x	X'tal Operating Frequency	40 to 400	kHz
t_{CY}	Cycle Time	10 to 100	μs
V_{LCD}	LCD Supply Voltage (V_{LCD} is with respect to V_{DD})	$-V_{DD}$ to -2.7	V

DC CHARACTERISTICS (Ta = −20 to +70°C, V_{DD} = 4 to 6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	(Note 1) TYP.	MAX.	UNIT
V_{IH}	Input High Voltage		V_{DD}x0.7	−	V_{DD}	V
V_{IHS}	Input High Voltage (Schmitt)		V_{DD}x0.85	−	V_{DD}	
V_{IHC}	Input High Voltage (x_{IN} Input)		V_{DD}x0.75	−	V_{DD}	
V_{IL}	Input Low Voltage		0	−	V_{DD}x0.3	
V_{ILS}	Input Low Voltage (Schmitt)		0	−	V_{DD}x0.15	
V_{ILC}	Input Low Voltage (X_{IN} Input)		0	−	V_{DD}x0.25	
I_{IH}	Input High Current	V_{DD}=6V, V_{IN}=6V	−	−	20	µA
I_{IL}	Input Low Current	V_{DD}=6V, V_{IN}=0V	−	−	−20	
R_{IN}	Input Resistance (PI_5)	V_{DD}=5V	75	150	350	kΩ
V_{OH}	Output High Voltage (Port)	V_{DD}=5V, Output open	4.7	4.9	−	V
V_{OL}	Output Low Voltage (Port)	V_{DD}=5V, Output open	−	0.1	0.3	
I_{OH}	Output High Current (P_1)	V_{DD}=4.5V, V_{OH}=2.4V	-0.7	−	−	mA
I_{OH2}	Output High Current (P_0,P_2,P_4,CK)	V_{DD}=4.5V, V_{OH}=2.4V	-0.35	−	−	
I_{OH3}	Output High Current (P_5,P_6)	V_{DD}=4.5V, V_{OH}=2.4V	-0.15	−	−	
I_{OL}	Output Low Current (P_1)	V_{DD}=4.5V, V_{OL}=0.45V	1.6	−	−	
I_{OL2}	Output Low Current (P_0,P_2,P_4,CK)	V_{DD}=4.5V, V_{OL}=0.45V	0.8	−	−	
I_{OL3}	Output Low Current (P_5,P_6)	V_{DD}=4.5V, V_{OL}=0.45V	0.4	−	−	
R_{OS3}, R_{OS0}	Output Impedance (SEG)	V_{DD}=5V, V_{DD}-V_{LCD}=3V (Note 5)	−	2	T.B.D	kΩ
R_{OC3}, R_{OC0}	Output Impedance (COM)	V_{OUT}=V_{LCD}+0.5V/ V_{DD}-0.5V	−	2	T.B.D	
R_{OS2}, R_{OS1}	Output Impedance (SEG)	V_{DD}=5V, V_{DD}-V_{LCD}=3V (Note 5)	−	20	T.B.D	
R_{OC2}, R_{OC1}	Output Impedance (COM)	V_{OUT}=3+0.5V/ 4−0.5V	−	20	T.B.D	
V_{OS1}	Output Intermediate Voltage (SEG,COM)	V_{DD}=5V, V_{DD}-V_{LCD}=3V	3 − 0.2	3	3 + 0.2	V
V_{OS2}			4 − 0.2	4	4 + 0.2	
I_{DDO}	V_{DD} Supply Current in Normal Operation	(Note 4) f_X = 400 kHz	−	600	T.B.D	µA
I_{DDH}	V_{DD} Supply Current in Hold operation		−	250	T.B.D	

Note 1) Typical values are at Ta=25°C and V_{DD}=5V.
2) Output characteristic excludes X_{OUT} terminal.
3) Output current at the time when other terminals than those to be tested are open.
4) Test conditions of current dissipation
V_{DD} = 6V, V_{IN} = V_{IH}/V_{IL}(all valid), PI_5 Open, C_L = 50pF
X_{IN} Input waveform



5) When supplying V_{LCD} power, When switching input/output.

OUTLINE DRAWINGS

Unit mm