

# TCS3490

## Color Light-to-Digital Converter

### General Description

The TCS3490 device provides color and IR (red, green, blue, clear and IR) light sensing. The color sensing provides for improved accuracy lux and color temperature measurements typically used to adjust the backlight intensity and correct the display color gamut. Additionally it can be used for light source type detection as it reports the IR content of the light.

*For further understanding in regards to the contents of the datasheet, please refer to the Reference Guide located at the end of the document.*

### Key Benefits & Features

The benefits and features of TCS3490, Color Light-to-Digital Converter are listed below:

**Figure 1:**  
Added Value of Using TCS3490

| Benefits                                    | Features  |
|---|---|
| Single Device Integrated Optical Solution   | <ul style="list-style-type: none"> <li>• RGBC and ALS Support</li> <li>• Power Management Features</li> </ul>                     |
| Color Temperature and Ambient Light Sensing | <ul style="list-style-type: none"> <li>• Programmable Gain &amp; Integration Time</li> <li>• 1,000,000:1 Dynamic Range</li> </ul> |
| Equal Response to 360 degree Incident Light | Circular Segmented RGBC Photodiode  |
| Ideal for Operation Behind Dark Glass       | Very High Sensitivity   |
| Light Source Detection                      | RGBC + IR sensor  |

### Applications

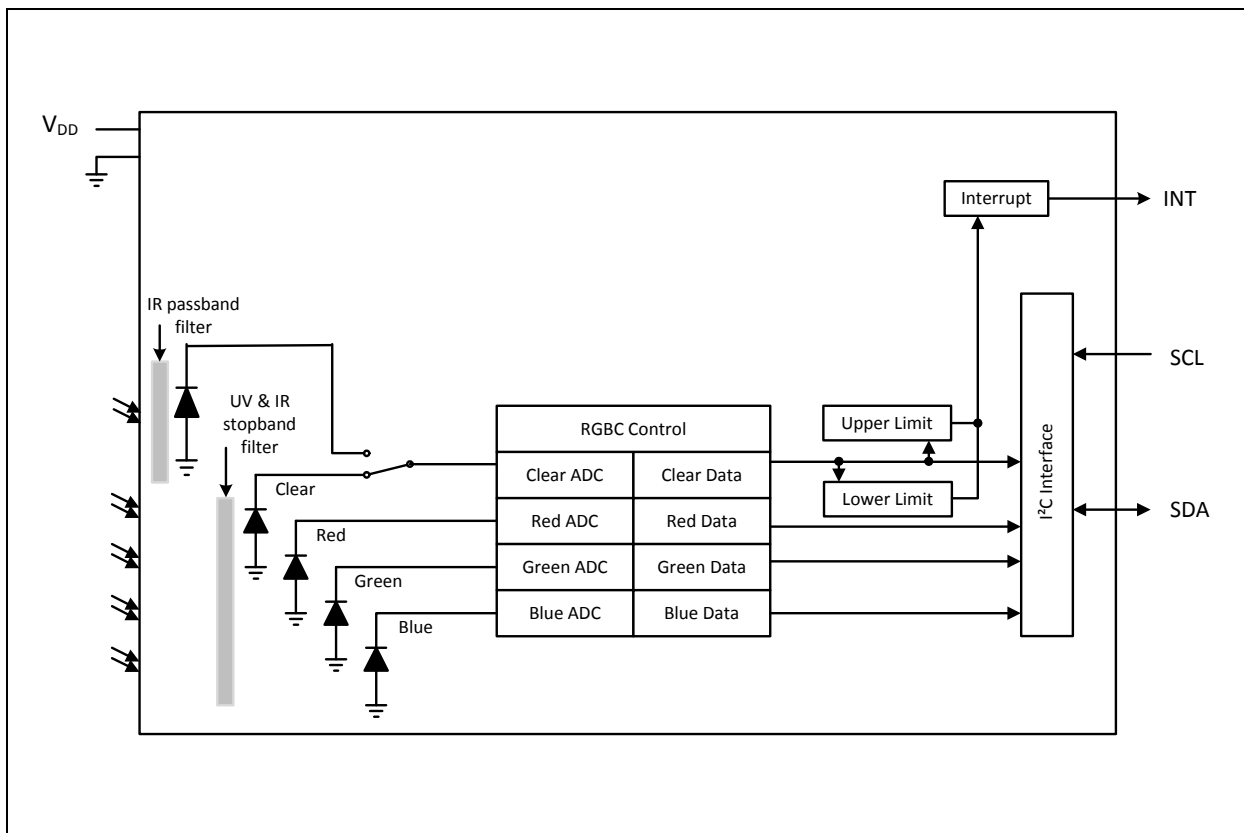
The TCS3490 applications include:

- Ambient Light Sensing
- Color Temperature Sensing
- Industrial Process Control
- Medical Diagnostics

### Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:  
TCS3490 Block Diagram

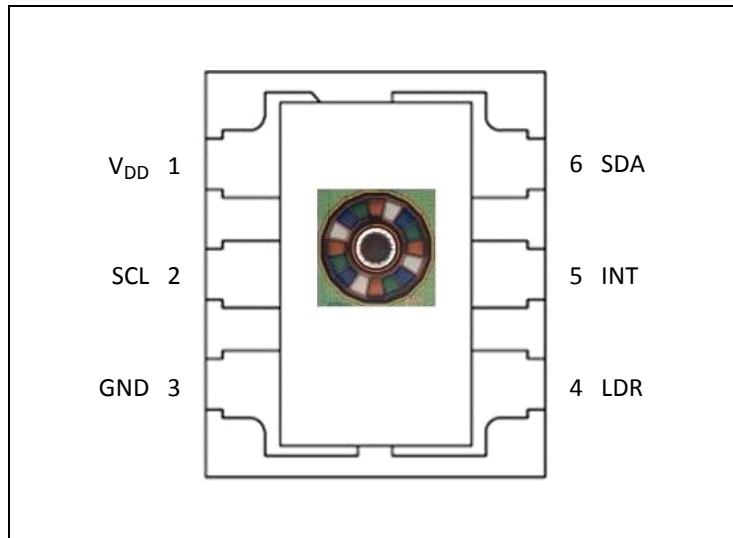


## Pin Assignment

The TCS3490 pin assignments are described below.

**Figure 3:  
Pin Diagram**

**Pin Diagram (Top View):**  
Package FN Dual Flat No-Lead.  
Package Drawing is not to scale.



**Figure 4:  
Pin Description**

| Pin Number | Pin Name        | Description  |
|------------|-----------------|--|
| 1          | V <sub>DD</sub> | Supply voltage   |
| 2          | SCL             | I <sup>2</sup> C serial clock input terminal             |
| 3          | GND             | Power supply ground. All voltages are referenced to GND. |
| 4          | LDR             | Connect to GND   |
| 5          | INT             | Interrupt — open drain output (active low)               |
| 6          | SDA             | I <sup>2</sup> C serial data I/O terminal – open drain   |

## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
Absolute Maximum Ratings

| Parameter                            | Min  | Max  | Units | Comments                             |
|--------------------------------------|------|------|-------|--------------------------------------|
| Supply voltage, $V_{DD}$             |      | 3.8  | V     | All voltages are with respect to GND |
| Input terminal voltage               | -0.5 | 3.8  | V     |                                      |
| Output terminal voltage              | -0.5 | 3.8  | V     |                                      |
| Output terminal voltage (LDR)        | -0.5 | 3.8  | V     |                                      |
| Output terminal current (SDA, INT)   | -1   | 20   | mA    |                                      |
| Storage temperature range, $T_{stg}$ | -40  | 85   | °C    |                                      |
| ESD tolerance, human body model      |      | 2000 | V     |                                      |

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Recommended Operating Conditions

| Symbol   | Parameter                                     | Min | Typ | Max | Units |
|----------|---|-----|-----|-----|-------|
| $V_{DD}$ | Supply voltage                                | 2.7 | 3   | 3.6 | V     |
| $T_A$    | Operating free-air temperature <sup>(1)</sup> | -40 |     | 70  | °C    |

**Note(s) and/or Footnote(s):**

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

**Figure 7:**  
Operating Characteristics,  $V_{DD}=3V$ ,  $T_A=25^\circ C$  (unless otherwise noted)

| Symbol     | Parameter                           | Conditions                                 | Min          | Typ | Max          | Units   |
|------------|-------------------------------------|--|--------------|-----|--------------|---------|
| $I_{DD}$   | Supply current                      | Active                                     |              | 235 | 330          | $\mu A$ |
|            |                                     | Wait state                                 |              | 60  |              |         |
|            |                                     | Sleep state - no I <sup>2</sup> C activity |              | 1.0 | 10           |         |
| $V_{OL}$   | INT, SDA output low voltage         | 3 mA sink current                          | 0            |     | 0.4          | V       |
|            |                                     | 6 mA sink current                          | 0            |     | 0.6          |         |
| $I_{LEAK}$ | Leakage current, SDA, SCL, INT pins |  | -5           |     | 5            | $\mu A$ |
|            | Leakage current, LDR pins           |  | -10          |     | 10           | $\mu A$ |
| $V_{IH}$   | SCL, SDA input high voltage         | TCS34901, TCS34905                         | $0.7 V_{DD}$ |     |              | V       |
|            |                                     | TCS34903, TCS34907                         | 1.26         |     |              |         |
| $V_{IL}$   | SCL, SDA input low voltage          | TCS34901, TCS34905                         |              |     | $0.3 V_{DD}$ | V       |
|            |                                     | TCS34903, TCS34907                         |              |     | 0.54         |         |

**Figure 8:**  
**Optical Characteristics (Clear channel),  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$ , AGAIN = 16x, ATIME = 0xF6**

| Parameter                                 | Test Conditions                    | Clear Channel |      |      | Unit                                     |
|---|------------------------------------|---------------|------|------|--|
|   |                                    | Min           | Typ  | Max  |  |
| R <sub>e</sub><br>Irradiance responsivity | $\lambda_D = 465 \text{ nm}^{(1)}$ | 39.5          | 49.4 | 59.3 | counts/<br>( $\mu\text{W}/\text{cm}^2$ ) |
|   | $\lambda_D = 525 \text{ nm}^{(2)}$ | 52.4          | 65.5 | 78.6 |  |
|   | $\lambda_D = 615 \text{ nm}^{(3)}$ | 61.2          | 76.5 | 91.8 |  |

**Figure 9:**  
**Optical Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$**

| Parameter  | Test Conditions                    | Red / Clear Channel |      | Green / Clear Channel |     | Blue / Clear Channel |     |
|--|------------------------------------|---------------------|------|-----------------------|-----|----------------------|-----|
|  |                                    | Min                 | Max  | Min                   | Max | Min                  | Max |
| Color ADC Count<br>value ratio:<br>Color / Clear | $\lambda_D = 465 \text{ nm}^{(1)}$ | 0%                  | 15%  | 10%                   | 42% | 70%                  | 90% |
|  | $\lambda_D = 525 \text{ nm}^{(2)}$ | 4%                  | 25%  | 60%                   | 85% | 10%                  | 45% |
|  | $\lambda_D = 615 \text{ nm}^{(3)}$ | 80%                 | 110% | 0%                    | 14% | 5%                   | 24% |

**Note(s) and/or Footnote(s):**

1. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 465 \text{ nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 22 \text{ nm}$ .
2. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 525 \text{ nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 35 \text{ nm}$ .
3. The 615 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength  $\lambda_D = 615 \text{ nm}$ , spectral halfwidth  $\Delta\lambda_{1/2} = 15 \text{ nm}$ .

**Figure 10:**  
**RGBC Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$ , AGAIN = 16x, AEN = 1 (unless otherwise noted)**

| Parameter                                 | Conditions                                     | Min | Typ  | Max   | Units                 |
|---|--|-----|------|-------|-----------------------|
| Dark ADC count value                      | $E_e = 0$ , AGAIN = 64x,<br>ATIME=0xDC (100ms) | 0   | 1    | 3     | counts                |
|   |  | 0   |      | 1     | counts <sup>(1)</sup> |
| ADC integration time step size            | ATIME = 0xFF                                   |     | 2.78 |       | ms                    |
| ADC number of integration steps           |  | 1   |      | 256   | steps                 |
| ADC counts per step                       | ATIME = 0xFF                                   | 0   |      | 1024  | counts                |
| ADC count value                           | ATIME = 0xC0                                   | 0   |      | 65535 | counts                |
| Gain scaling, relative to 1x gain setting | AGAIN = 4x                                     | 3.8 | 4    | 4.2   | x                     |
|   | AGAIN = 16x                                    | 15  | 16   | 17    |                       |
|   | AGAIN = 64x                                    | 62  | 64   | 66    |                       |

**Note(s) and/or Footnote(s):**

1. Based on typical 3-sigma distribution. Not 100% tested.

**Figure 11:**  
**Wait Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$ , WEN = 1 (unless otherwise noted)**

| Parameter      | Conditions   | Min | Typ  | Max | Units |
|----------------|--------------|-----|------|-----|-------|
| Wait step size | WTIME = 0xFF |     | 2.78 |     | ms    |

**Timing Characteristics**

The timing characteristics of TCS3490 are given below.

**Figure 12:**  
AC Electrical Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

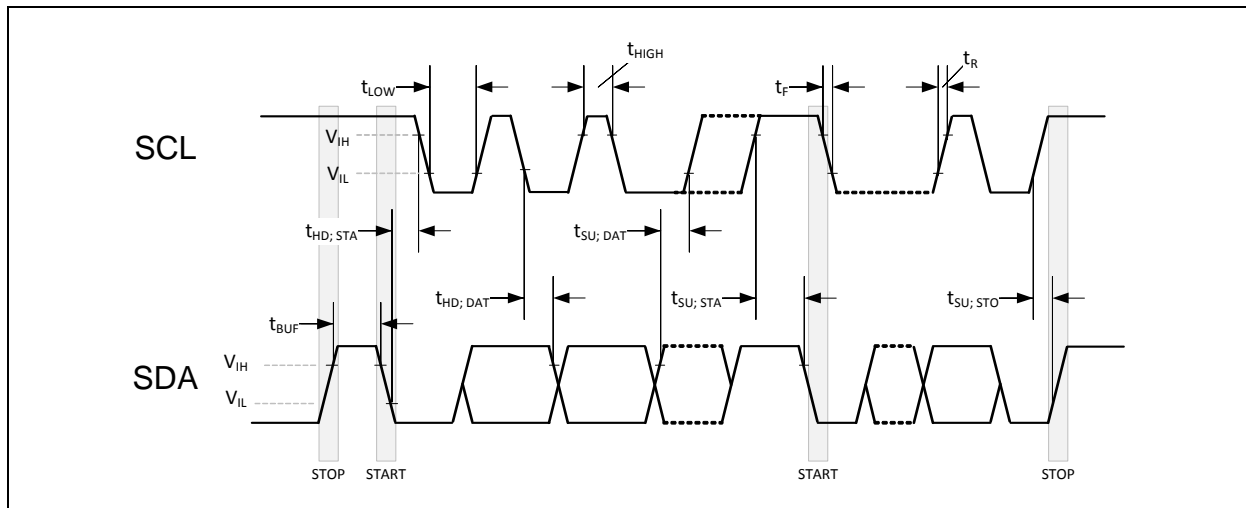
| Parameter <sup>(1)</sup> | Conditions   | Min | Max | Unit    |
|--------------------------|--|-----|-----|---------|
| $f_{SCL}$                | Clock frequency (I <sup>2</sup> C only)  | 0   | 400 | kHz     |
| $t_{BUF}$                | Bus free time between start and stop condition   | 1.3 |     | $\mu s$ |
| $t_{HS;STA}$             | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 |     | $\mu s$ |
| $t_{SU;STA}$             | Repeated start condition setup time  | 0.6 |     | $\mu s$ |
| $t_{SU;STO}$             | Stop condition setup time  | 0.6 |     | $\mu s$ |
| $t_{HD;DAT}$             | Data hold time   | 60  |     | ns      |
| $t_{SU;DAT}$             | Data setup time  | 100 |     | ns      |
| $t_{LOW}$                | SCL clock low period   | 1.3 |     | $\mu s$ |
| $t_{HIGH}$               | SCL clock high period  | 0.6 |     | $\mu s$ |
| $t_F$                    | Clock/data fall time   |     | 300 | ns      |
| $t_R$                    | Clock/data rise time   |     | 300 | ns      |
| $C_i$                    | Input pin capacitance  |     | 10  | pF      |

**Note(s) and/or Footnote(s):**

- 1. Specified by design and characterization; not production tested.

**Timing Diagram**

**Figure 13:**  
Parameter Measurement Information





## Typical Operating Characteristics

Figure 14:  
Spectral Responsivity

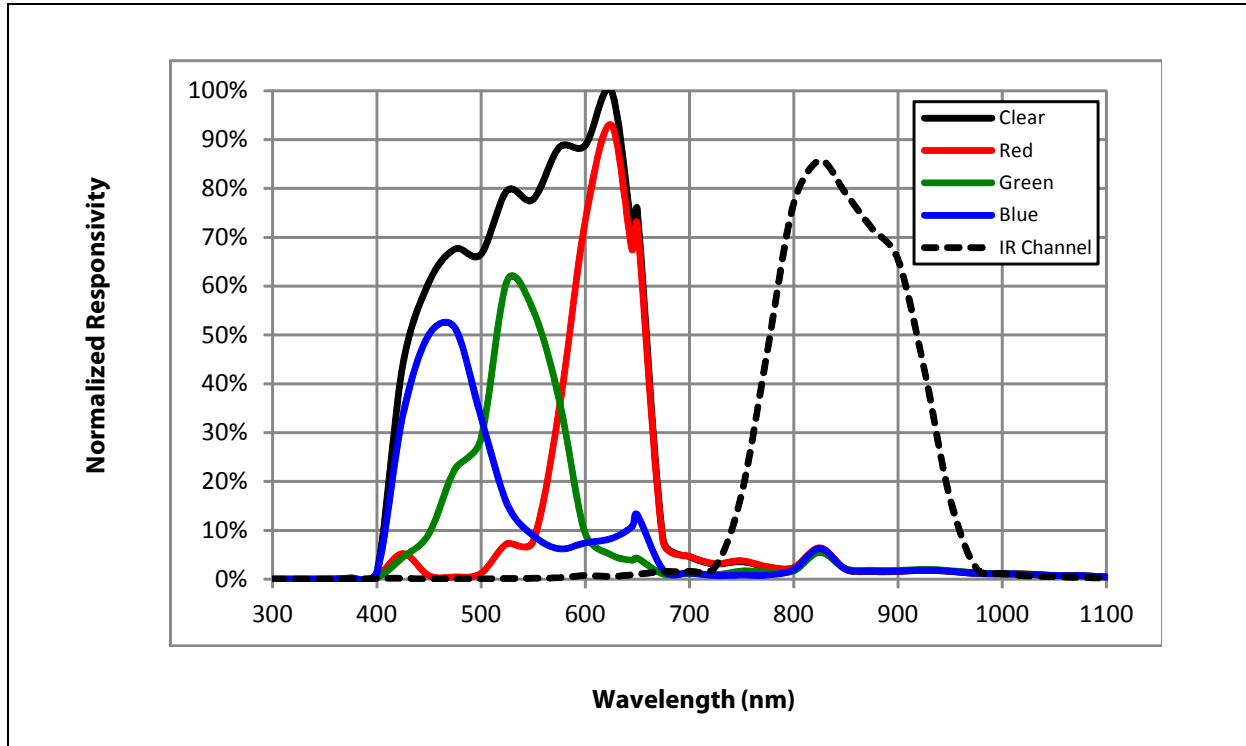


Figure 15:  
Normalized Responsivity vs. Angular Displacement

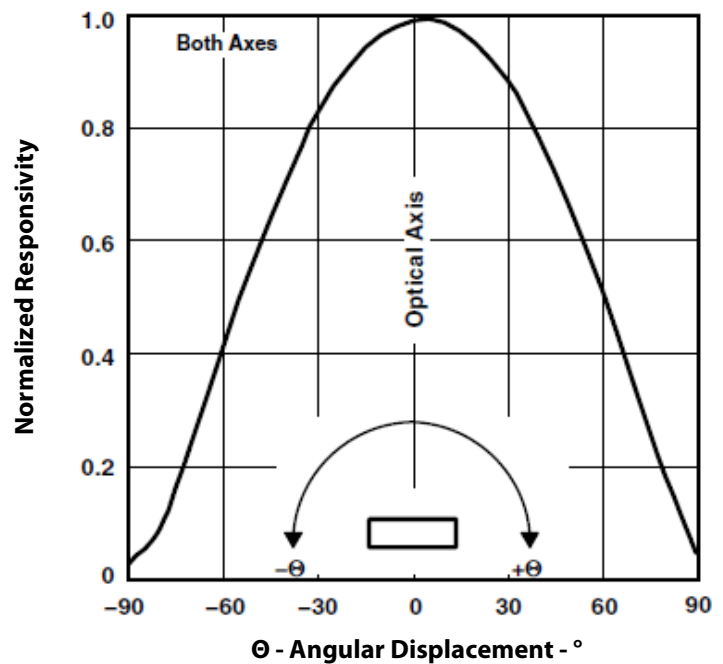
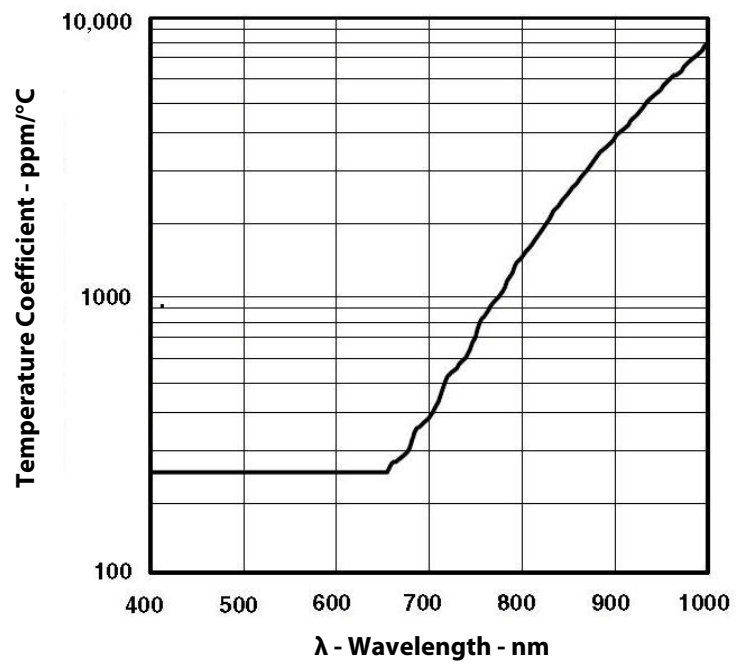


Figure 16:  
Responsivity Temperature Coefficient



## Functional Description

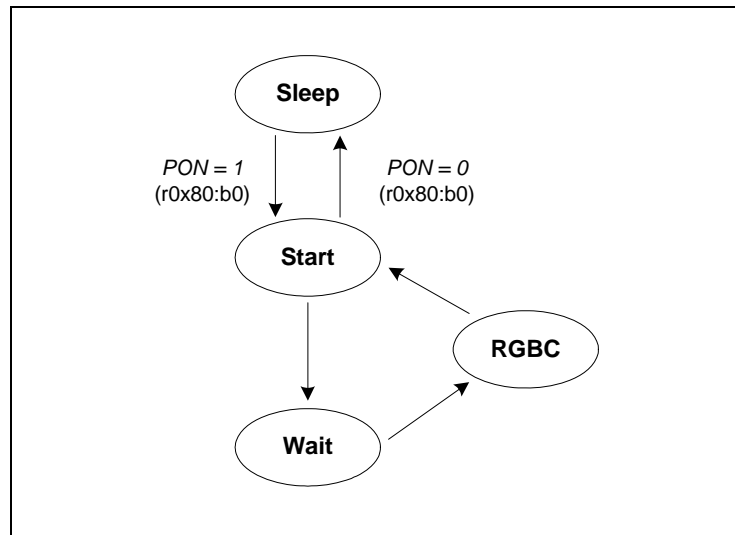
The TCS3490 device provides ambient light sensing and color temperature sensing. The internal state machine manages the operation of the device. It controls the ALS functionality and power down modes. Average power consumption is managed via control of variable endurance low power wait cycles.

The interrupt feature improves system efficiency by eliminating the need to poll the sensor. Three interrupt sources (ALS, ALS saturation) can activate the open drain output pin. Each interrupt source is enabled independently. ALS interrupts appear when upper or lower thresholds are exceeded for a consecutive number of sample readings.

The advanced digital color light sensor portion of the TCS3490 contains a segmented circular photodiode array used for color measurements. This architecture provides stable color sensing independent of the incident angle of light. Four integrating analog-to-digital converters (ADCs) integrate light energy from photodiodes simultaneously. The advanced digital color light sensor portion of the TCS3490 contains a segmented circular photodiode array used for color measurements. This architecture provides stable color sensing independent of the incident angle of light. Four integrating analog-to-digital converters (ADCs) integrate light energy from photodiodes simultaneously.

**Figure 17:**  
**Simplified ALS State Machine**

Communication with the device is accomplished through a fast (up to 400 kHz) two wire I<sup>2</sup>C serial bus for easy connection to a microcontroller or embedded controller. The device typically draws only 235µA in color operation and 1uA during power down.



## Register Description

The device is controlled and monitored by registers accessed through the I<sup>2</sup>C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in the figure below.

**Figure 18:**  
Register Map

| Address | Register Name | R/W | Register Function                        | Reset Value                 |
|---------|---------------|-----|--|-----------------------------|
| 0x80    | ENABLE        | R/W | Enables states and interrupts            | 0x00                        |
| 0x81    | ATIME         | R/W | RGBC integration time                    | 0xFF                        |
| 0x83    | WTIME         | R/W | Wait time                                | 0xFF                        |
| 0x84    | AILTL         | R/W | Clear interrupt low threshold low byte   | 0x00                        |
| 0x85    | AILTH         | R/W | Clear interrupt low threshold high byte  | 0x00                        |
| 0x86    | AIHTL         | R/W | Clear interrupt high threshold low byte  | 0x00                        |
| 0x87    | AIHTH         | R/W | Clear interrupt high threshold high byte | 0x00                        |
| 0x8C    | PERS          | R/W | Interrupt persistence filter             | 0x00                        |
| 0x8D    | CONFIG        | R/W | Configuration                            | 0x40                        |
| 0x8F    | CONTROL       | R/W | Gain control register                    | 0x00                        |
| 0x90    | AUX           | R/W | Auxiliary control register               | 0x00                        |
| 0x91    | REVID         | R   | Revision ID                              | Rev                         |
| 0x92    | ID            | R   | Device ID                                | 84h for TCS34901 & TCS34905 |
|         |               |     |  | 87h for TCS34903 & TCS34907 |
| 0x93    | STATUS        | R   | Device status                            | 0x00                        |
| 0x94    | CDATAL        | R   | Clear / IR channel low data register     | 0x00                        |
| 0x95    | CDATAH        | R   | Clear / IR channel high data register    | 0x00                        |
| 0x96    | RDATAH        | R   | Red ADC low data register                | 0x00                        |
| 0x97    | RDATAH        | R   | Red ADC high data register               | 0x00                        |

| Address | Register Name | R/W | Register Function             | Reset Value |
|---------|---------------|-----|-------------------------------|-------------|
| 0x98    | GDATA_L       | R   | Green ADC low data register   | 0x00        |
| 0x99    | GDATA_H       | R   | Green ADC high data register  | 0x00        |
| 0x9A    | BDATA_L       | R   | Blue ADC low data register    | 0x00        |
| 0x9B    | BDATA_H       | R   | Blue ADC high data register   | 0x00        |
| 0xC0    | IR            | R/W | Access IR Channel             | 0x00        |
| 0xE4    | IFORCE        | W   | Force Interrupt               | 0x00        |
| 0xE6    | CICLEAR       | W   | Clear channel interrupt clear | 0x00        |
| 0xE7    | AICLEAR       | W   | Clear all interrupts          | 0x00        |

### Enable Register (ENABLE 0 x 80)

The Enable Register is used primarily to power the device on/off, and enable functions and interrupts.

**Figure 19:**  
Enable Register

|          |     |          |      |     |          |     |     |
|----------|-----|----------|------|-----|----------|-----|-----|
| 7        | 6   | 5        | 4    | 3   | 2        | 1   | 0   |
| Reserved | SAI | Reserved | AIEN | WEN | Reserved | AEN | PON |

| Field    | Bits | Description  |
|----------|------|--|
| Reserved | 7    | <b>Reserved.</b> Write as 0.   |
| SAI      | 6    | <b>Sleep After Interrupt.</b> When asserted, the device will power down at the end of a RGBC cycle if an interrupt is generated.   |
| Reserved | 5    | <b>Reserved.</b> Write as 0.   |
| AIEN     | 4    | <b>ALS Interrupt Enable.</b> When asserted permits ALS interrupts to be generated, subject to the persist filter.  |
| WEN      | 3    | <b>Wait Enable.</b> This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.  |
| Reserved | 2    | Reserved. Write as 0.  |
| AEN      | 1    | <b>ADC Enable.</b> This bit activates the four-channel (RGBC) ADC. Writing a 1 enables the ADC. Writing a 0 disables the ADC. When IBEN is set, the proximity pulse will not be output to the LDR pin. |

| Field | Bits | Description  |
|-------|------|--|
| PON   | 0    | <b>Power ON.</b> This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator and puts the part into a low power sleep mode. During reads and writes over the I <sup>2</sup> C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON. |

**RGBC Integration Time Register (ATIME 0x81)**

The ATIME register controls the internal integration time of the RGBC channel ADCs. Upon power up, the RGBC time register is set to 0xFF.

The maximum (or saturation) count value can be calculated based upon the integration time cycles as follows:

$$\text{min [CYCLES * 1024, 65535]}$$

**Figure 20:**  
RGBC Integration Time Register

| Field | Bits | Description |        |         |           |
|-------|------|-------------|--------|---------|-----------|
|       |      | Value       | Cycles | Time    | Max Count |
| ATIME | 7:0  | 0xFF        | 1      | 2.78 ms | 1024      |
|       |      | 0xF6        | 10     | 27.8 ms | 10240     |
|       |      | 0xDB        | 37     | 103 ms  | 37888     |
|       |      | 0xC0        | 64     | 178 ms  | 65535     |
|       |      | 0x00        | 256    | 712 ms  | 65535     |

### Wait Time Register (WTIME 0x83)

The WTIME controls the amount of time in a low power mode. It is set 2.78 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2’s complement number. Upon power up, the wait time register is set to 0xFF.

**Figure 21:**  
Wait Time Register

| Field | Bits | Description    |           |                |                |
|-------|------|----------------|-----------|----------------|----------------|
|       |      | Register Value | Wait Time | Time (WLONG=0) | Time (WLONG=1) |
| WTIME | 7:0  | 0xFF           | 1         | 2.78 ms        | 0.03 sec       |
|       |      | 0xAB           | 85        | 236 ms         | 2.84 sec       |
|       |      | 0x00           | 256       | 712 ms         | 8.54 sec       |

**Note:** The wait time register should be configured before AEN is asserted.

### Clear Channel Interrupt Threshold Register (0x84 - 0x87)

The Clear Channel Interrupt Threshold Registers provide 16 bit values to be used as the high and low thresholds for comparison to the 16 bit CDATA values. If AIEN (r0x80:b4) is enabled and CDATA is not between AILT and AIHT for the number of consecutive samples specified in APERS (r0x8C:b[3:0]) an interrupt is asserted on the interrupt pin.

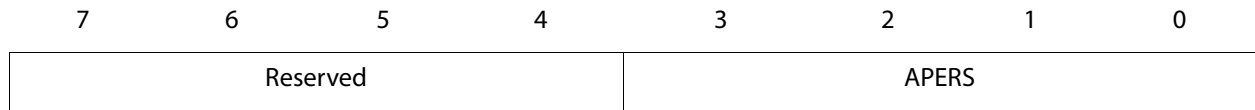
**Figure 22:**  
Clear Channel Interrupt Threshold Registers

| Register | Address | Bits | Description                             |
|----------|---------|------|---|
| AILTL    | 0x84    | 7:0  | Clear Channel low threshold lower byte  |
| AILTH    | 0x85    | 7:0  | Clear Channel low threshold upper byte  |
| AIHTL    | 0x86    | 7:0  | Clear Channel high threshold lower byte |
| AIHTH    | 0x87    | 7:0  | Clear Channel high threshold upper byte |

### Interrupt Register (0x8C)

The interrupt register controls the interrupt capabilities of the device.

**Figure 23:**  
Interrupt Register



| Field    | Bits                               | Description   |   |
|----------|------------------------------------|---|---|
| Reserved | 7:4                                | Reserved. Write as 0.   |   |
| APERS    | 3:0                                | <b>Clear Interrupt persistence.</b> Controls rate of Clear channel interrupt to the host processor. |   |
|          |                                    | Field Value   | Persistence                             |
|          |                                    | 0000  | Every RGBC cycle generates an interrupt |
|          |                                    | 0001  | Any value outside of threshold range    |
|          |                                    | 0010  | 2 consecutive values out of range       |
|          |                                    | 0011  | 3 consecutive values out of range       |
|          |                                    | 0100  | 5 consecutive values out of range       |
|          |                                    | 0101  | 10 consecutive values out of range      |
|          |                                    | 0110  | 15 consecutive values out of range      |
|          |                                    | 0111  | 20 consecutive values out of range      |
|          |                                    | 1000  | 25 consecutive values out of range      |
|          |                                    | 1001  | 30 consecutive values out of range      |
|          |                                    | 1010  | 35 consecutive values out of range      |
|          |                                    | 1011  | 40 consecutive values out of range      |
|          |                                    | 1100  | 45 consecutive values out of range      |
|          |                                    | 1101  | 50 consecutive values out of range      |
|          |                                    | 1110  | 55 consecutive values out of range      |
| 1111     | 60 consecutive values out of range |   |   |



### Configuration Register (CONFIG 0x8D)

The CONFIG register sets the wait long time. The registers is set 0x40 at power up.

**Figure 24:**  
Configuration Register



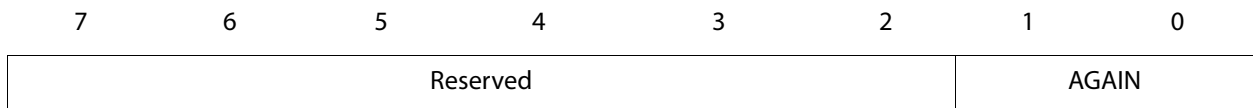
| Field                   | Bits | Description  |
|-------------------------|------|--|
| Reserved                | 7    | Reserved. Write as 0.  |
| Reserved <sup>(1)</sup> | 6    | Reserved. Write as 1.  |
| Reserved                | 5:2  | Reserved. Write all as 0.  |
| WLONG                   | 1    | <b>Wait Long.</b> When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register. |
| Reserved                | 0    | Reserved. Write as 0.  |

**Note(s) and/or Footnote(s):**

1. Bit 6 is reserved and has to be programmed = 1.

### Control Register (CONTROL 0x8F)

**Figure 25:**  
Control Register



| Field    | Bits | Description               |                        |
|----------|------|---------------------------|------------------------|
| Reserved | 7:2  | Reserved. Write all as 0. |                        |
| AGAIN    | 1:0  | RGBC Gain Control.        |                        |
|          |      | <b>FIELD VALUE</b>        | <b>RGBC GAIN VALUE</b> |
|          |      | 00                        | 1X Gain                |
|          |      | 01                        | 4X Gain                |
|          |      | 10                        | 16X Gain               |
|          |      | 11                        | 64X Gain               |

### Auxiliary Register (AUX 0x90)

The AUX register enables the ALS saturation detection interrupt. If ASIEN = 1 and an interrupt occurs it is cleared by accessing the Clear Interrupt registers at 0XE6 or 0XE7.

**Figure 26:**  
Auxiliary Register

|          |   |       |          |   |   |   |   |
|----------|---|-------|----------|---|---|---|---|
| 7        | 6 | 5     | 4        | 3 | 2 | 1 | 0 |
| Reserved |   | ASIEN | Reserved |   |   |   |   |

| Field    | Bits | Description                                    |
|----------|------|--|
| Reserved | 7:6  | Reserved. Write all as 0.                      |
| ASIEN    | 5    | 0 disables, 1 enables ALS Saturation Interrupt |
| Reserved | 4:0  | Reserved                                       |

### Revision ID Register (REVID 0x91)

This read-only register identifies the die revision level.

**Figure 27:**  
Revision ID Register

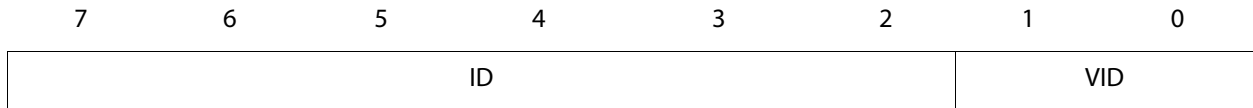
|      |       |      |          |       |   |   |   |
|------|-------|------|----------|-------|---|---|---|
| 7    | 6     | 5    | 4        | 3     | 2 | 1 | 0 |
| ALSF | PROXF | IRBF | Reserved | RevID |   |   |   |

| Field    | Bits | Description                           |
|----------|------|---------------------------------------|
| ALSF     | 7    | ALS Functionality (1=Yes, 0=No)       |
| PROXF    | 6    | Proximity Functionality (1=Yes, 0=No) |
| IRBF     | 5    | IRBeam Functionality (1=Yes, 0=No)    |
| Reserved | 4    | Reserved                              |
| RevID    | 3:0  | Wafer die revision level              |

### ID Register (ID 0x92)

The read-only ID register provides the device identification.

**Figure 28:**  
ID Register

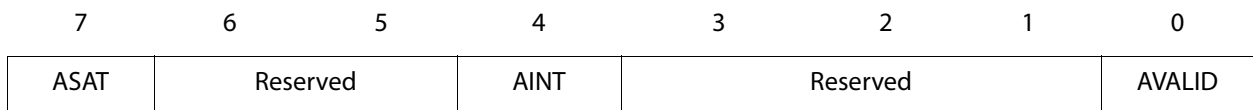


| Field | Bits | Description  |
|-------|------|--|
| ID    | 7:2  | Device Identification = 100001                             |
| VID   | 1:0  | 00b for TCS34901 & TCS34905<br>11b for TCS34903 & TCS34907 |

### Status Register (STATUS 0x93)

The read-only STATUS register provides the internal status of the device.

**Figure 29:**  
Status Register



| Field    | Bits | Description  |
|----------|------|--|
| ASAT     | 7    | <b>ALS Saturation.</b> When asserted, the analog sensor was at the upper end of its dynamic range. The bit can be de-asserted by sending a clear channel interrupt command (0xE6 CICLEAR) or by disabling the ALS ADC (AEN=0). Depending on cover glass transmissivity, gain configuration (CONTROL:AGAIN) and/or accumulation time (ATIME) should be adjusted to avoid this situation. This bit triggers an interrupt if ASIEN in AUX is set. |
| Reserved | 6:5  | Reserved   |
| AINT     | 4    | <b>ALS Interrupt.</b> This bit triggers an interrupt if AEN in ENABLE is set.  |
| Reserved | 3:1  | Reserved   |
| AVALID   | 0    | <b>RGBC Valid.</b> Indicates that the RGBC cycle has completed since AEN was asserted.   |

### RGBC Data Registers (0x94 - 0x9B)

Clear, red, green, and blue data is stored as 16-bit values. The read sequence must read byte pairs (low followed by high) starting on an even address boundary (0x94, 0x96, 0x98, or 0x9A) inside the RGBC Data Register block. When the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

**Figure 30:**  
RGBC Data Registers

| Register | Address | Bits | Description               |
|----------|---------|------|---------------------------|
| CDATAL   | 0x94    | 7:0  | Clear / IR data low byte  |
| CDATAH   | 0x95    | 7:0  | Clear / IR data high byte |
| RDATAH   | 0x96    | 7:0  | Red data high byte        |
| RDATAH   | 0x97    | 7:0  | Red data low byte         |
| GDATAH   | 0x98    | 7:0  | Green data high byte      |
| GDATAH   | 0x99    | 7:0  | Green data low byte       |
| BDATAH   | 0x9A    | 7:0  | Blue data high byte       |
| BDATAH   | 0x9B    | 7:0  | Blue data low byte        |

### IR Register (0xC0)

Access to IR channel; allows mapping of IR channel on clear channel.

**Figure 31:**  
IR Register

|    |          |   |   |   |   |   |   |
|----|----------|---|---|---|---|---|---|
| 7  | 6        | 5 | 4 | 3 | 2 | 1 | 0 |
| IR | Reserved |   |   |   |   |   |   |

| Field    | Bits | Description  |
|----------|------|--|
| IR       | 7    | <b>IR Sensor access.</b> If this bit is set the clear channel reports the measurement from the IR sensor (center diode). |
| Reserved | 6:0  | <b>Reserved.</b> Always write as '0'.  |

**Clear Interrupt Registers (0xE3, 0xE7)**

Any dummy data byte (0x00 recommended) written to the specified register will clear the indicated interrupt.

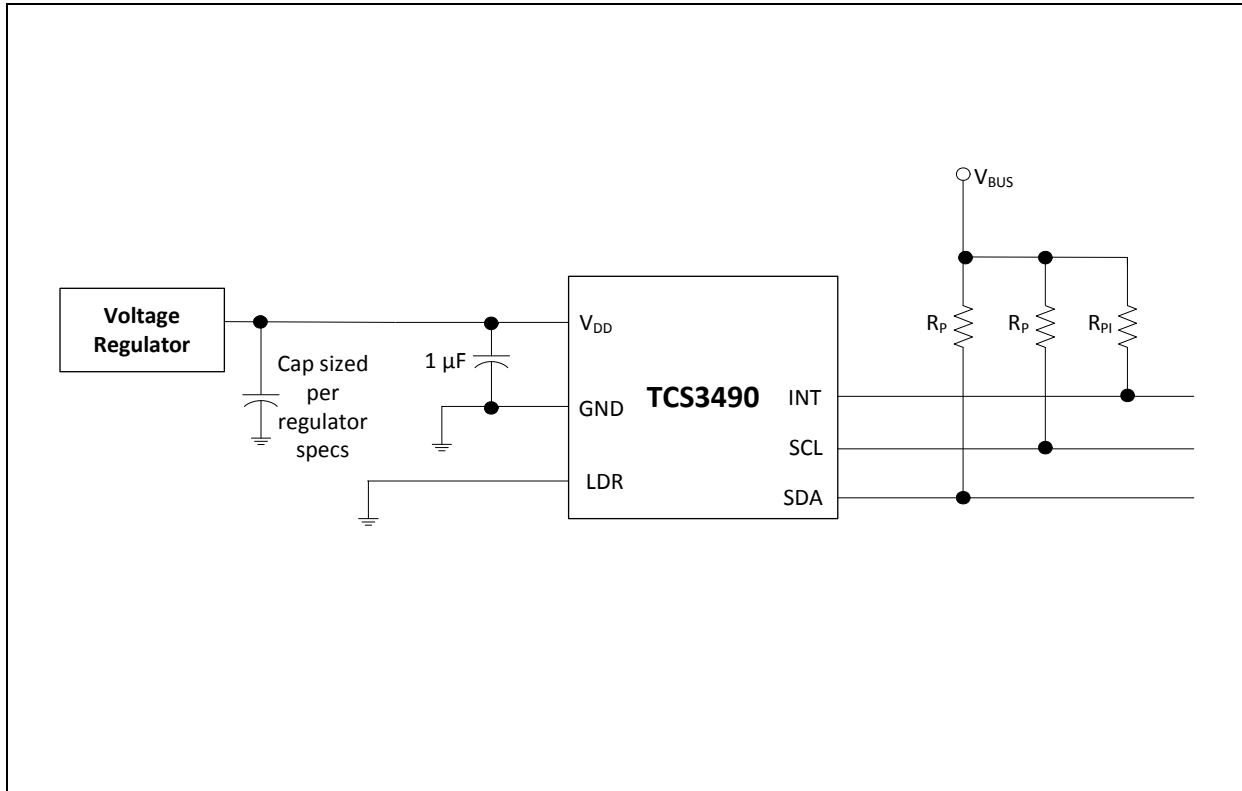
**Figure 32:**  
**Clear Interrupt Registers**

| Register | Address | Bits | Description                               |
|----------|---------|------|---|
| IFORCE   | 0xE4    | 7:0  | Forces an interrupt (any value)           |
| CICLEAR  | 0xE6    | 7:0  | Clear channel interrupt clear (any value) |
| AICLEAR  | 0xE7    | 7:0  | Clears all interrupts (any value)         |

## Power Supply Considerations

Place a 1- $\mu\text{F}$  low-ESR decoupling capacitor as close as possible to the  $V_{\text{DD}}$  pin.

**Figure 33:**  
Typical Application Hardware Circuit



$V_{\text{BUS}}$  in the above figures refers to the I<sup>2</sup>C bus voltage which is either  $V_{\text{DD}}$  or 1.8 V. Be sure to apply the specified I<sup>2</sup>C bus voltage shown in the “[Ordering & Contact Information](#)” on page 29 for the specific device being used.

The I<sup>2</sup>C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor ( $R_{\text{P}}$ ) value is a function of the I<sup>2</sup>C bus speed, the I<sup>2</sup>C bus voltage, and the capacitive load. The ams EVM running at 400 kbps, uses 1.5-k $\Omega$  resistors. A 10-k $\Omega$  pull-up resistor ( $R_{\text{PI}}$ ) can be used for the interrupt line.

## PCB Pad Layout

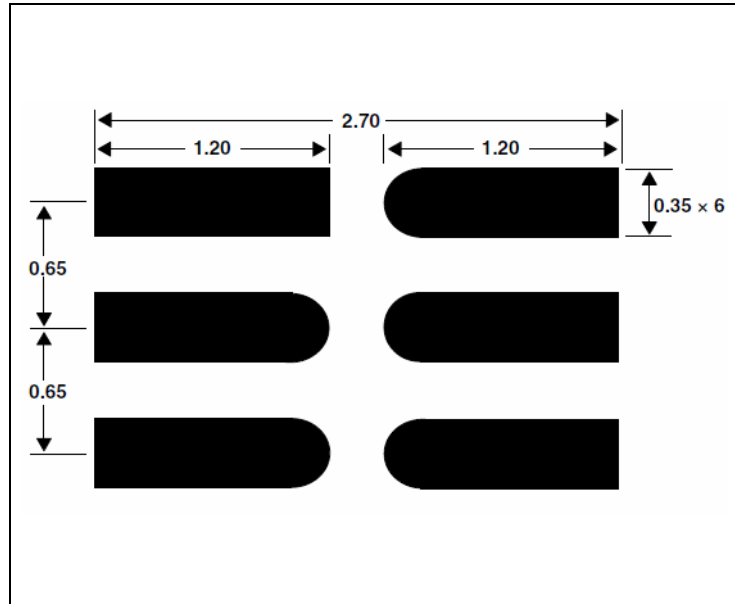
Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

**Figure 34:**  
**Suggested PCB Layout**

Suggested land pattern based on the IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package.

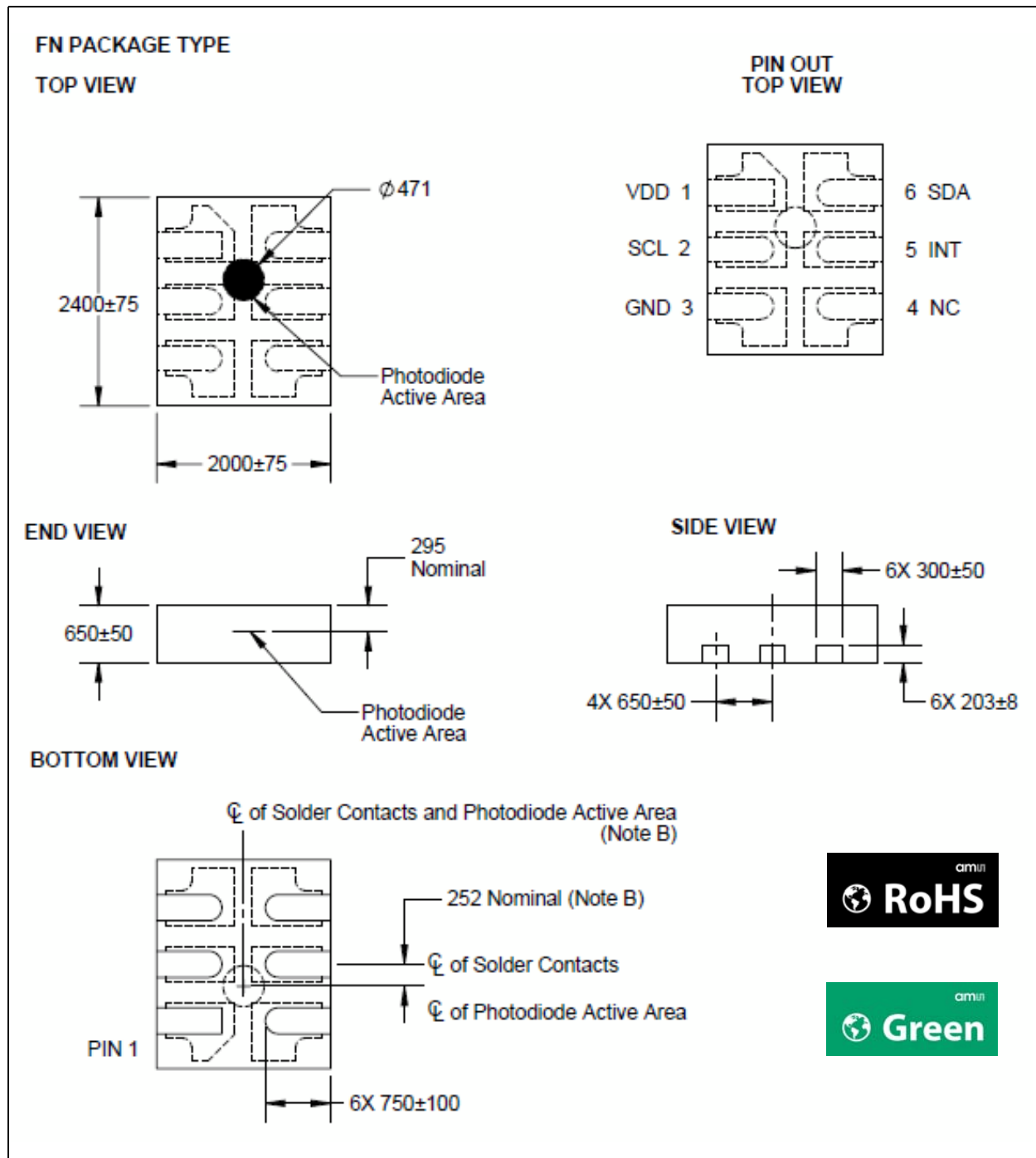
Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.



## Package Drawings & Markings

Figure 35:  
IC Package Mechanical



**Note(s) and/or Footnote(s):**

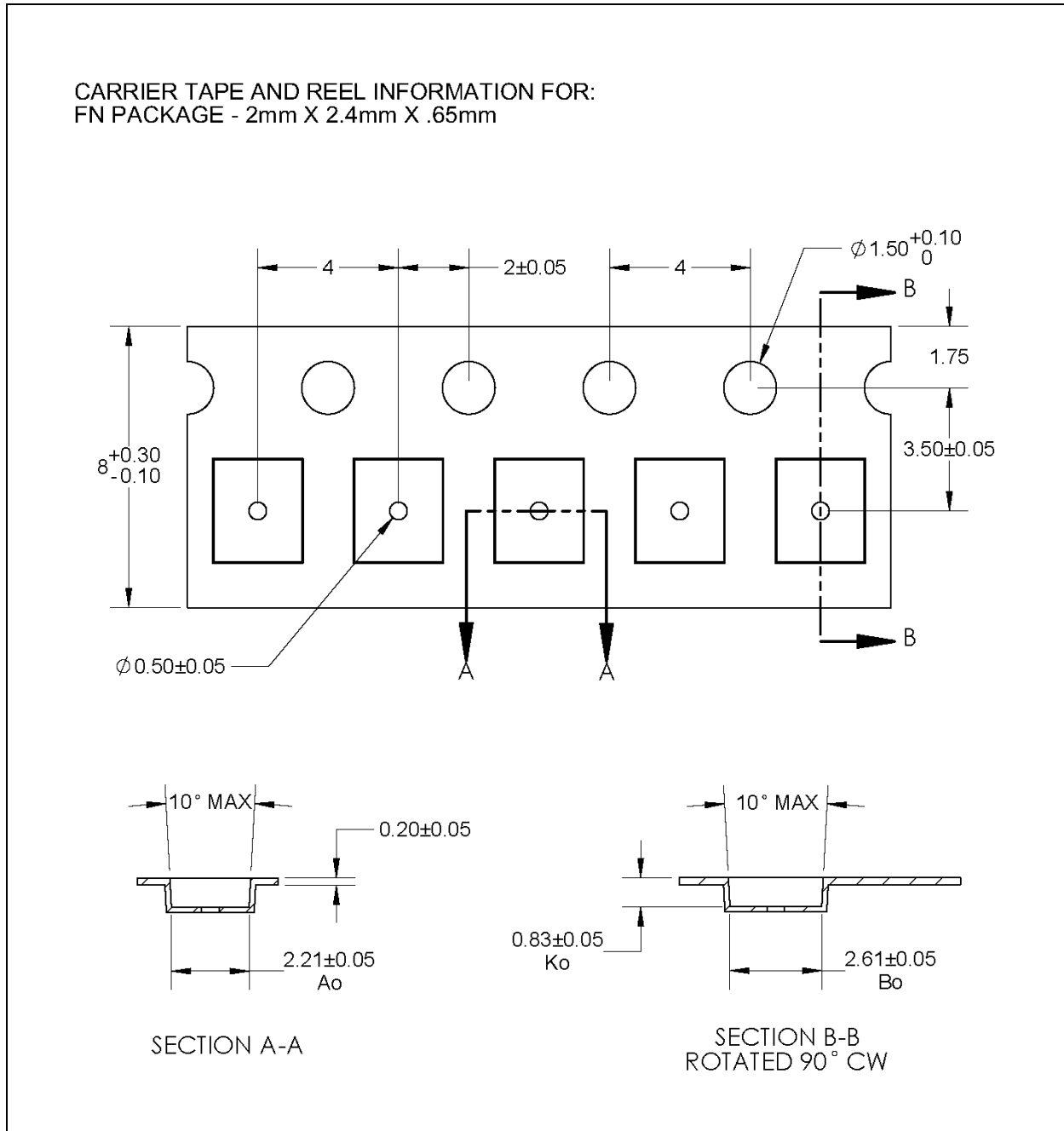
1. All linear dimensions are in micrometers. Dimension tolerance is  $\pm 20 \mu\text{m}$  unless otherwise noted.
2. The die is centered within the package within a tolerance of  $\pm 75 \mu\text{m}$ .
3. Package top surface is molded with an electrically non-conductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is Copper Alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.



**Package Mechanical Data**

The package mechanical data of TCS3490 is given below.

**Figure 36:**  
IC Package Mechanical



**Note(s) and/or Footnote(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is  $\pm 0.10$  mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 330 millimeters in diameter and contains 2500 parts.
5. Packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.
8. The device pin 1 is located in the upper left corner inside the T&R pockets.

## Soldering & Storage Information

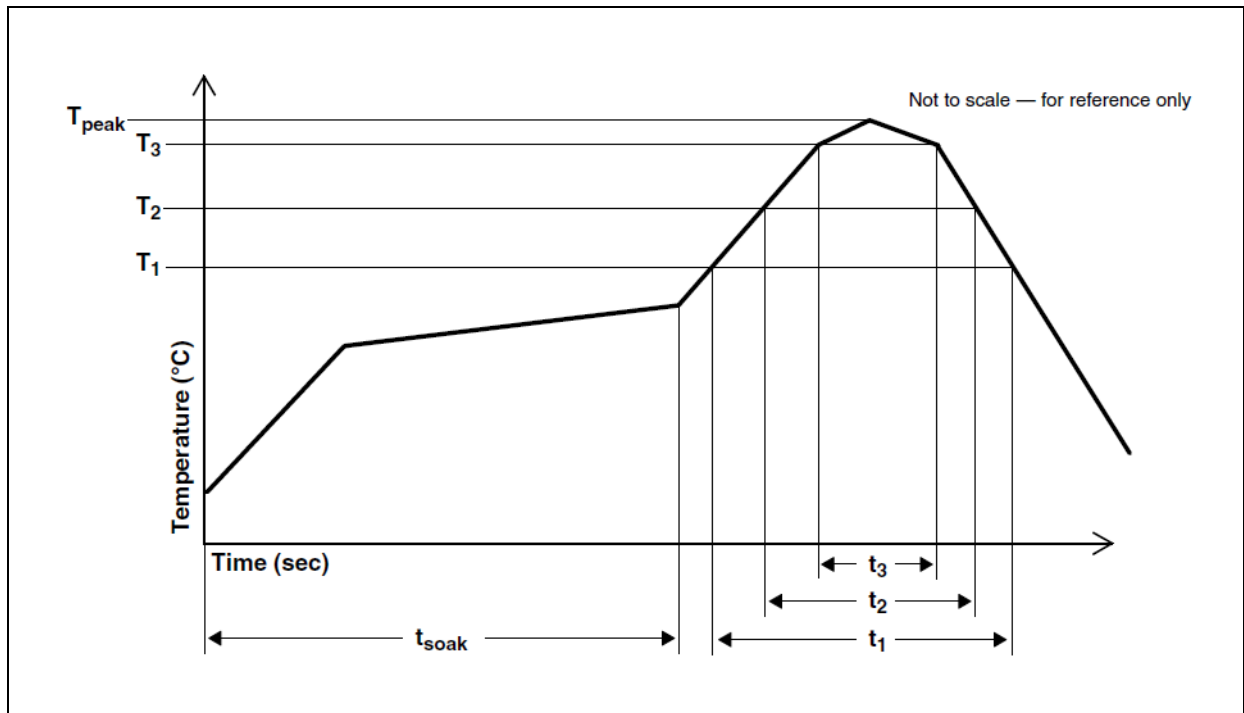
The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 37:**  
Solder Reflow Profile

| Parameter                                  | Reference  | Device         |
|--|------------|----------------|
| Average temperature gradient in preheating |            | 2.5 °C/sec     |
| Soak time                                  | $t_{soak}$ | 2 to 3 minutes |
| Time above 217 °C ( $T_1$ )                | $t_1$      | Max 60 sec     |
| Time above 230 °C ( $T_2$ )                | $t_2$      | Max 50 sec     |
| Time above $T_{peak} - 10$ °C ( $T_3$ )    | $t_3$      | Max 10 sec     |
| Peak temperature in reflow                 | $T_{peak}$ | 260 °C         |
| Temperature gradient in cooling            |            | Max -5 °C/sec  |

**Figure 38:**  
Solder Reflow Profile Graph



## Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

## Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

## Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

## Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

## RoHS Compliant & ams Green Statement

**RoHS:** The term RoHS compliant means that ams products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

**ams Green (RoHS compliant and no Sb/Br):** ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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**Ordering & Contact Information**

The device is packaged in a small OFN (Optical FN) package which is 2mm x 2.4mm.

**Figure 39:**  
**Ordering Information**

| Ordering Code             | Address | Interface   | Delivery Form |
|---------------------------|---------|---|---------------|
| TCS34901FN <sup>(1)</sup> | 0x39    | I <sup>2</sup> C V <sub>BUS</sub> = V <sub>DD</sub> Interface | FN-6          |
| TCS34903FN                | 0x39    | I <sup>2</sup> C bus = 1.8V Interface                         | FN-6          |
| TCS34905FN <sup>(1)</sup> | 0x29    | I <sup>2</sup> C V <sub>BUS</sub> = V <sub>DD</sub> Interface | FN-6          |
| TCS34907FN                | 0x29    | I <sup>2</sup> C bus = 1.8V Interface                         | FN-6          |

**Note(s) and/or Footnote(s):**

1. Contact ams for availability.

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**Headquarters**

ams AG  
Tobelbaderstrasse 30  
8141 Unterpremstaetten  
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: [www.ams.com](http://www.ams.com)

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