TFT LCD Specification

Model Name: TD016SHEC1

Customer Signature
Date

This technical specification is subjected to change without notice.

Table of Contents

Record of Revision

Rev	Issued Date	Description
1.00	Oct 20, 2004	New Release
1.01	Dec 10, 2004	Update Brightness

1. FEATURES

The 1.6”(4.06cm) LCD module is an active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used. Vertical drivers are built on the panel.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	1.6 (4.06)	Inch (cm)
Display Type	Trans-flective	
Active Area (HxV)	28.608 x 28.608	mm
Number of Dots (HxV)	128 x RGB x 128	dot
Dot Pitch (HxV)	0.0745 x 0.2235	mm
Color Arrangement	RGB Stripe	
Color Numbers	65 K / 262 K	
Outline Dimension (HxVxT) *	32.61 x 37.21 x 4.2	mm
Weight	7.8 +- 0.5	g

* Exclude protrusions.

3. INPUT/OUTPUT TERMINALS(USE i80 System)

Pin No	Symbol	I/O	Description	Remark
1	VCC(+2.8V)	I	System Power Supply	
2	/CS	I	Chip Select	
3	/WR	I	Write (Write/Read)	
4	/RD	I	Read (Enable)	
5	GND	-	Ground	
6	NC	--	NC	
7	D0	I	Data0	
8	D1	I	Data1	
9	D2	I	Data2	
10	D3	I	Data3	
11	D4	I	Data4	
12	D5	I	Data5	
13	D6	I	Data6	
14	D7	I	Data7	
15	NC	--	NC	
16	D8	I	Data8	
17	D9	I	Data9	
18	D10	I	Data10	
19	D11	I	Data11	
20	D12	I	Data12	
21	D13	I	Data13	
22	D14	I	Data14	
23	D15	I	Data15	
24	/RESET	I	RESET	
25	RS	I	Command (L)/Data (H)	
26	LED-	I	LED (Cathode)	
27	NC	--	NC	
28	LED+	I	LED (Anode)	
29	NC	--	NC	
30	NC	--	NC	

4. ABSOLUTE MAXIMUM RATINGS

VSS=0V

Item	Symbol	Min	MAX	Unit	Remark
Input voltage	VI	--	+4.2	V	Note 4-1
Back Light Forward Current	I_F	--	+25	mA	
Operating temperature	Topr	-20	+70	℃	
Storage temperature	Tstg	-30	+80	℃	

Note 4-1 :VI：D0~D15, /CS, RS, /WR, /RD, HOST, Reset

5. ELECTRICAL CHARACTERISTICS

5.1. Driving TFT LCD Panel

VSS=0V, Ta=25℃

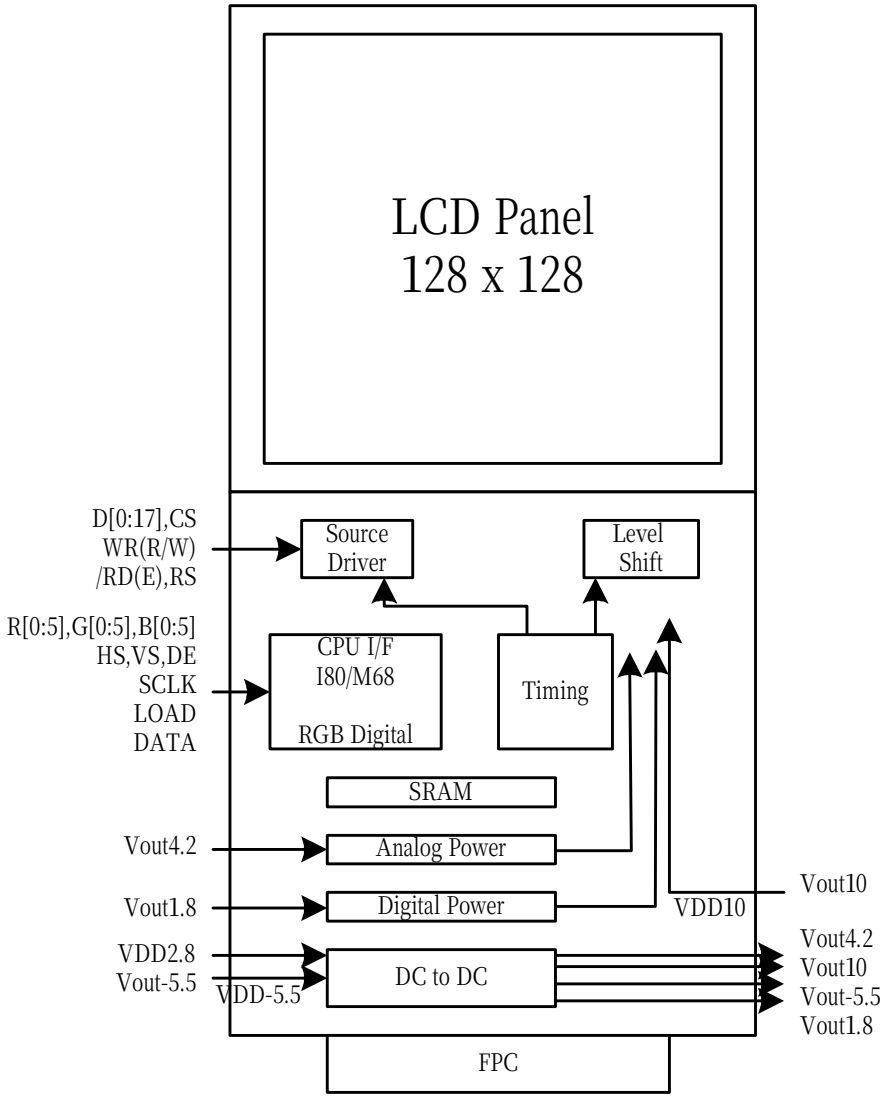
Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VCC	2.7	2.8	3.0	V	
Logic Input High Level		VIH	2.7	2.8	3.0	V	
Logic Input Low Level		VIL	0	--	0.25	V	
System Current	Normal mode	Isc	--	0.96	1.43	mA	Note 5-1
	8 Color mode		--	0.32	0.43	mA	
	8 Color Partial mode		--	0.21	0.3	mA	

Note: 5-1: Power consumption test condition

a. Input voltage(VCC): 2.8V

b. Test pattern:

5.2. Driving TFT LCD Panel Block Diagram



5.3. Driving Backlight

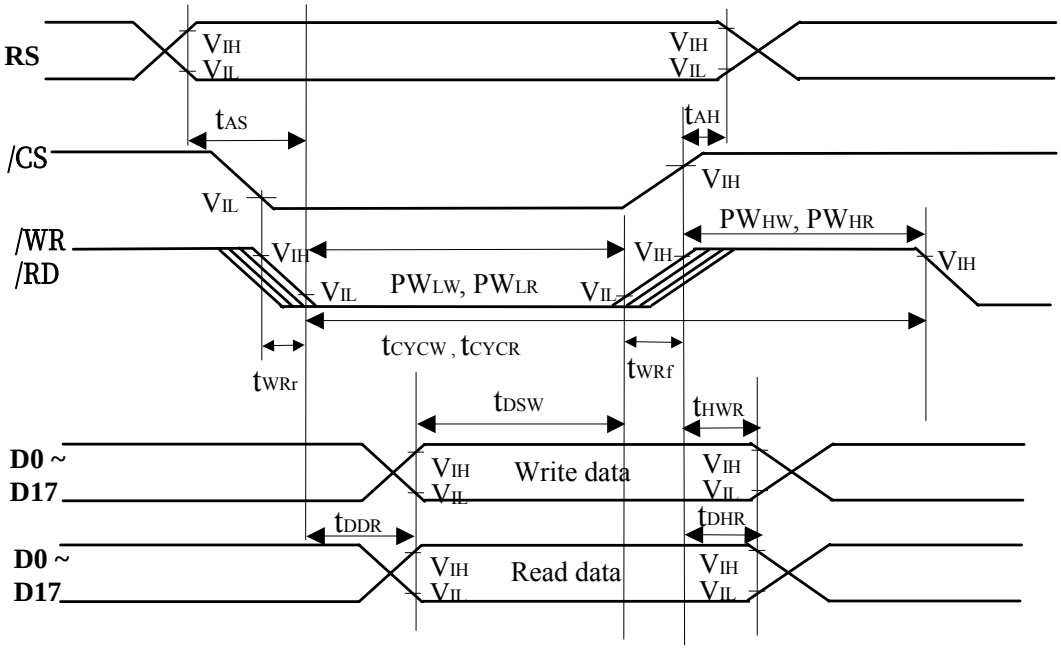
Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	15	25	mA	Note 5-2
Forward Current Voltage	V_F	--	7.2	8.4	V	
Backlight Power Consumption	W_{BL}	--	108	--	mW	

Note 5-2: Backlight driving circuit is recommend as the fix current circuit.

6. TIMING CHART

6.1 I80 system CPU interface



Item	Symbol	Min	Typ	Max	unit
/WR , /RD cycle time	t_{CYCW}	250	—	—	ns
	t_{CYCR}	500	—	—	ns
/WR , /RD pulse width low	PW_{LW}	40	—	—	ns
	PW_{LR}	250	—	—	ns
/WR , /RD pulse width high	PW_{HW}	70	—	—	ns
	PW_{HR}	200			
Pulse rise/fall time	t_{WRr}, t_{WRf}	—	—	25	ns
Setup time (RS to /CS , /WR , /RD)	t_{AS}	10	—	—	ns
Chip select hold time	t_{AH}	5	—	—	ns
Data input setup time	t_{DSW}	60	—	—	ns
Data input hold time	t_{HWR}	15	—	—	ns
Data output setup time	t_{DDR}	—	—	200	ns
Data output hold time	t_{DHR}	5	—	—	ns

6.2 Input Timing signal data mapping

6.2.1 CPU Interface 16 bit mode

Signal data

BODR : 00

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	—	—	—	—	—	—	—	—	—	—	—	—	—	—	R5	R4
2nd cycle	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BODR : 01

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2
2nd cycle	B1	B0	—	—	—	—	—	—	—	—	—	—	—	—	—	—

BODR : 1x

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Command data

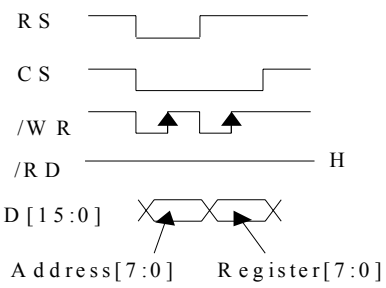
1-time write mode	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st cycle	—	—	—	—	—	—	—	—	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	—	—	—	—	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0

Input timing waveform

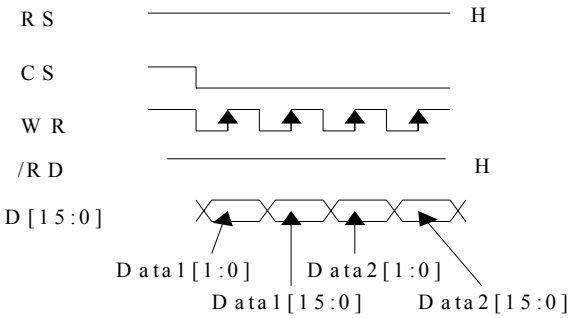
BODR:00

i80 System

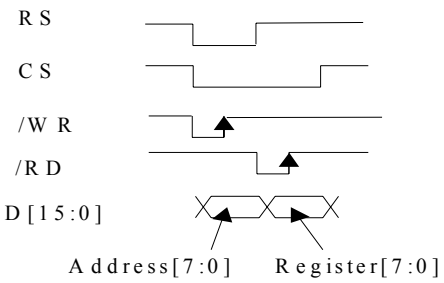
1)command (Write mode)



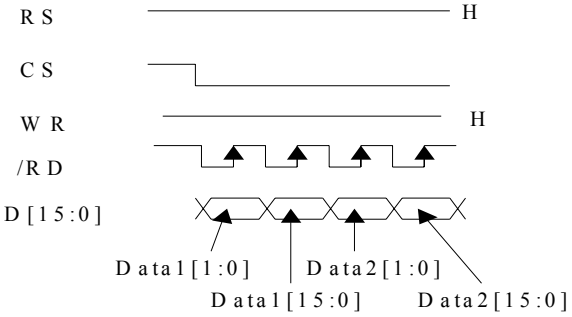
2)data (Write mode)



3)command (Read mode)



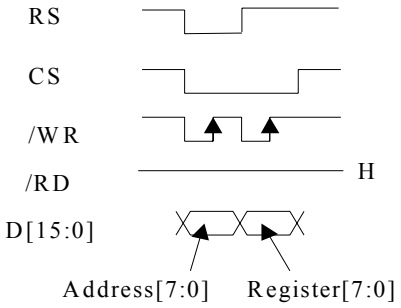
4)data (Read mode)



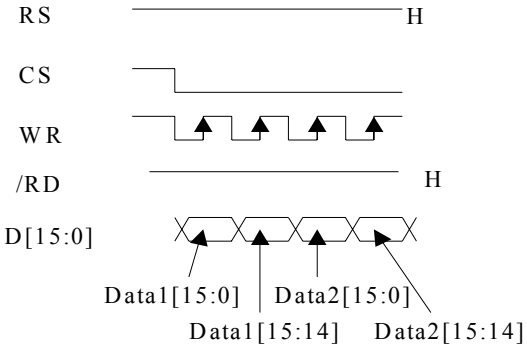
BODR:01

i80 System

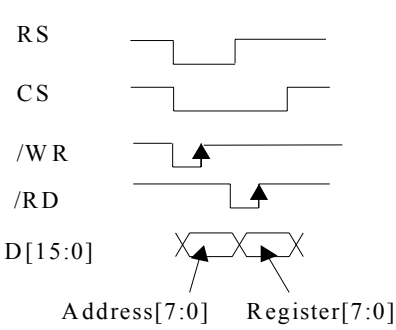
1)command (Write mode)



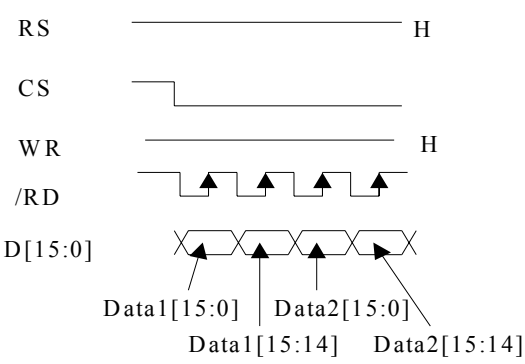
2)data (Write mode)

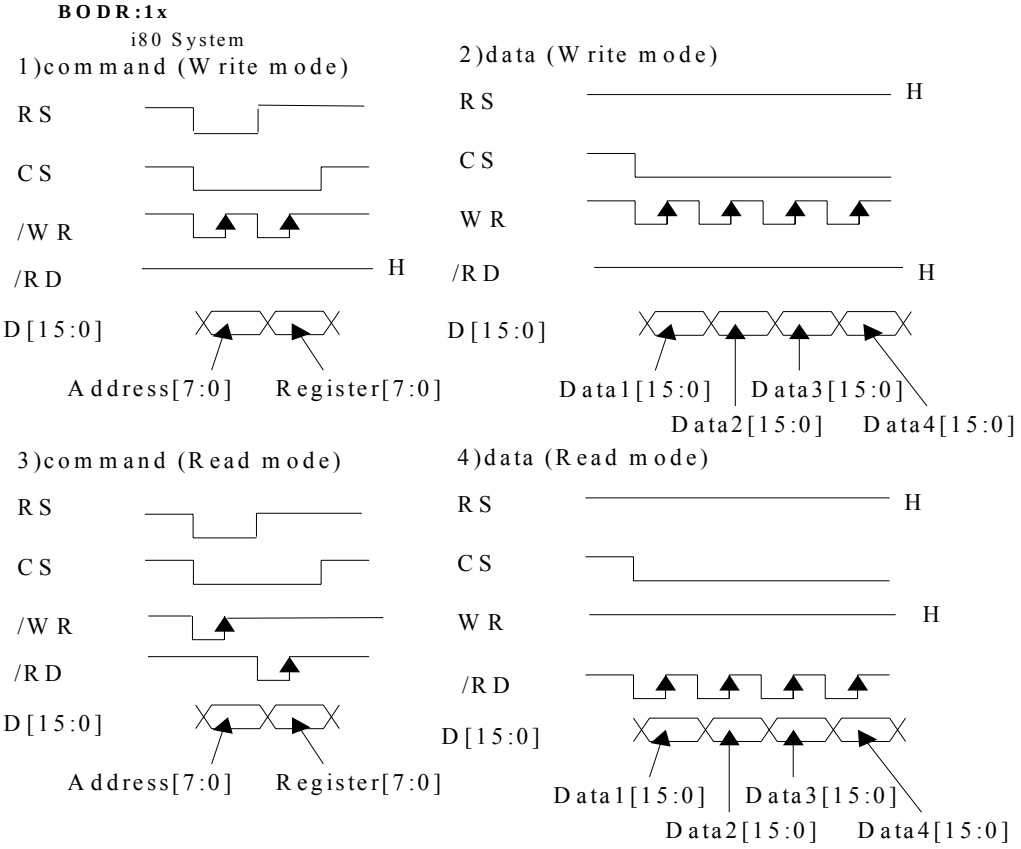


3)command (Read mode)



4)data (Read mode)





6.2.2 CPU Interface 18 bit mode

Signal data

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

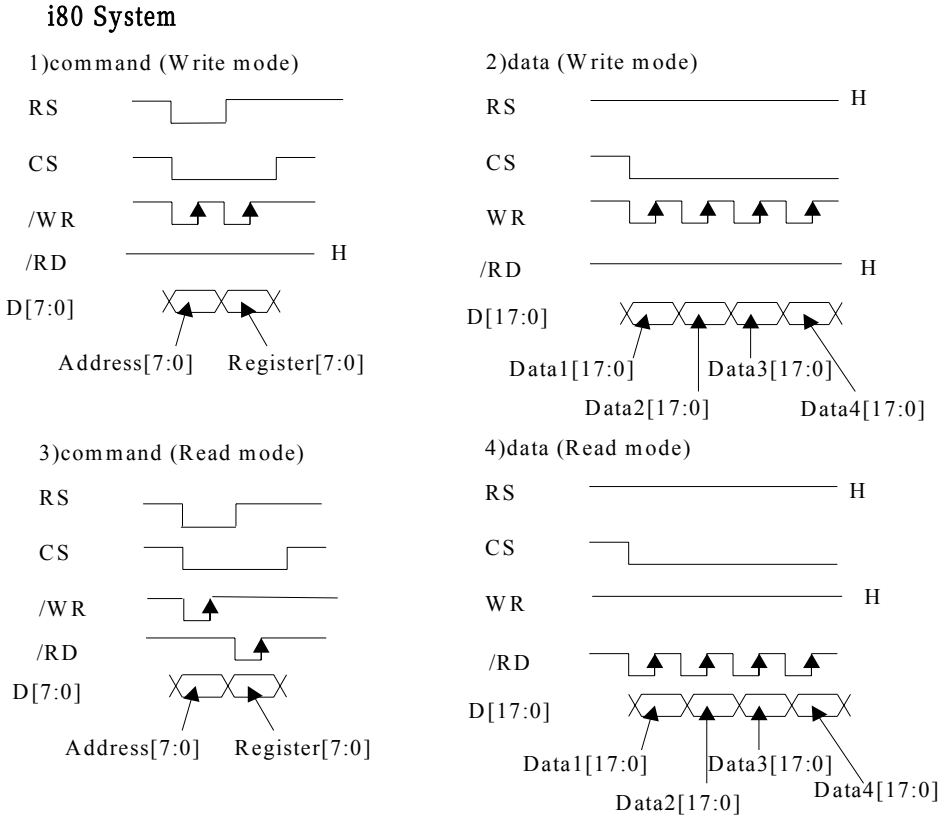
Command data

1-time write mode

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	—	—	—	—	—	A7	A6	A5	A4	A3	A2	A1	A0
—	—	—	—	—	—	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0

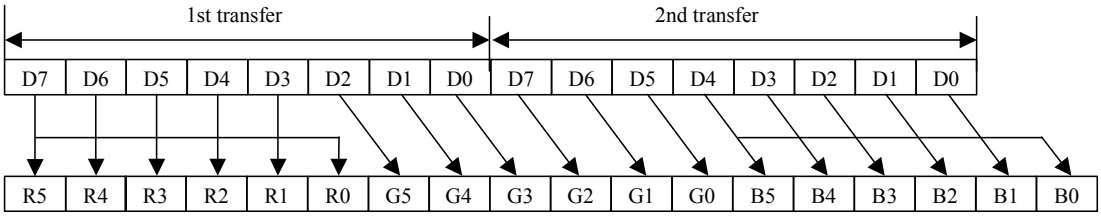
Input timing waveform

i80 System

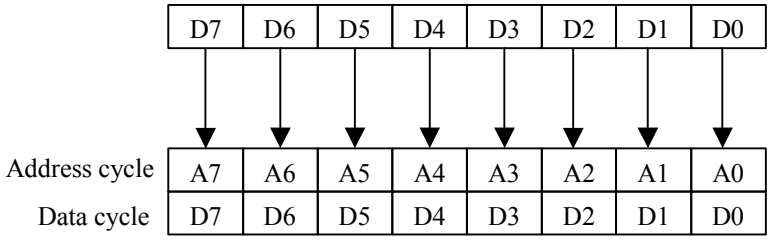


6.2.3 CPU Interface 8 bit mode

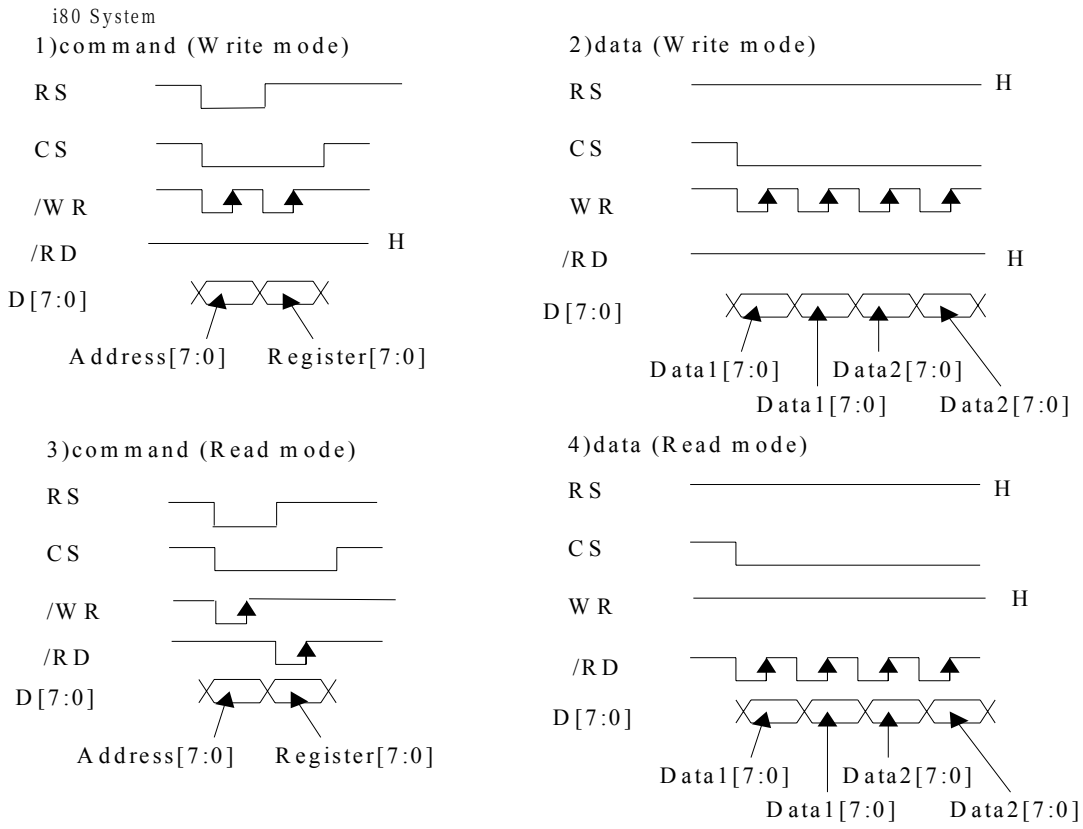
Signal data



Command data

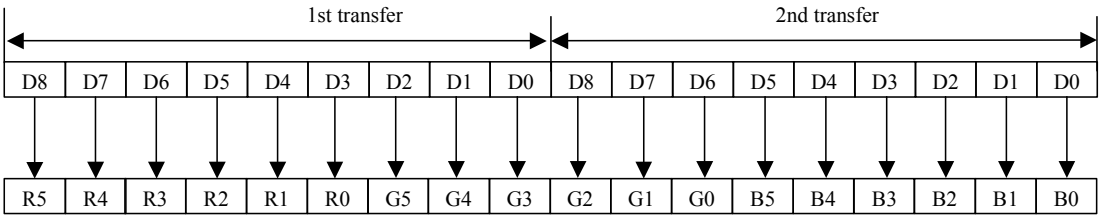


Input timing waveform



6.2.4 CPU Interface 9 bit mode

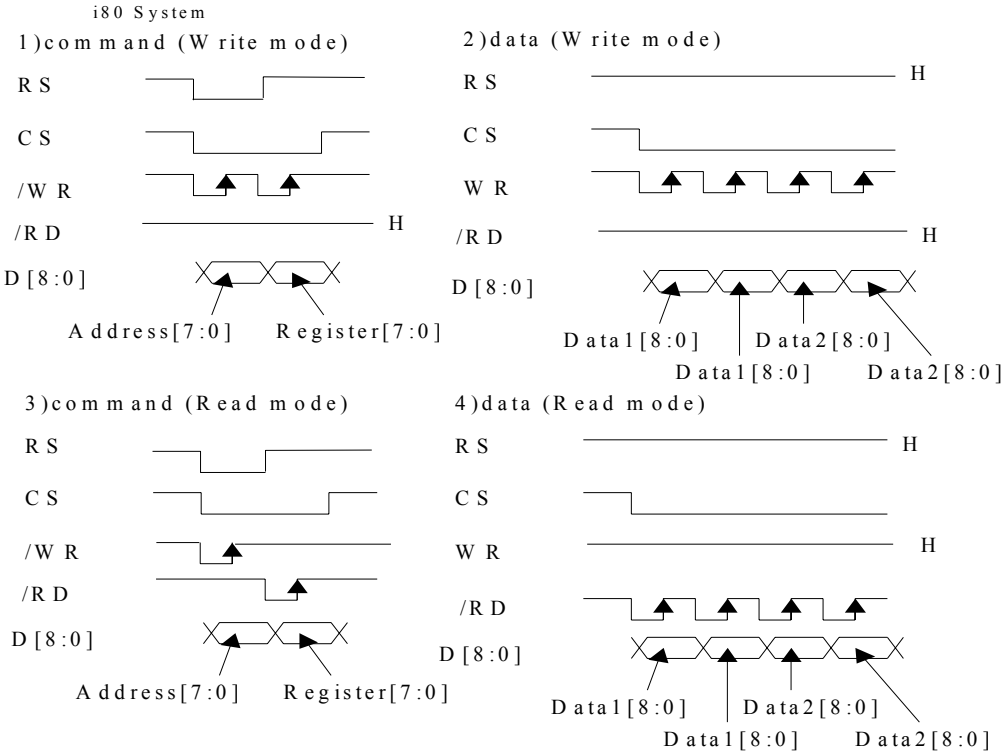
Signal data



Command data

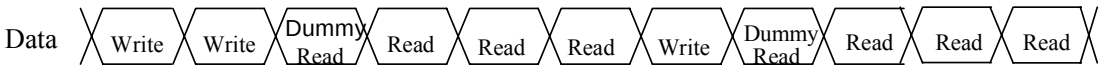
	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address cycle	—	A7	A6	A5	A4	A3	A2	A1	A0
Data cycle	—	D7	D6	D5	D4	D3	D2	D1	D0

Input timing waveform



Note : The first RAM read operation after write cycle , the RAM data of address counter is read to read data latch. In the next read operation, the RAM data of address counter is read to interface from read data latch and the RAM data of address counter + 1 is read to read data latch.

Therefore, a dummy read operation is necessary between write→read.



6.3 SRAM address for RGB database

	R0	G0	B0	R1	G1	B1	…….	R126	G126	B126	R127	G127	B127
	D17……D0			D17…….D0				D17…….D0			D17…….D0		
L1	“0000”H			“0001”H			…….	“007E”H			“007F”H		
L2	“0100”H			“0101”H			…….	“017E”H			“017F”H		
L3	“0200”H			“0201”H			…….	“027E”H			“027F”H		
L4	“0300”H			“0301”H			…….	“037E”H			“037F”H		
L5	“0400”H			“0401”H			…….	“047E”H			“047F”H		
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
L155	“9A00”H			“9A01”H			…….	“9A7E”H			“9A7F”H		
L156	“9B00”H			“9B01”H			…….	“9B7E”H			“9B7F”H		
L157	“9C00”H			“9C01”H			…….	“9C7E”H			“9C7F”H		
L158	“9D00”H			“9D01”H			…….	“9D7E”H			“9D7F”H		
L159	“9E00”H			“9E01”H			…….	“9E7E”H			“9E7F”H		
L160	“9F00”H			“9F01”H			…….	“9F7E”H			“9F7F”H		

6.4 Setup data (CPU interface)

Address	Register/Bit Name	Reset Value	Meaning	Comment
0x00	CHIPID	xx00-1001	[5:3] : REVID (read only) [2:0] : CHIPID (read only)	
0x01	MODE_SEL1	0000-0010	[7:6] Panel resolution select 00: 128 x 160 (Default) 01: 128 x 128 10 :96 x 96 11 : 132 x 160 [5] Vcom output mask in partial mode 0: Normal (unmask) **(Default)** 1: Vcom output mask [4:2] display mode 000: 16/18 bit color 001: 16/18 bit color + partial 010: 1bit color 011: 8 color + partial 100: 8color + dithering 101: 8 color + dithering + partial [1] SLP: sleep mode 0: sleep 1: normal(Default) [0] Out of range data control: 0 : White (Default) 1 : Black	
0x02	MODE_SEL2	0001-0010	[7:6] Scan direction [7] 0: CSV=1(V normal scan) (Default) 1: CSV=0 (V reverse scan) [6] 0 : CSH=1(H normal scan) (Default) 1: CSH=0(H reverse scan) [5] : line or frame inversion select : 0 : line inversion (Default) 1 : frame inversion [4] STV2 signal output 0 :STV2 output 1 : STV2 NO output(Default) [3] STV1 signal output 0 :STV1 output (Default) 1 : STV1 NO output [2:1] Non-partial area data output control 00 : GND output 01 : VcomL output **(Default)** 1x : Hi-Z [0] Non-partial area CKH1/2/3 output control 0 : CKH1/2/3 output = “Low” **(Default)** 1 : CKH1/2/3 output = “High”	
0x03	MODE_SEL3	0000-xxxx	[7:6] Input data selection 00 : 8 bit mode (Default) 01 : 16 bit mode 10 : 9 bit mode 11 : 18 bit mode [5:4] BODR : 16 bit data access control 00 : 1st cycle include only 2 bit data and 2nd cycle include 16 bit data (Default) 01 : 1st cycle include 16 bit data and 2nd cycle include only	

			2 bit data 1x : Use 16 Bit transfer 18 Bit data (R:G:B = 5:6:5)	
0x05	VCO_Mode	xx00-1000	[4:3] : VCO bias mode select 00 : -5% 01 : typical (Default) 10 : +5% 11 : +10% [5] , [2:0] : VCO frequency 0 , 000 : 1.82 MHz **(Default)** 1 , 000 : 1.82 × 3/4 MHz 0 , 001 : 1.82 / 2 MHz 0 , 010 : 1.5 MHz 1 , 010 : 1.5 × 3/4 MHz 0 , 011 : 1.5 / 2 MHz 0 , 100 : 0.9 MHz 1 , 100 : 0.9 × 3/4 MHz 0 , 101 : 0.9 / 2 MHz	
0x06	DAC_OP_CTRL 2	1000-0101	[7] 4.2V,10V , -5.5V power on signal select 0 : Input pin PWDN 1 : Internal register ([6]) **(Default)** [6] int_PWDN : 4.2V ,10V , -5.5V power on signal 0 : Vout4.2 ,Vout10 , Vout-5.5 power off**(Default)** 1 : Vout4.2 ,Vout10 , Vout-5.5 power on [5:4] DAC bias select 00 : 100% (Default) 01 : 80% 10 : 60% 11 : 50% [3:2] Vcom bias select 00 : -20% × normal 01 : normal **(Default)** 10 : 20% × normal 11 : 40% × normal [1:0] RGB loading select 00 : 5p 01 : 10.5p (Default) 10 : 15p 11 : 20p	
0x07	VCOMH_CTRL	x111-0100	[7:0] VCOM_H output Voltage control step = 2.1V/128 = 0.0164V **(Default = 4.0V)** **(** VCOM_H=2.1V in settting x000-0001)	Note 1
0x08	VCOML_CTRL	x000-1100	[7:0] VCOM_L output Voltage control step = 2.1V/128 = 0.0164V **(Default = 0.197V)** **(** VCOM_L=0V in setting x000-0000)	Note 1
SRAM control				
0x09	PWS-X	0000-0000	[7:0] Write SRAM window start X point	
0x10	PWS-Y	0000-0000	[7:0] Write SRAM window start Y point	
0x11	PWE-X	0111-1111	[7:0] Write SRAM window end X point	
0x12	PWE-Y	1001-1111	[7:0] Write SRAM window end Y point	
0x14	PDS-Y	0000-0000	[7:0] Partial Display start Y point	

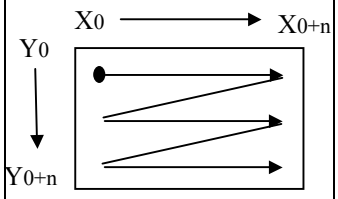
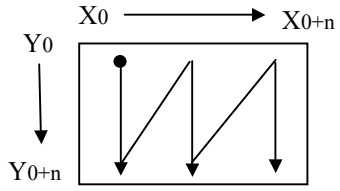
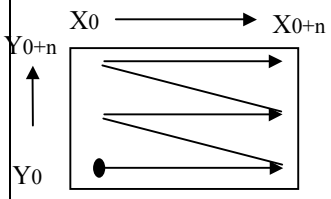
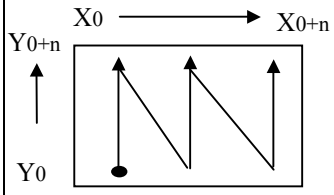
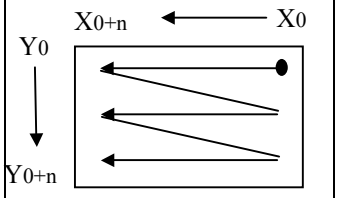
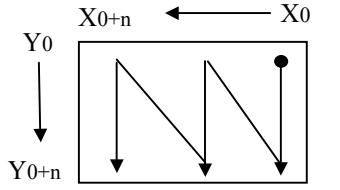
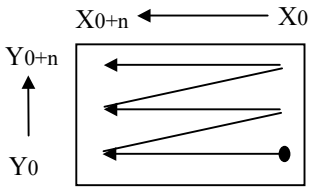
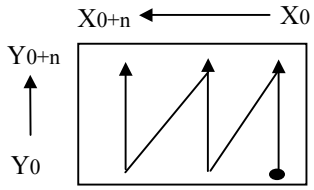
0x16	PDE-Y	0010-0000	[7:0] Partial Display end Y point	
0x17	SRAM _Control	xxx0-0000	**[4] reserve** [3] If X or Y position is set over range, 0 : Ineffective writing. X or Y position are not changed. **(Default)** [2] SACX (SRAM X Address Counter) 0 : SRAM X position + 1 **(Default)** 1 : SRAM X position – 1 [1] SACY (SRAM Y Address Counter) 0 : SRAM Y position + 1 **(Default)** 1 : SRAM Y position –1 [0] SACA (SRAM access control) 0 : add X position first then add Y position **(Default)** 1 : add Y position first then add X position	Note 2 [3] register always 0
0x18	SRAM_Position_X	x000-0000	[7:0] SRAM X position 0<= X <=0x83	
0x19	SRAM_Position_Y	0000-0000	[7:0] SRAM Y position 0<= Y <= 0x9F	
0x21	Gamma Adj. 1	xx00-0000	[5:3] PV0 ; [2:0] NV0	
0x22	Gamma Adj. 2	xx00-0000	[5:3] PV1 ; [2:0] NV1	
0x23	Gamma Adj. 3	xx00-0000	[5:3] PV8 ; [2:0] NV8	
0x24	Gamma Adj. 4	xx00-0000	[5:3] PV20 ; [2:0] NV20	
0x25	Gamma Adj. 5	xx00-0000	[5:3] PV43 ; [2:0] NV43	
0x26	Gamma Adj. 6	xx00-0000	[5:3] PV55 ; [2:0] NV55	
0x27	Gamma Adj. 7	xx00-0000	[5:3] PV62 ; [2:0] NV62	
0x28	Gamma Adj. 8	xx00-0000	[5:3] PV63 ; [2:0] NV63	

Note1: Vcom Table

Digital Input	VCOMH Output
Decimal	Voltage (V)
127	4.184
126	4.167
125	4.151
124	4.134
123	4.118
122	4.102
121	4.085
120	4.069
119	4.052
118	4.036
117	4.020
116	4.003 (Normal mode)
115	3.987
114	3.970
81	3.429
80	3.413
79	3.396
78	3.380
77	3.363
25	2.510
24	2.494
23	2.477
22	2.461
21	2.445
20	2.428
19	2.412 (8 color /8 color partial)
18	2.395
17	2.379
16	2.363
15	2.346
14	2.330
13	2.313
12	2.297
11	2.280
10	2.264
9	2.248
8	2.231
7	2.215
6	2.198
5	2.182
4	2.166
3	2.149
2	2.133
1	2.1

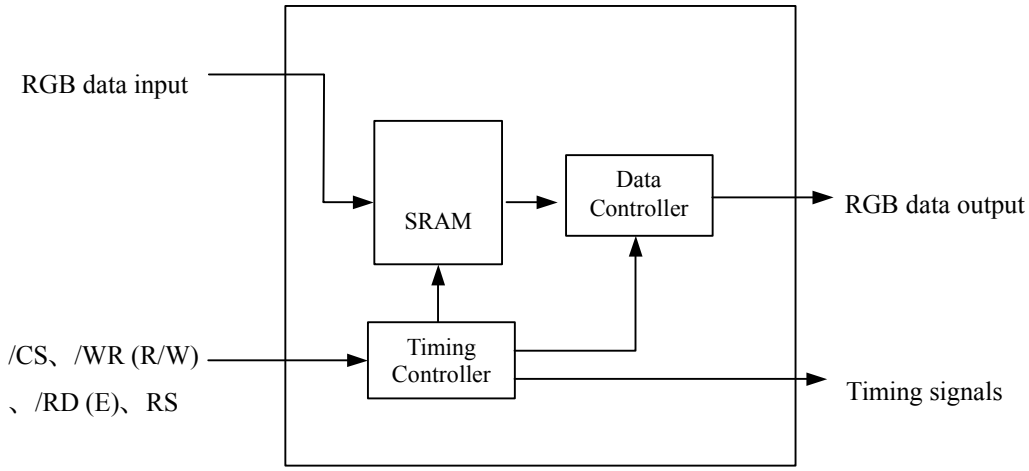
Digital Input	VCOML Output
Decimal	Voltage (V)
127	2.084
126	2.067
125	2.051
124	2.034
123	2.018
122	2.002
121	1.985
120	1.969
119	1.952
118	1.936
117	1.920
116	1.903
115	1.887
114	1.870
81	1.329
80	1.313
79	1.296
78	1.280
77	1.263
25	0.410
24	0.394
23	0.377
22	0.361
21	0.345
20	0.328
19	0.312
18	0.295
17	0.279
16	0.263
15	0.246
14	0.230
13	0.213
12	0.197(Normal mode)
11	0.180
10	0.164
9	0.148
8	0.131
7	0.115
6	0.098
5	0.082
4	0.066
3	0.049
2	0.033
1	0.016 (8 color /8 color partial)

Note2: SRAM _Control

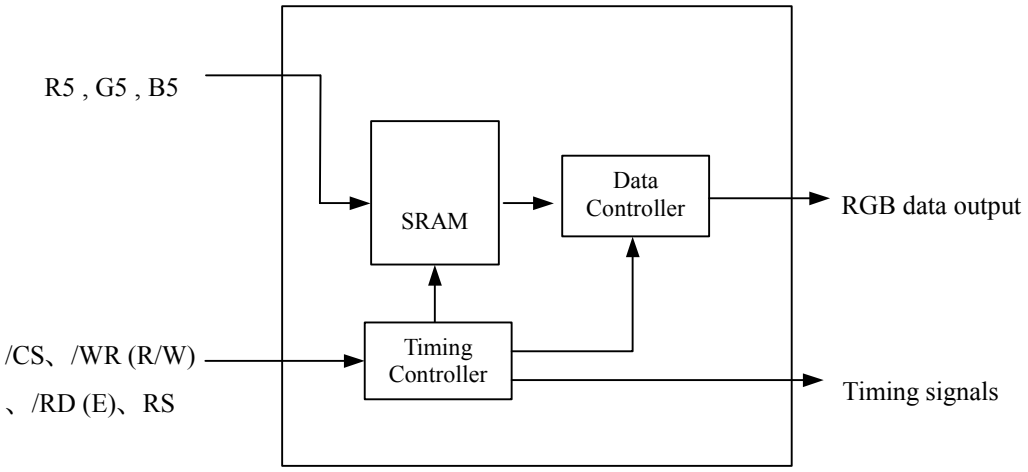
SACA	SACX	SACY		SACA	SACX	SACY	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

6.5 Mode Setup

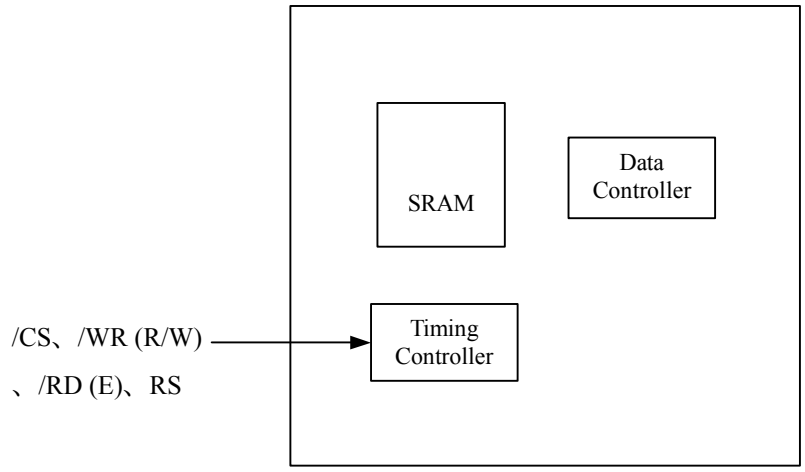
6.5.1 Normal (Moving) Mode



6.5.2 8 color(Partial) Mode



6.5.3 Sleep Mode

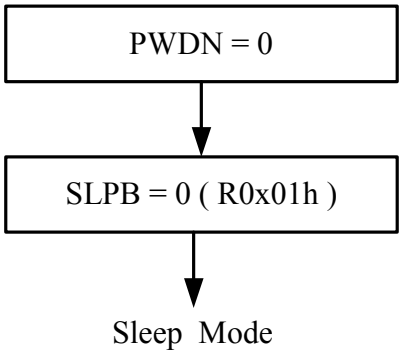


Note 1: Only receive register data. SRAM data can be retained.

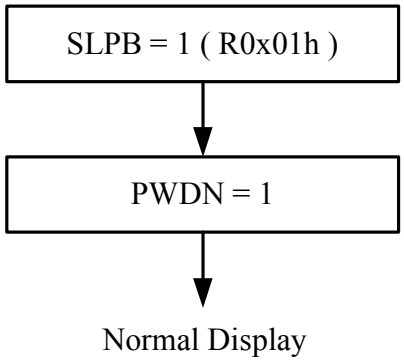
Note 2: The VCO is stopped in sleep mode.

Note 3: The power Vout1.8 is not off in sleep mode and is controlled by PS1 input.

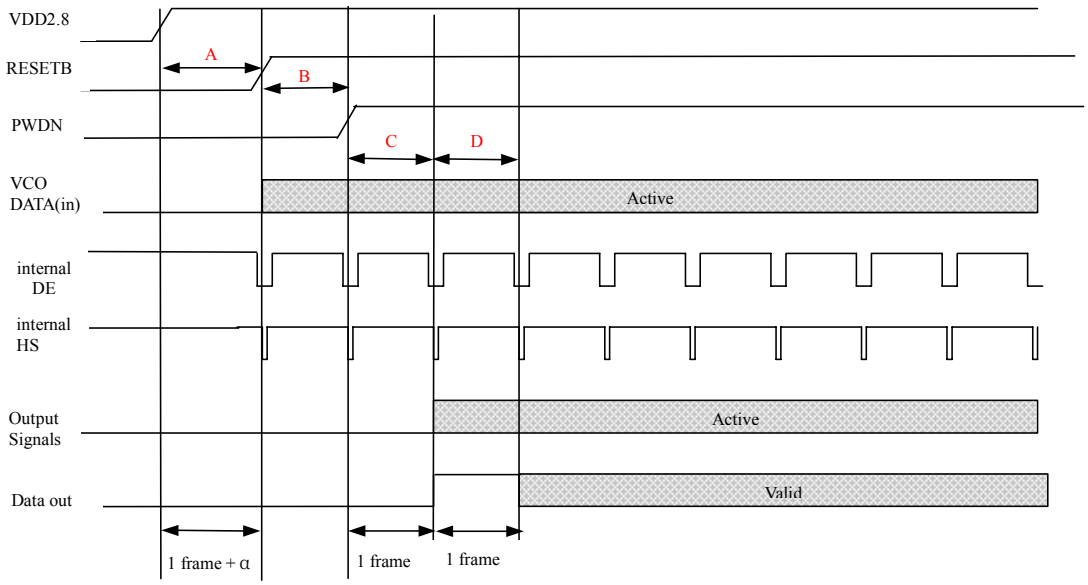
Sleep Mode Setting Flow



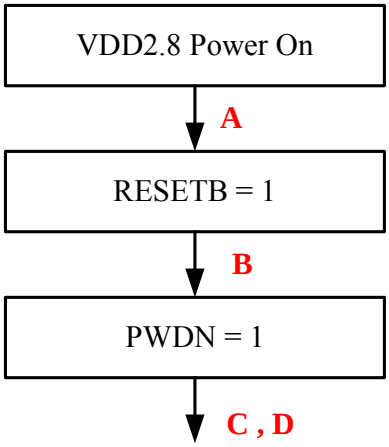
Sleep Mode Cancel Flow



6.5.4 Power on sequence



Power on Flow



Normal Mode Display

A : Vout1.8 Power on , SRAM selfclear , Normal mode , VCO clock start oscillation.

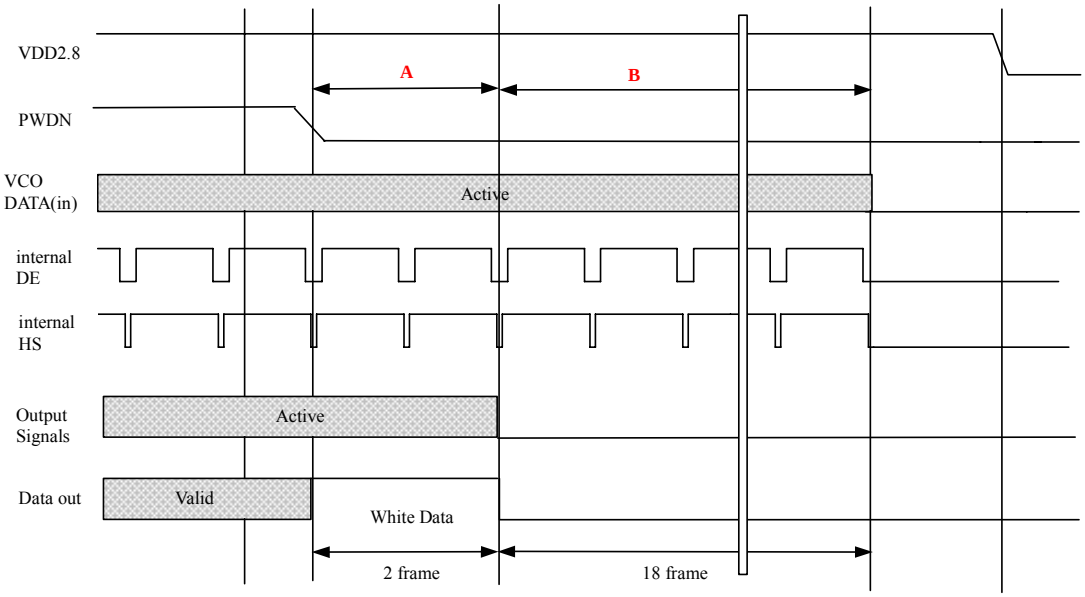
B : Start SRAM update and register setting .

C : Vout4.2 , Vout10 , Vout-5.5 power source generation.

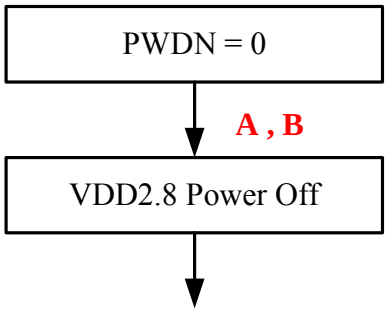
D : Display timing signal output and white data display.

Note : PWDN = 0 Vout4.2 , Vout10 , Vout-5.5 power off
PWDN = 1 Vout4.2 , Vout10 , Vout-5.5 power on

6.5.5 Power off sequence



Power Off Flow



A : White data display

B : Display timing and data output stop
Vout4.2 , Vout10 , Vout-5.5 power off

6.6 Input Signals, Basic Display Color and Gray Scale of Each Color

6.6.1 65K

Color	Display	Data Signal																Gray Scale
		Red					Green						Blue					
		R0	R1	R2	R3	R4	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	-
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	-
	Cyan	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
																		R3~
																		R28
	↓	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R29
	Light	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R30
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R31
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	G2
																		G3~
																		G60
	↓	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	G62
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	G63
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	B2
																		B3~
																		B28
	↓	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	B29
	Light	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	B30
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B31

6.6.2 262K

Color	Display	Data Signal																		Gray Scale
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
																				R3~
																				R60
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
																				G3~
																				G60
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
																				B3~
																				B60
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

6.7 Software Algorithms

Step 1: Follow power on sequence

- ⇨ ***Input power (+2.8V) on***
- ⇨ ***Wait 1 frame + γ time***
- ⇨ ***Reset signal from Lo to Hi***
- ⇨ ***Setting register***
  - ■ R01 (Mode_SEL1)
  - ■ R02 (Mode_SEL2)
  - ■ R03 (Mode_SEL3)
  - ■ R05 (VCO_Mode)
  - ■ R08 (VCOML_CTRH)
  - ■ R07 (VCOMH_CTRH)

Setp 2: Display turn on

- ⇨ ***Setting PWDN register turn on***
  - ■ R06 (Power Mode) →C5H

Setp 3: Display mode change (R01_[3:2])

- ⇨ ***Full color mode***
  - ■ Display mode select(R01_[3:2]) → 00 (Full color mode)
  - ■ VcomL Voltage setting R08 (VCOML_CTRH) →0x0C
  - ■ VcomH Voltage setting R07 (VCOMH_CTRH) →0x74
  - ■ Vcom inversion select R02_[5]→ 0 (Line inversion)

- ⇨ ***8 color mode***
  - ■ Display mode select(R01_[3:2]) → 10 (8 color mode)
  - ■ Vcom inversion select R02_[5]→ 1 (Frame inversion)
  - ■ Wait at least 2 frame
  - ■ VcomL Voltage setting R08 (VCOML_CTRH) →0x01
  - ■ VcomH Voltage setting R07 (VCOMH_CTRH) →0x1B

- ⇨ ***8 color partial mode***
  - ■ Write 1 frame white data ➔ Clear SRAM
  - ■ Setting partial start point (R14_[7:0]) → 0x01
  - ■ Setting partial end point (R16_[7:0]) → 0x9F
  - ■ Display mode select(R01_[3:2]) → 11 (8 color partial mode)
  - ■ Vcom inversion select R02_[5]→ 1 (Frame inversion)
  - ■ Write 2 frame white data ➔ Clear SRAM
  - ■ Setting partial start point (R14_[7:0])

- ✓ Line 1 → 0000-0001
- ✓ Line 160 → 1010-0000

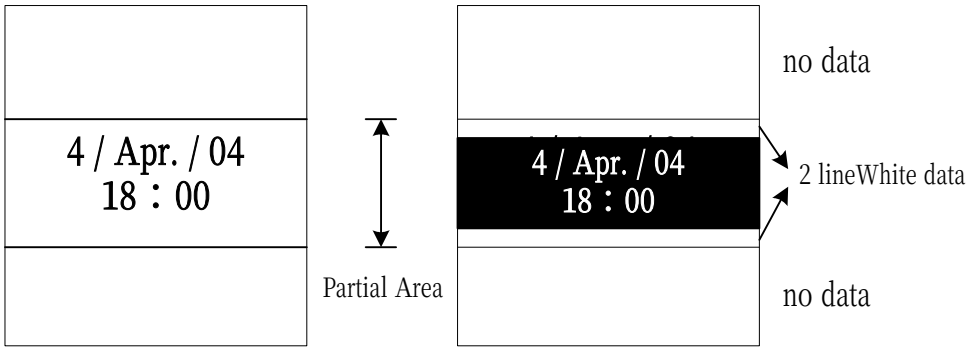
■ Setting partial end point (R16_[7:0])

- ✓ Line 1 → 0000-0001
- ✓ Line 160 → 1010-0000

■ VcomL Voltage setting R08 (VCOML_CTRH) →0x01

■ VcomH Voltage setting R07 (VCOMH_CTRH) →0x1B

■ Display type



⇨ ***Change to sleep mode***

■ Setting PWDN register turn off

- ✓ R06 (Power Mode)→ 85H

■ Wait 20 frame (0.3 S)

■ Sleep bit (R01[1]) → 0

⇨ ***Main Panel & Sub Panel control(R02_[4:3])***

■ Main on

- ✓ Write (R02_[7:6])→ 00
- ✓ Write (R02_[4:3])→ 01

■ Sub on

- ✓ Write (R02_[7:6])→ 10
- ✓ Write (R02_[4:3])→ 10

Setp 4: Follow power off sequence

⇨ ***Setting PWDN register turn off***

■ R06 (Power Mode)→ 85H

⇨ ***Wait 20 frame (0.3 S)***

⇨ ***Input power (+2.8V) off***

7 OPTICAL CHARACTERISTICS

7.1 Optical Specification

7.1.1 Transmissive Mode (Backlight On, I_F=15mA)

Ta=25℃

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles		Θ11	CR ≥ 2	40	45	--	Degree	Note 7-1
		Θ12		40	45	--		
		Θ21		40	45	--		
		Θ22		55	60	--		
Contrast Ratio		CR	Θ=0°	70	80	--		Note 7-2
Response Time		Tr+Tf		--	35	45	ms	Note 7-3
Luminance (I_F=15mA)		L		180	200	--	cd/m^2	Note 7-4
Color	White	x_{WON}		0.25	0.30	0.35		Note 7-5
		y_{WON}		0.27	0.32	0.37		
Uniformity		%		70				

7.1.2 Reflective Mode (Backlight Off)

Ta=25℃

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11	CR ≥ 2	40	45	--	Degree	Note 7-1
	Θ12		40	45	--		
	Θ21		40	45	--		
	Θ22		55	60	--		
Contrast Ratio	CR	Θ=10°	10	15	--		Note 7-6
Reflectance	Rf		10	15			Note 7-7
White Chromaticity	x_{WOFF}		0.26	0.31	0.36		Note 7-8
	y_{WOFF}		0.29	0.34	0.39		

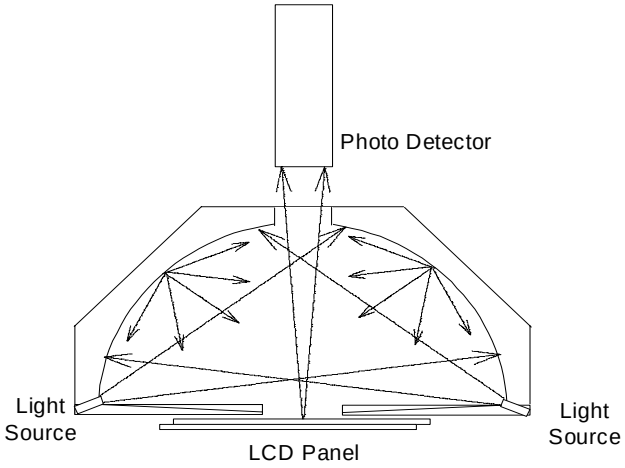
7.2 Basic Measure Condition

(1) Ambient Temperature: Ta=25℃

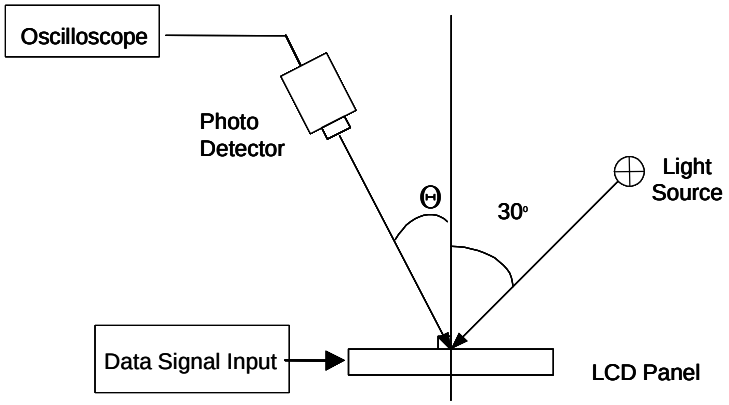
(2) Testing Point: Measure in the display center point and the test angle Θ=0°

(3) Measuring System

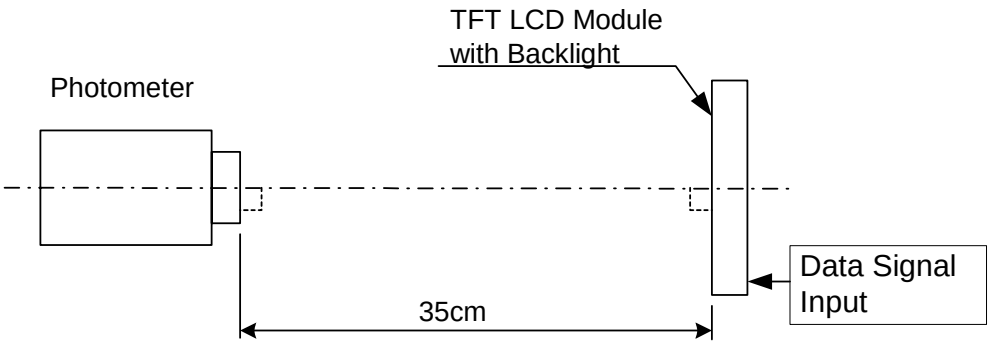
a. Measure System A



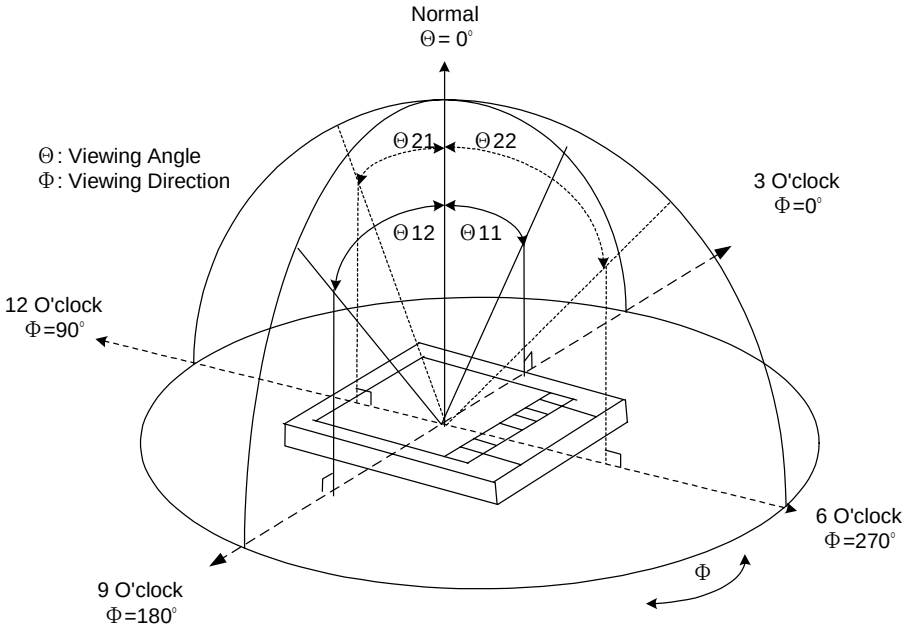
b. Measure System B



c. Measure System C



Note 7-1: Viewing angle diagram:

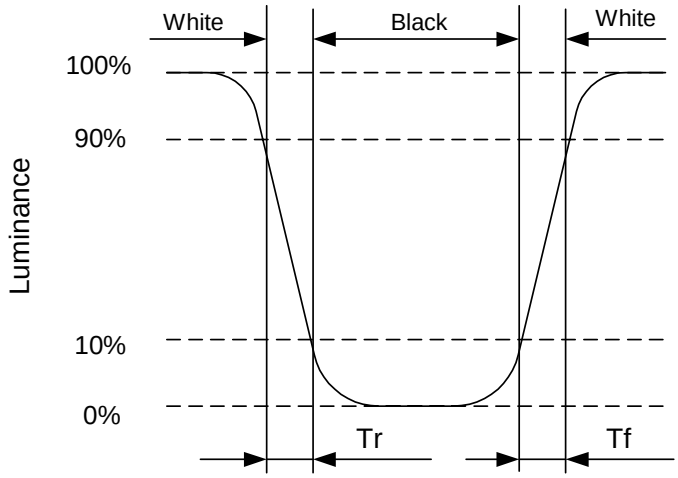


Note 7-2: Contrast Ratio as Backlight On: (Measure System C)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time: (Measure System C)



Note 7-4: Luminance: (Measure System C)

Test Point: Display Center

LED Current If = 15 mA

Note 7-5: Chromaticity: The same test condition as Note 7-4.

Note: 7-6: Contrast Ratio as Backlight Off: (Measure System B)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-7: Reflectance: (Measure System B)

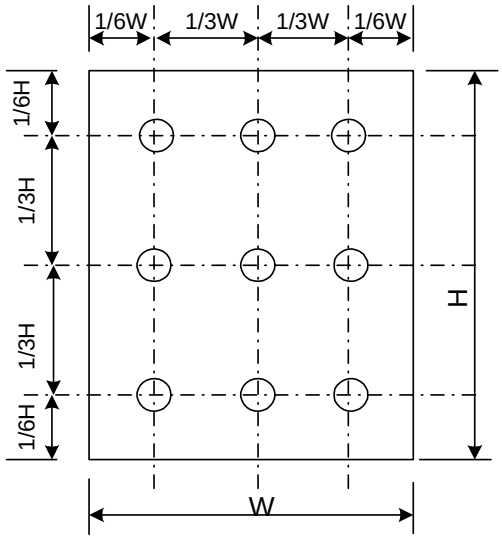
$$\text{Reflection ratio(R)} = \frac{\text{Light detected level of refection by the LCD module}}{\text{Light detected level of refection by the standard white}}$$

Note 7-8: White chromaticity as back light off: (Measure System A)

Notes 7-9: Definition of uniformity: Light on backlight 5 minutes before test.

$$\text{Uniformity (Lu)} = \frac{\text{Minimum Luminance of 9 test points}}{\text{Center Point Luminance of 9 test points}} \text{X100\%}$$

The definition of 9 test points:



8 RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta = +70℃, 240hrs
2	High Temperature & High Humidity Operation	Ta = +40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta = -20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta = +80℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta = -30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃←→ 80℃, 30 cycles 30 min 30 min
7	Surface Discharge (non-operation)	C=150pF, R=330Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11 min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Twice

Ta: Ambient Temperature

9 HANDLING CAUTIONS

9.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. Connect the wrist conduction ring to the earth and the conducting shoes to the earth are necessary.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, using ionized air to decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

9.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) The front polarizer is easy damaged. Handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface. Please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

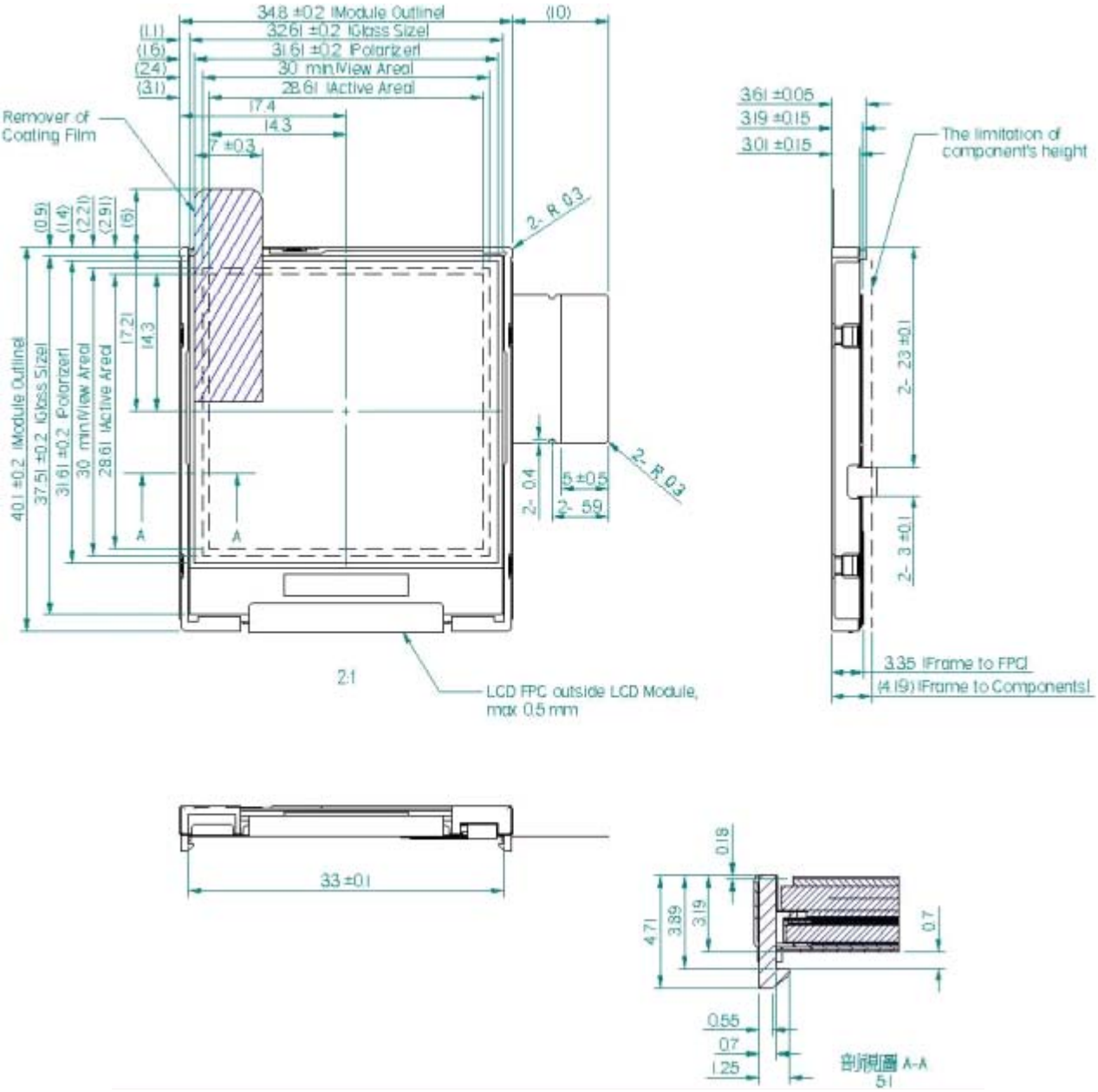
(1) Turn off the power supply before connecting and disconnecting signal input cable.

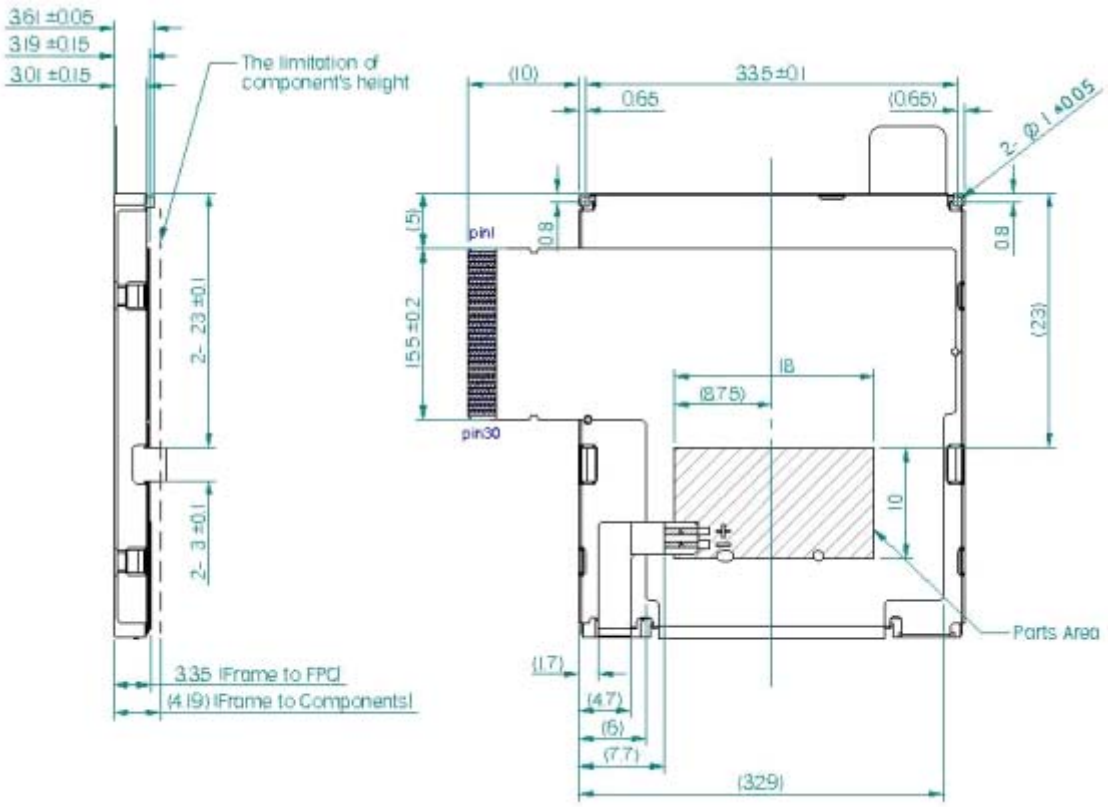
(2) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(3) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

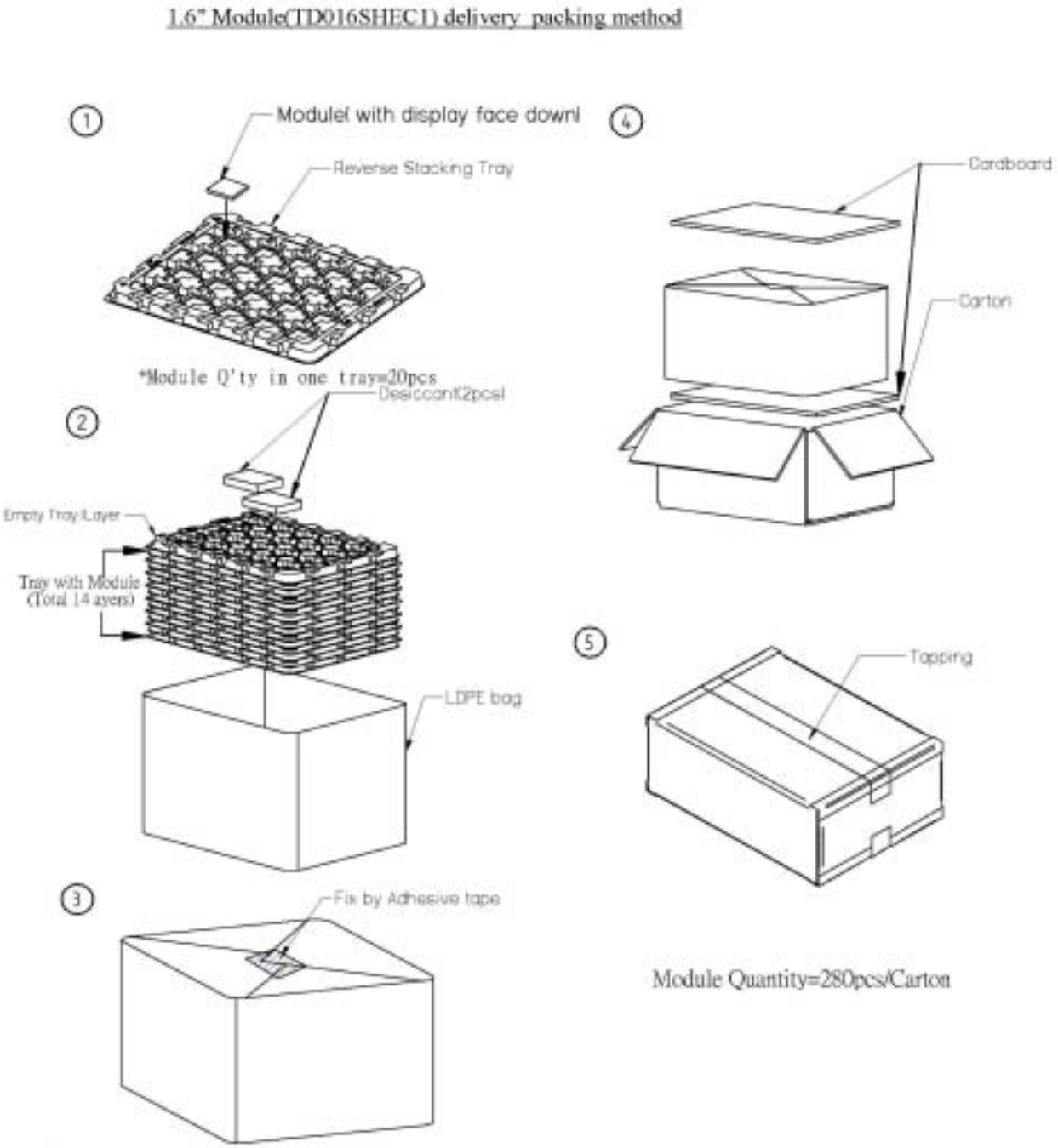
(4) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

10 MECHANICAL DRAWING





11. PACKING DRAWING



1.6" module(TD016SHEC1) delivery packing method

(1).Module packed into tray cavity(with Module display face down).

(2).Tray pack with module (Tray stacking with 14 layers) and with 1 empty tray above the stacking tray unit.2pcs desiccant put above the empty tray.

(3).Stacking tray unit put into the LDPE bag and fixed by adhesive tape.

(4).Put 1pc cardboard inside the carton bottom, then pack the package unit into the carton. and with 1pc cardboard above the package unit.

(5).Carton tapping with adhesive tape.