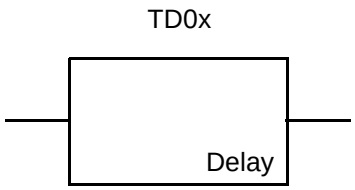
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD02	TD03	TD08
A	1.5	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD02	9.0	TBD	20.9
TD03	9.0	TBD	22.8
TD08	17.0	TBD	48.4

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

TD02	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	2.62 2.73	2.71 2.88	2.80 2.96	2.88 3.03	2.98 3.09
TD03	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	4.01 4.12	4.05 4.15	4.13 4.24	4.24 4.37	4.41 4.57
TD08	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	11.98 11.49	12.11 11.54	12.21 11.62	12.29 11.75	12.37 11.93