TFT LCD Specification

Model NO.: TD028STEB2

Customer Signature
Date

This technical specification is subjected to change without notice.

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Record of Reversion

Rev	Issued Date	Description
0.0	Jul, 8 , 2005	New
0.1	Sep, 22, 2005	1. Update Weight in Page 4. 2. Update 5.1 Driving TFT LCD Panel 3. Update 7.3 Setup / Hold Timing Chart 4. Update 8 Power ON/OFF Sequence 5. Add 8.3 Command descriptions
0.2	Mar, 1, 2006	1. Update Power consumption, LCD Panel + System 2. Update 3 INPUT/OUTPUT TERMINALS 3. Update 12 Mechanical Drawing for T/P outline enlarged
1.0	Mar, 28, 2006	Apply for production 1. Update 5.1 Driving TFT LCD Panel 2. Update 6. BLOCK DIAGRAM 3. Update 7.1 Display timing 4. Update 7.3 Setup/Hold Timing chart
1.1	July, 20, 2006	1. Update 5.1 Driving TFT LCD Panel 2. Update 7.3 Setup / Hold Timing chart 3. Update 8.1 Power On Sequence 4. Update 12 Panel drawing with 2nd source T/P

1. FEATURES

The 2.8 inch (real 2.83 inch) LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and COG design are built on the panel. Highly integrated LCD module includes backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		2.8 inch (real 2.83 inch)	-
Display Type		Transflective	-
Active Area (HxV)		43.2 X 57.6	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.06 X 0.180	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		52.9 X 71.7 X 4.2 (FPC excluded)	mm
Weight		35 (Max)	g
Power consumption	LCD Panel + System	23	mW
	Backlight	288 (Typ, I_F= 20mA)	

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Recommend connector: FH23-61S-0.3SHW, HIROSE

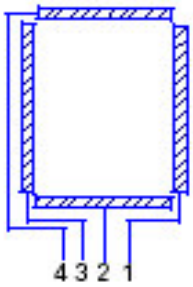
Pin	Symbol	P/I/O	Description	Remark
1	DE	I	Data enable	
2	MCLK	I	Main clock	
3	RESET	I	IC Reset	
4	YU	I	TSP YU Signal	
5	GND	P	Ground	
6	N.C.		No connection	
7	N.C.		No connection	
8	GND	P	Ground	
9	N.C.		No connection	
10	N.C.		No connection	
11	N.C.		No connection	
12	N.C.		No connection	
13	GND	P	Ground	
14	XL	O	TSP XL Signal	
15	N.C.		No connection	
16	N.C.		No connection	
17	N.C.		No connection	
18	N.C.		No connection	
19	GND	P	Ground	
20	DVDD	P	Logic Power	
21	DVDD	P	Logic Power	
22	N.C.		No connection	
23	N.C.		No connection	
24	YL	I	TSP YL Signal	
25	GND	P	Ground	
26	N.C.		No connection	
27	XR	O	TSP XR Signal	
28	DVDD	P	Logic Power	
29	D17	I	Red data (R5)	
30	D16	I	Red data (R4)	
31	D15	I	Red data (R3)	
32	D14	I	Red data (R2)	
33	D13	I	Red data (R1)	

34	D12	I	Red data (R0)	
35	D11	I	Green data (G5)	
36	D10	I	Green data (G4)	
37	D9	I	Green data (G3)	
38	D8	I	Green data (G2)	
39	D7	I	Green data (G1)	
40	D6	I	Green data (G0)	
41	D5	I	Blue data (B5)	
42	D4	I	Blue data (B4)	
43	D3	I	Blue data (B3)	
44	D2	I	Blue data (B2)	
45	D1	I	Blue data (B1)	
46	D0	I	Blue data (B0)	
47	N.C.		No connection	
48	CS	I	Chip select	
49	SCL	I	SPI / Write clock	
50	SDA	I/O	SPI / Data input	
51	NC		No connection	
52	HSYNC	I	Horizontal sync signal	
53	GND	P	Ground	
54	N.C.		No connection	
55	N.C.		No connection	
56	VSYNC	I	Vertical sync signal	
57	LED+	P	LED ANODE	
58	LED+	P	LED ANODE	
59	LED-	P	LED CATHODE	
60	LED-	P	LED CATHODE	
61	GND	P	Ground	

3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	27	XR	Touch Panel Right Side	
2	24	YL	Touch Panel Lower Side	
3	14	XL	Touch Panel Left Side	
4	4	YU	Touch Panel Upper Side	

Pin Assignment for Touch panel



Touch Panel Pin Name		
Pin No	Assignment	Note
1	XR	Glass
2	YL	Film
3	XL	Glass
4	YU	Film

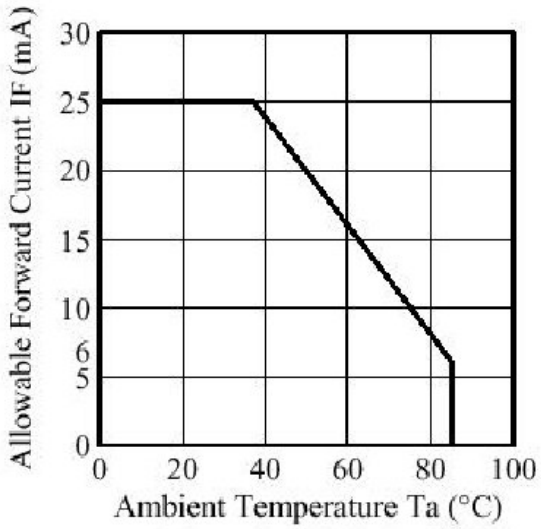
4.ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	DVDD	-0.3	3.6	V	
Touch Panel Operation Voltage	V_{Touch}	-	5	V	
Backlight LED forward Voltage	V_F	-	14.4	V	
Backlight LED reverse Voltage	V_R	-	20	V	
Backlight LED forward current (Ta=25℃)	I_F	-	25	mA	Note
Operating Temperature	Topr	-20	+60	℃	
Storage Temperature	Tstg	-30	+70	℃	

Note: Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs. Allowable Forward Current



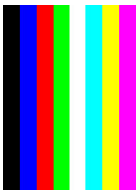
5.ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

Allowable Operation condition (Ta= -20 ~ +60℃ , VSS=0V)

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage (DC/DC)	DVDD	2.5	2.8	3.3	V	
Logic high-level input	Vih	0.8DVDD	—	DVDD	V	VSYNC、HSYNC、MCLK、DE、Data
Logic low-level input	Vil	GND	—	0.2DVDD	V	
Leakage Current	iL	-1	—	1	A	
DVDD Supply Current	I_{DVDD}	---	4.1	4.37	mA	Note

Note: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



5.2 Driving backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	25	mA	LED/Part
LED Life Time	-	-	10000	-	Hr	I_F: 20mA
Forward Current Voltage	V_F	-	14.4	16	V	I_F: 20mA ,LED/Part

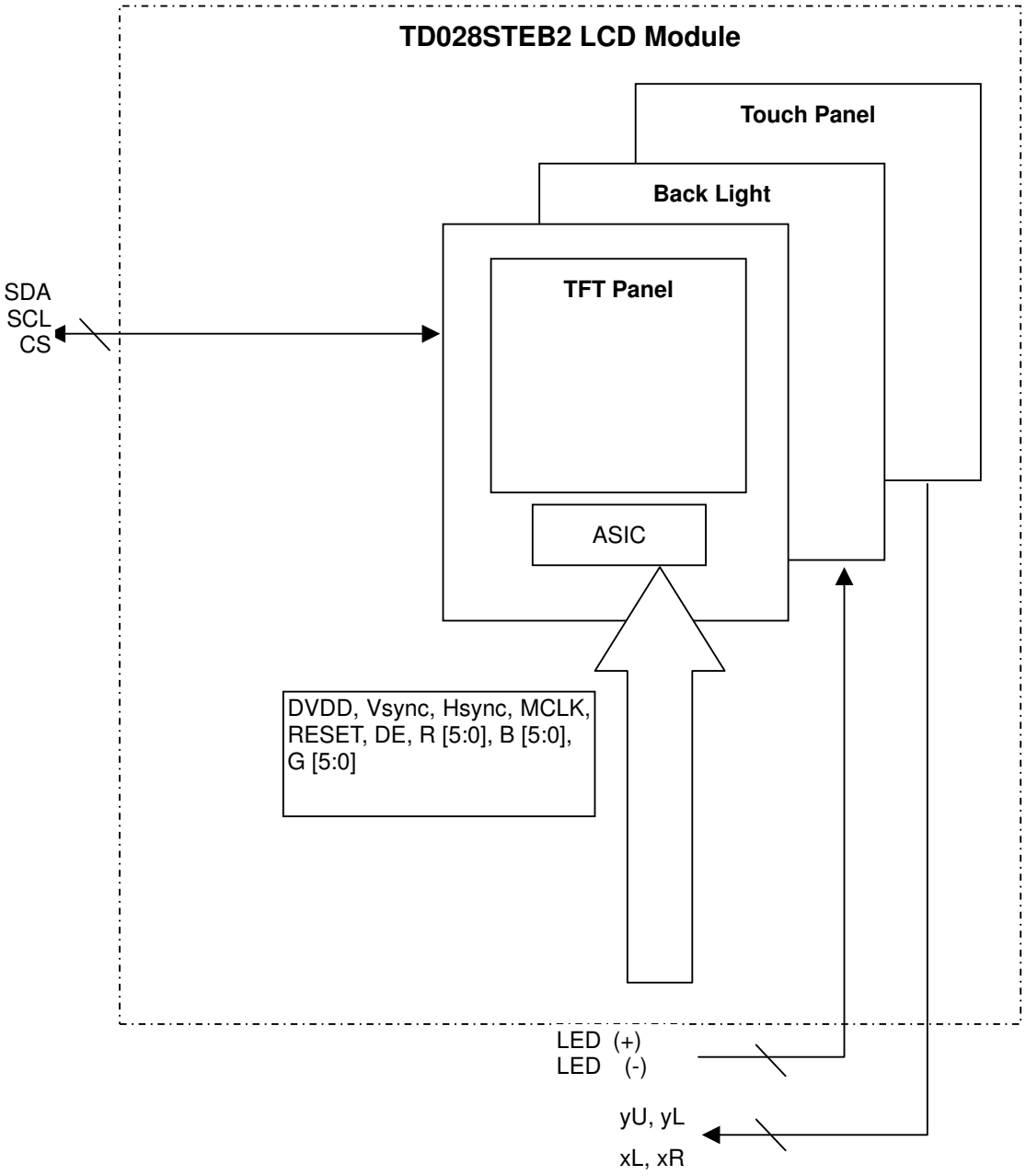
Note: Backtlight driving circuit is recommend as the fix current circuit.

5.3 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	200	-	1300	Ω	
Resistor between terminals (YU-YL)	Ry	200	-	1300	Ω	
Operation Voltage	V_{Touch}	-	5	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	10	-	ms	
Surface Hardness	-	3	-	-	H	JIS K 5600
Minimum tension for detecting	-	-	-	80	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note. The minimum test force is 80 g.

6. BLOCK DIAGRAM



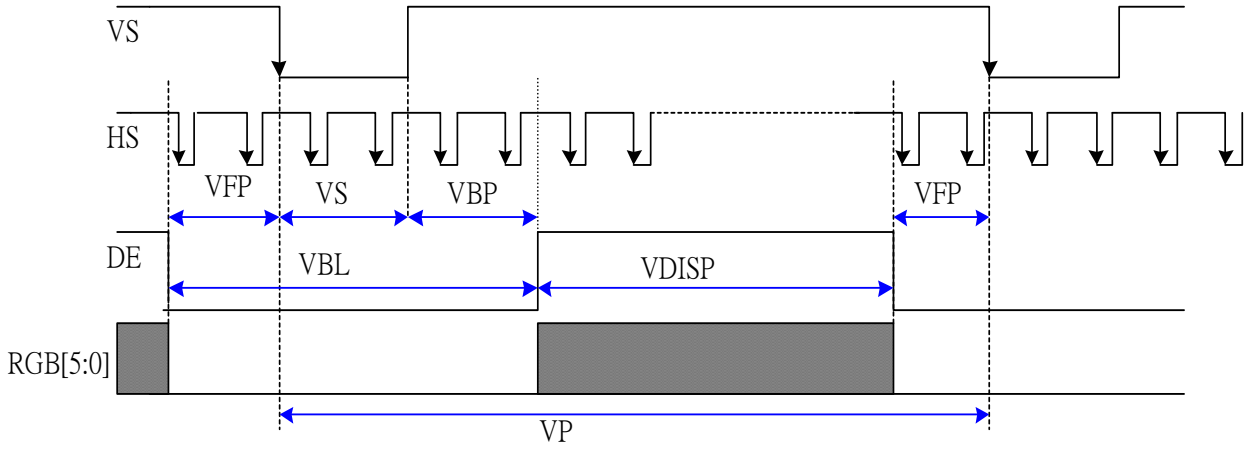
7. TIMING CHART

7.1 Display timing

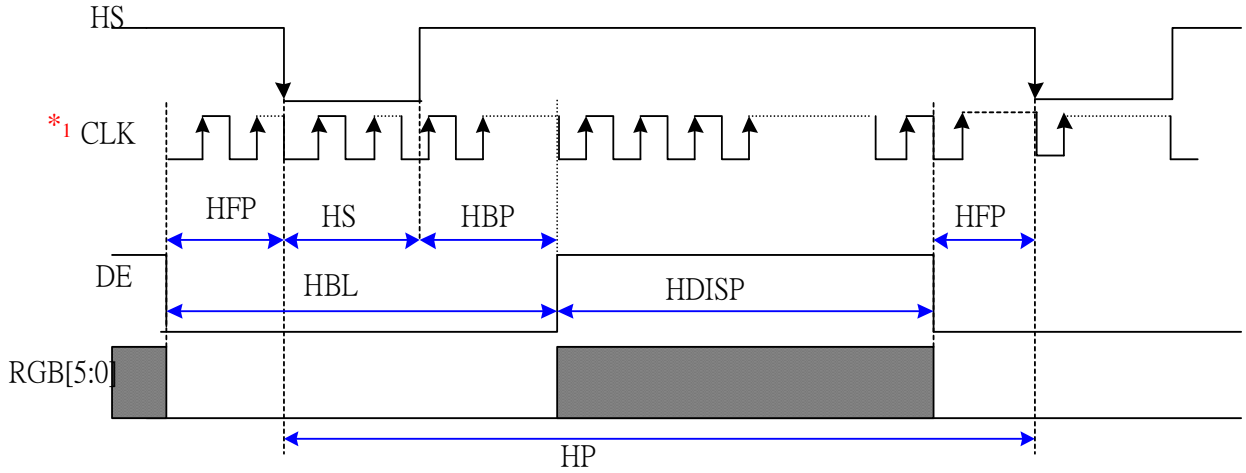
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP	-	323	326	340	Line
	Vertical data start	VDS	VS+VBP	—	4	—	Line
	Vertical front porch	VFP	-	—	2	—	Line
	Vertical back portch	VBP	-	—	2	—	Line
	Vertical active area	VDISP	-	—	320	—	Line
	Horizontal cycle	HP	-	260	280	300	dot
	Horizontal front porch	HFP	-	—	10	—	dot
	Horizontal Sync Pulse width	HS	-	—	10	—	dot
	Horizontal Back porch	HBP		—	20	—	dot
	Horizontal Data start	HDS	HS+HBP	—	30	—	dot
	Horizontal active area	HDISP	-	—	240	—	dot
	Clock frequency	fclk	-	5.02	6.39	6.85	MHz
		tclk		199	156	146	ns

7.2 Input timing chart

＜Vertical Timing chart＞

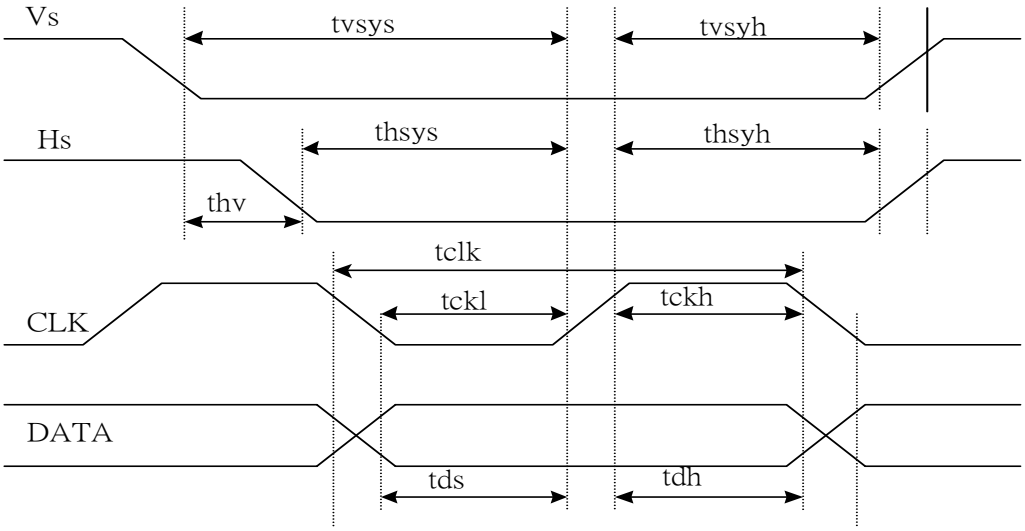


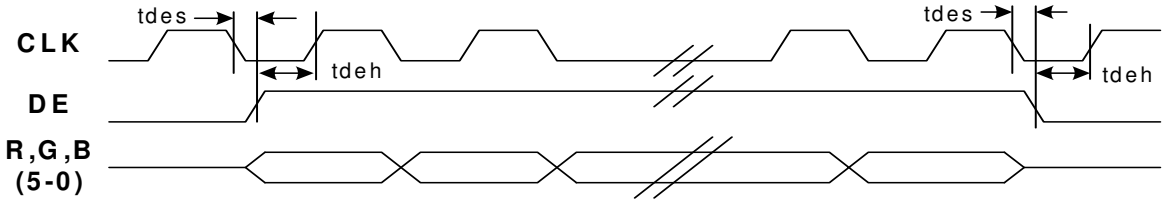
＜Horizontal Timing chart＞



*1 The frequency of CLK should keep in the range as input timing chart determined whether in display or blanking region to ensure IC operating normally.

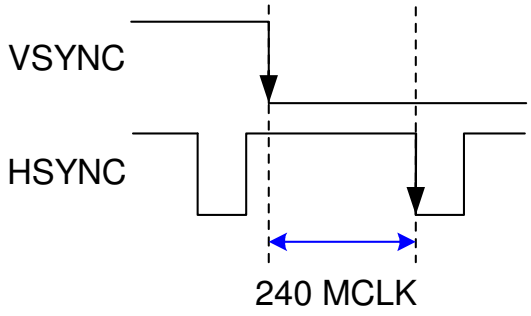
7.3 Setup / Hold Timing chart



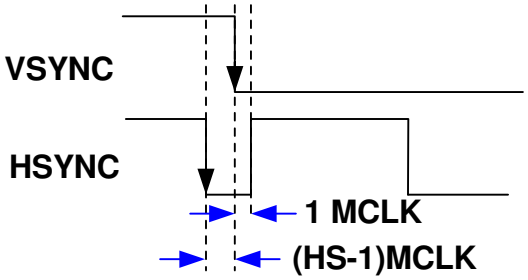


Note1：

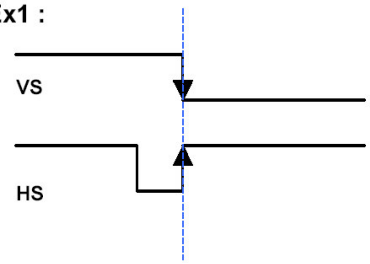
Maximum Timing chart：



Minimum Timing chart：

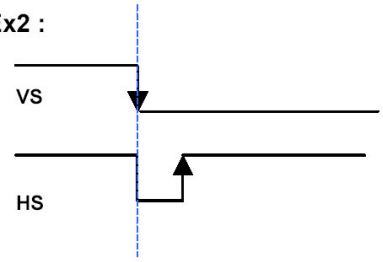


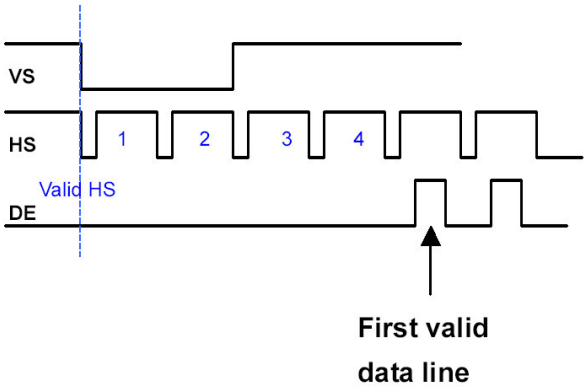
Ex1：



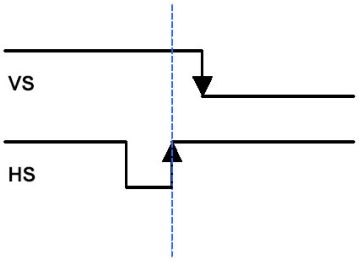
If the VS falling edge and HS rising edge are in the same time, the timing is in the margin and not surely which is the first valid data line.

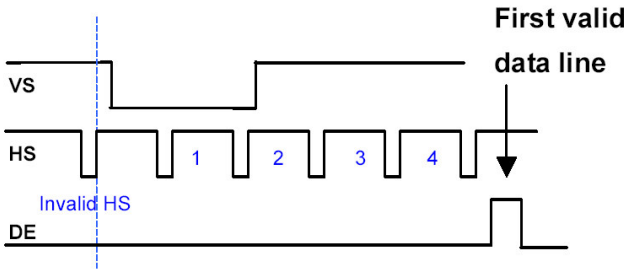
Ex2：





Ex3：





If VS falling edge is delay some time after HS rising edge, this timing will cause the first valid data line delay one HS time.

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	-	-	ns
Vertical Sync. Hold time	tvsyh		20	-	-	ns
Horizontal Sync. Setup time	thsys		20	-	-	ns
Horizontal Sync. Hold time	thsyh		20	-	-	ns
Phase difference of Sync. Signal Falling edge (Note1)	thv	240x320	-(HS-1)	-	240	clk
Clock “L” Period	tckl		75	-	-	ns
Clock “H” Period	tckh		75	-	-	ns
Data setup time	tds		20	-	--	ns
Data Hold time	tdh		20	-	-	ns
DE timing（1）	tdes		-5	—	—	ns
DE timing（2）	tdeh		30	—	—	ns

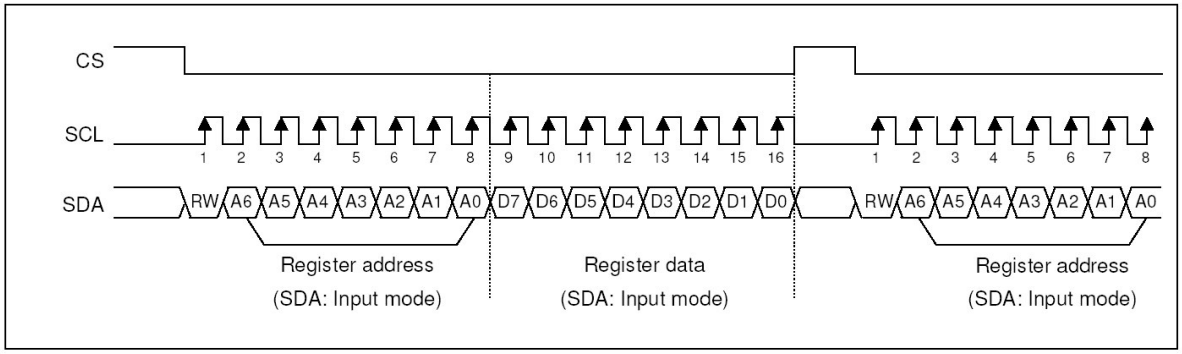
Note: Thv range if it can't meet our spec, just give up first Hsync. It can't impact any side effect.

<SERIAL INTERFACE>

The LCM support the 3-pin serial interface to set internal register. Read/Write bit RW, Serial address A6 to A0 and serial data D7 to D0 are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

Serial interface signal timing chart

Write Mode (RW=L)

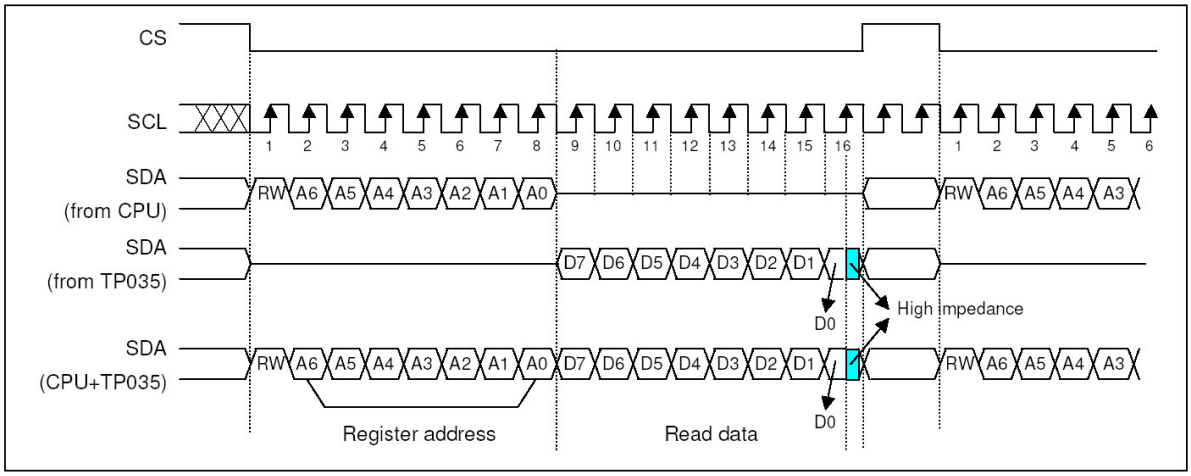


The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommand checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then LCM will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.

Read Mode (RW=H)



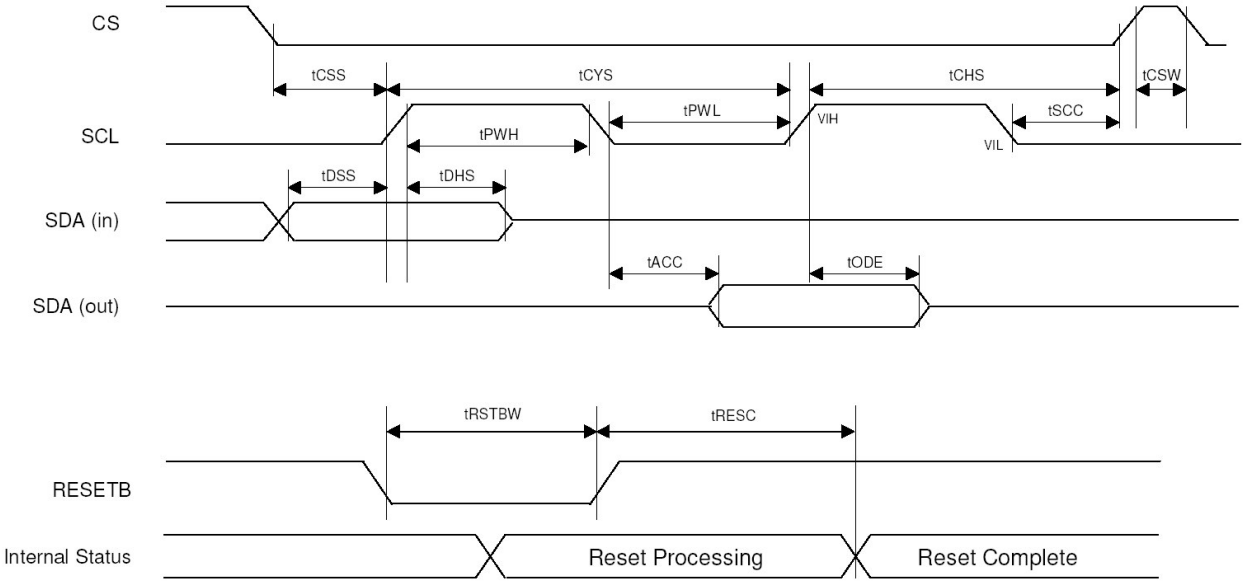
The read mode of the interface means that the micro controller reads data from the LCM.
To do so the micro controller first has to send a command: the read status command.
Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

The LCM samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges.
Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The LCM can read data of the Register0 to Register63

Serial interface and reset waveform (VIH=0.8DVDD，VIL=0.2DVDD)



Serial interface and Reset						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock cycle	tCYS	-	150	-	-	ns
Clock High Period	tPWH	-	60	-	-	ns
Clock Low Period	tPWL	-	60	-	-	ns
Data Set-up Time	tDSS	-	60	-	-	ns
Data Hold Time	tDHS	-	60	-	-	ns
CS High width	tCSW	-	1	-	-	us
CS Set-up Time	tCSS	-	60	-	-	ns
CS Hold Time	tCHS	-	70	-	-	ns
SCL to CS	tSCC		40	-	-	ns
Output Access Time	tACC		10	-	50	ns
Output Disable Time	tODE		25	-	80	ns
RSTB low width	tRSTBW	-	1000	-	-	ns
RESET complete time	tRESC	-	-	-	1000	ns

Command descriptions

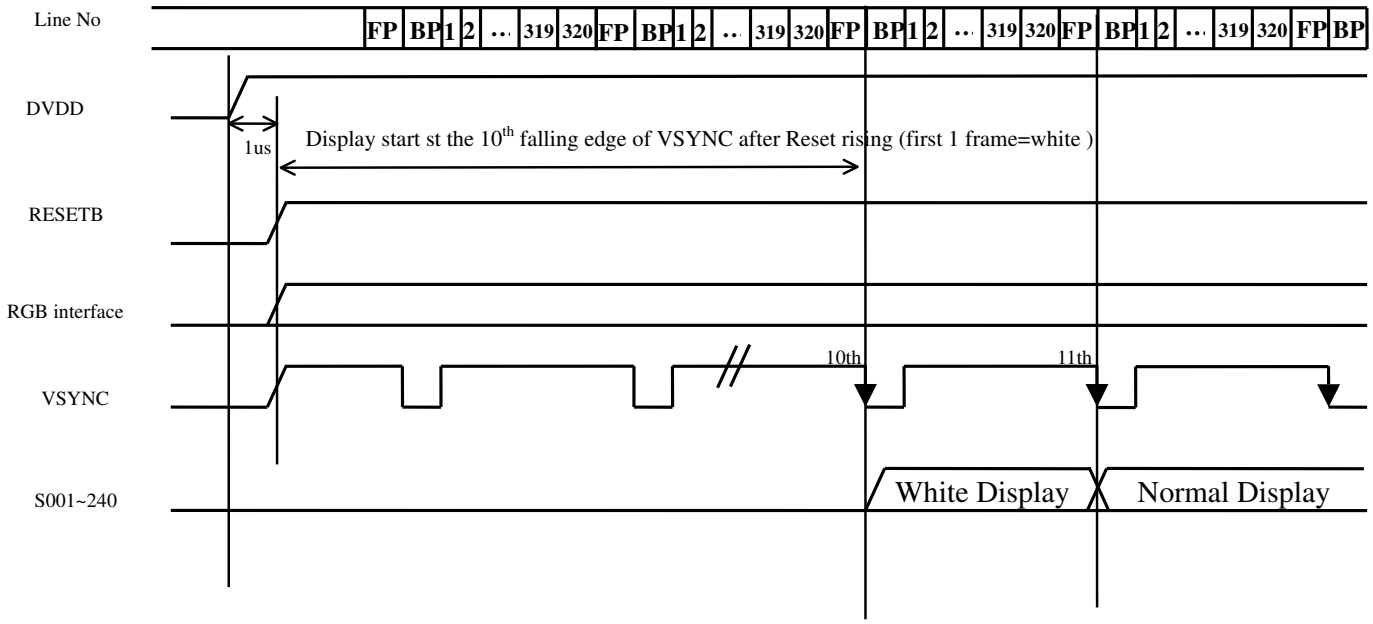
Reset the internal register by setting low level the RESETB pin or software reset command.

Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R0	00h	CHIPID[2:0]									Chip ID (Read only)	The Chip ID can be changed by MASK Option.
			1								D7=1 for SPFD5413	
					0	0	0				ID 0	
					0	0	1				ID 1	
					-	-	-				-	
					1	1	0				ID 6	
					1	1	1				ID 7	
		REVID[2:0]									Revision ID (Read only)	The Revision ID can be changed by MASK Option.
								0	0	0	REV 0	
								0	0	1	REV 1	
								0	1	0	REV2	
								-	-	-	-	
								1	1	1	REV 7	
R1	68h	VCM[7:5]									VCOM amplitude adjustment by VCOMH voltage change at full	VCOMH voltage change at full color mode
			0	0	0						-0.3V	
			0	0	1						-0.2V	
			0	1	0						-0.1V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	
		VCM[3:0]									VCOM voltage select at full color mode	VCOM_DC value setting at full color mode The default value of VCM[3:0] is "1000".
							0	0	0	0	VCOMH=3.90V, VCOML=0.20V	
							0	0	0	1	VCOMH=3.92V, VCOML=0.22V	
							0	0	1	0	VCOMH=3.94V, VCOML=0.24V	
							0	0	1	1	VCOMH=3.96V, VCOML=0.26V	
							0	1	0	0	VCOMH=3.98V,VCOML=0.28V	
							0	1	0	0	VCOMH=4.00V,VCOML=0.30V	
							0	1	0	1	VCOMH=4.02V,VCOML=0.32V	
							0	1	1	1	VCOMH=4.04V,VCOML=0.34V	
							1	0	0	0	VCOMH=4.06V,VCOML=0.36V	
							1	0	0	1	VCOMH=4.08V,VCOML=0.38V	
							1	0	1	0	VCOMH=4.10V,VCOML=0.40V	
							1	0	1	1	VCOMH=4.12V,VCOML=0.42V	
							1	1	0	0	VCOMH=4.14V,VCOML=0.44V	
							1	1	0	1	VCOMH=4.16V,VCOML=0.46V	
							1	1	1	0	VCOMH=4.18V,VCOML=0.48V	
							1	1	1	1	VCOMH=4.20V,VCOML=0.50V	
R2	00h	SYNCP									SYNC polarity select	Mode slection
				0							Negative	
				1							Positive	
		DINT									Input data mapping select	
					0						18 bit interface (262k color)	
					1						16 bit interface (65k color, R:G:B=5:6:5)	
		DCKP									Input clock polarity change	
						0					No change	
						1					Change	
		MSEL									Input Timing Model Select	
									0	0	HS+VS+DE	
									0	1	HS+VS	
									1	X	DE Only	

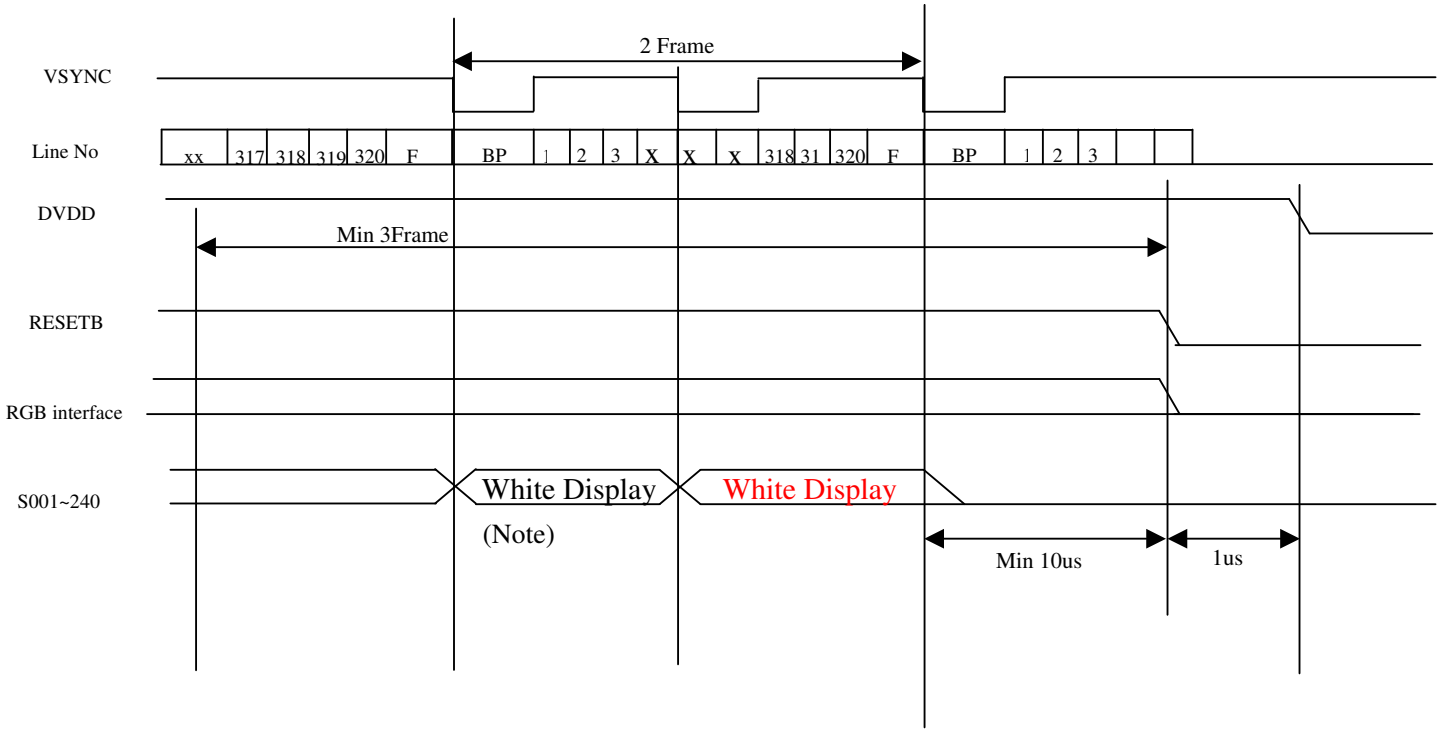
Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R3	04h	VSTS[3:0]									Vertical valid data start time select (VBP)	
							0	0	0	0	2 HSYNC	
							0	0	0	1	2 HSYNC	
							0	0	1	0	2 HSYNC	
							0	0	1	1	3 HSYNC	
							0	1	0	0	4 HSYNC	
							0	1	0	1	5 HSYNC	
							-	-	-	-	-	
							1	1	1	1	15 HSYNC	
R4	1Dh	HSTS[5:0]									Horizontal valid data start time select (HBP)	
				0	0	0	0	0	0	0	10 DCK	
				0	0	0	0	0	1	0	10 DCK	
				0	0	0	0	1	0	0	10 DCK	
				0	0	0	0	1	1	0	10 DCK	
				0	0	0	1	0	0	0	10 DCK	
				0	0	0	1	0	1	0	10 DCK	
				0	0	0	1	1	0	0	10 DCK	
				0	0	0	1	1	1	0	10 DCK	
				0	0	1	0	0	0	0	10 DCK	
				0	0	1	0	0	1	0	10 DCK	
				0	0	1	0	1	0	0	10 DCK	
				0	0	0	1	0	1	1	11 DCK	
				0	0	1	1	0	0	0	12 DCK	
				-	-	-	-	-	-	-	-	
				0	1	1	1	1	0	0	30 DCK	
				-	-	-	-	-	-	-	-	
				1	1	1	1	1	1	1	63 DCK	
R9	C1h	RL									Shift direction (right / left)	
			0								D240 to D1	
			1								D1 t0 D240	
		TB									Shift direction (top / bottom)	
				0							Bottom to top	
				1							Top to bottom	
		CM									Full color or partial color setup	
					0						Normal (262K color)	
					1						Partial(8 color)	
		RESOL[1:0]									Resolution mode select	
						0	0				240 x RGB x 320	
						0	1				176 x RGB x 220	
						1	0				128 x RGB x 160	
						1	1				240 x RGB x 240	
		INVSEL									Invert mode eclect	
								0			Line inversion	
								1			Frame inversion	
		STV1									STV1(single / main panel) signal control	
									0		STV1 signal output	
									1		STV1 signal not output	
		STV2									STV2(dual / sub panel) signal control	
										0	STV2 signal output	
										1	STV2 signal not output	
R10	00h	CMDR									Software reset	
										0	Normal	
										1	Software reset	

8. Power On/Off Sequence

8.1 Power On Sequence



8.2 Power Off Sequence



Note: To avoid image retention , please input white image for two frame before power off.

9. Optical Characteristics

9.1 Optical Specification

9.1.1 Backlight Off

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11(R)		CR ≥ 2	35	45	-	Degree	Note 9-1
	Θ12(L)			25	35	-		
	Θ21(U)			35	45	-		
	Θ22(D)			35	45	-		
Chromaticity	White	x	Θ=0°	0.275	0.310	0.345	-	Note 9-3
		y		0.290	0.330	0.370	-	
Contrast Ratio	CR		Θ=0°	5:1	10:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	5	10	-	%	Note 9-4

9.1.2 Back light On

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11(R)		CR ≥ 10	40	45	-	Degree	Note 9-1
	Θ12(L)			35	40	-		
	Θ21(U)			55	60	-		
	Θ22(D)			30	35	-		
Response Time	Tr+Tf		Θ=0°	-	35	50	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	90:1	150:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F=20mA	125	150	-	cd/m^2	Note 9-7
NTSC	-		-	40	45	-	%	Note 9-7
Uniformity	-		-	75	80	-	%	Note 9-8
Chromaticity	Red	x	Θ=0°	0.533	0.568	0.603	-	Note 9-9
		y		0.305	0.345	0.385		
	Green	x		0.265	0.300	0.335		
		y		0.529	0.569	0.609		
	Blue	x		0.111	0.146	0.181		
		y		0.093	0.133	0.173		
	White	x		0.260	0.295	0.330		
		y		0.283	0.323	0.363		

9.2 Basic measure condition

9.2.1 Driving voltage

VDD= 12.0V, VEE=-6.5V

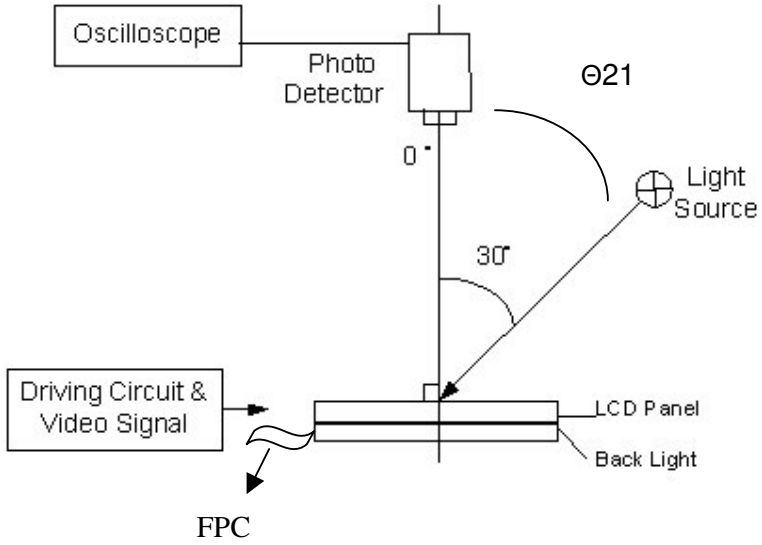
9.2.2 Ambient temperature: Ta=25℃

9.2.3 Testing point: measure in the display center point and the test angle Θ=0°

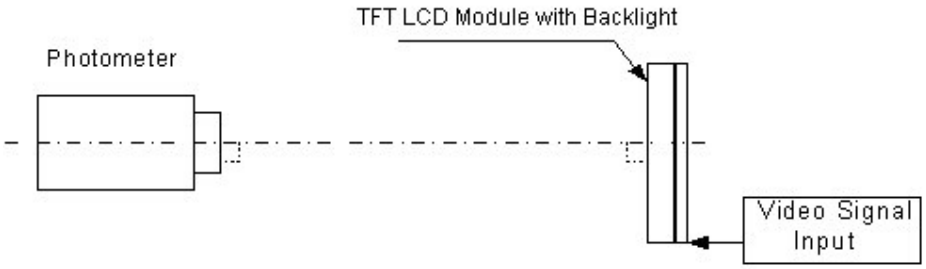
9.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

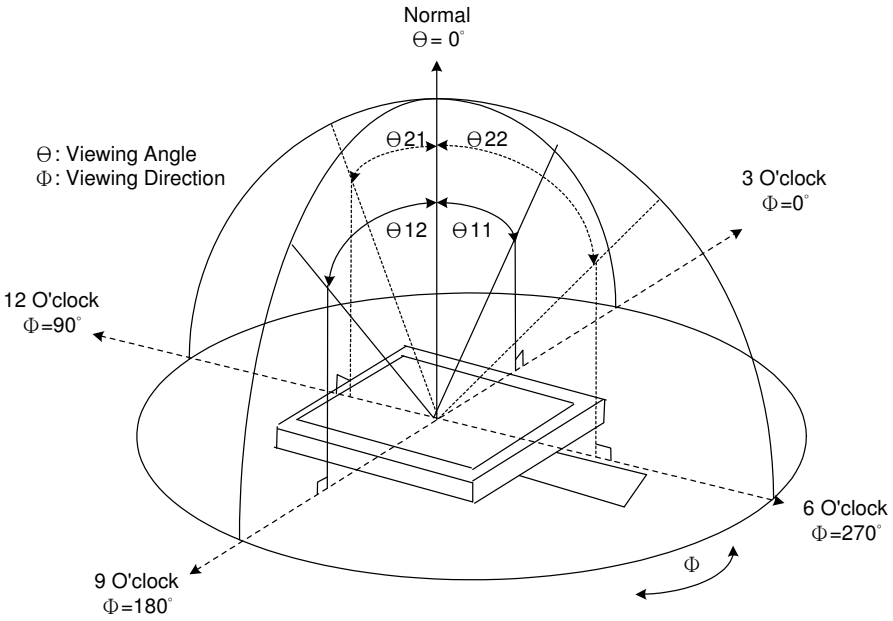
A. System A



B. System B



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

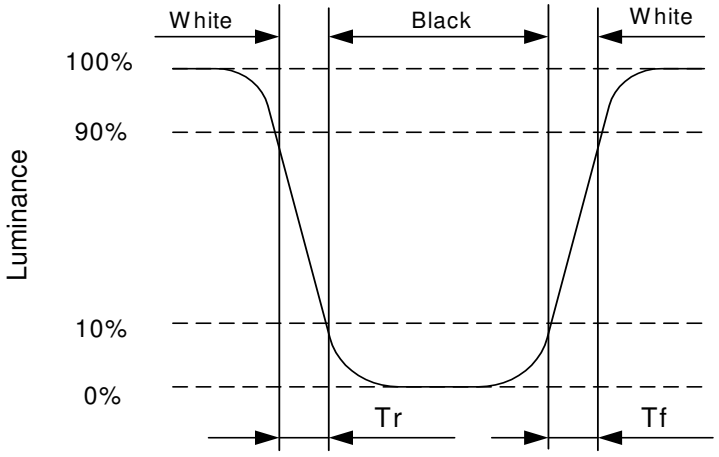
Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system A, calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \text{ X } \text{Reflectance factor of reflectance standard}$$

Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light on (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

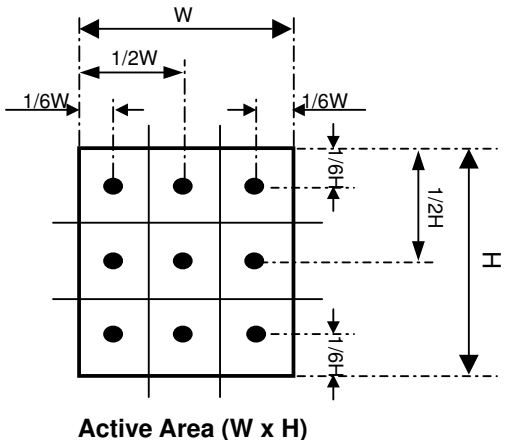
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

Note 9-9: White chromaticity as back light on (Measure System B)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃ ← → 70℃, 50 cycles 30 min 30 min
7	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times
10	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R8 HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
11	Writing Friction Resistance Test (Touch Panel)	Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35mm 100000 times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

11.1.1 In handling LCD panel, please wear gloves with non -charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

11.1.2 The machine and working table for the panel should have ESD protection strategy.

11.1.3 In handling the panel, ionized airflow decreases the charge in the environment is necessary.

11.1.4 In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

11.2.1 Working environment of the panel should be in the clean room.

11.2.2 Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

11.3 Touch panel

11.3.1 The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

11.3.2 When any dust or stain is observed on a film surface, clean it using a glass lens cleaner for something similar.

11.4 Others

11.4.1 Turn off the power supply before connecting and disconnecting signal input cable.

11.4.2 Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

11.4.3 Water drop on the surface or condensation as panel power on will corrode panel electrode.

11.4.4 As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

11.4.5 In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand s cleanly with water and soap as soon as possible.

11.5 Design notes on touch panel

11.5.1 Explanation of each boundary of touch panel

A .Boundary of Double-sided adhesive

a. Electrically detectable within this zone.
When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B .Viewing area

a. Cosmetic inspection to be done for this area.

This area is set as inside of boundary of double-sided adhesive with tolerance.

C .Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

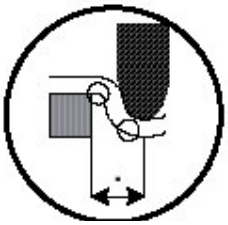
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

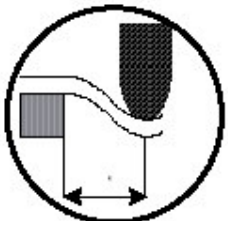
D .Active area

a. This area is where the performance is guaranteed.

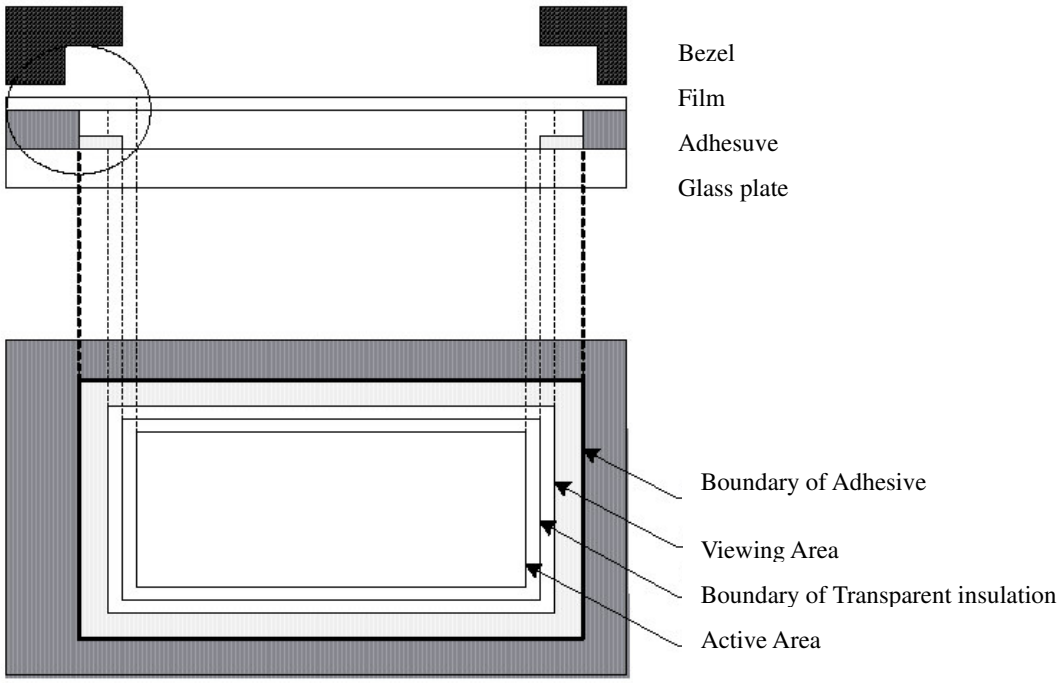
This area set as 2.3mm inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.



Th There is some possibility to damage ITO



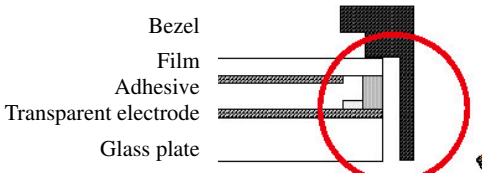
No Damage to ITO



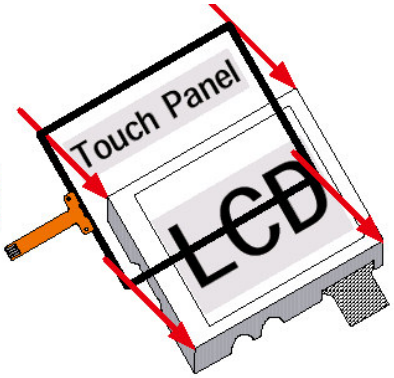
11.5.2 Housing and touch panel

A. Please have clearance between the side of touch panel and any conductive material such as metal frame (Drawing.1). Transparent electrode exists on glass of touch panel from end to end.

B. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause the malfunction.



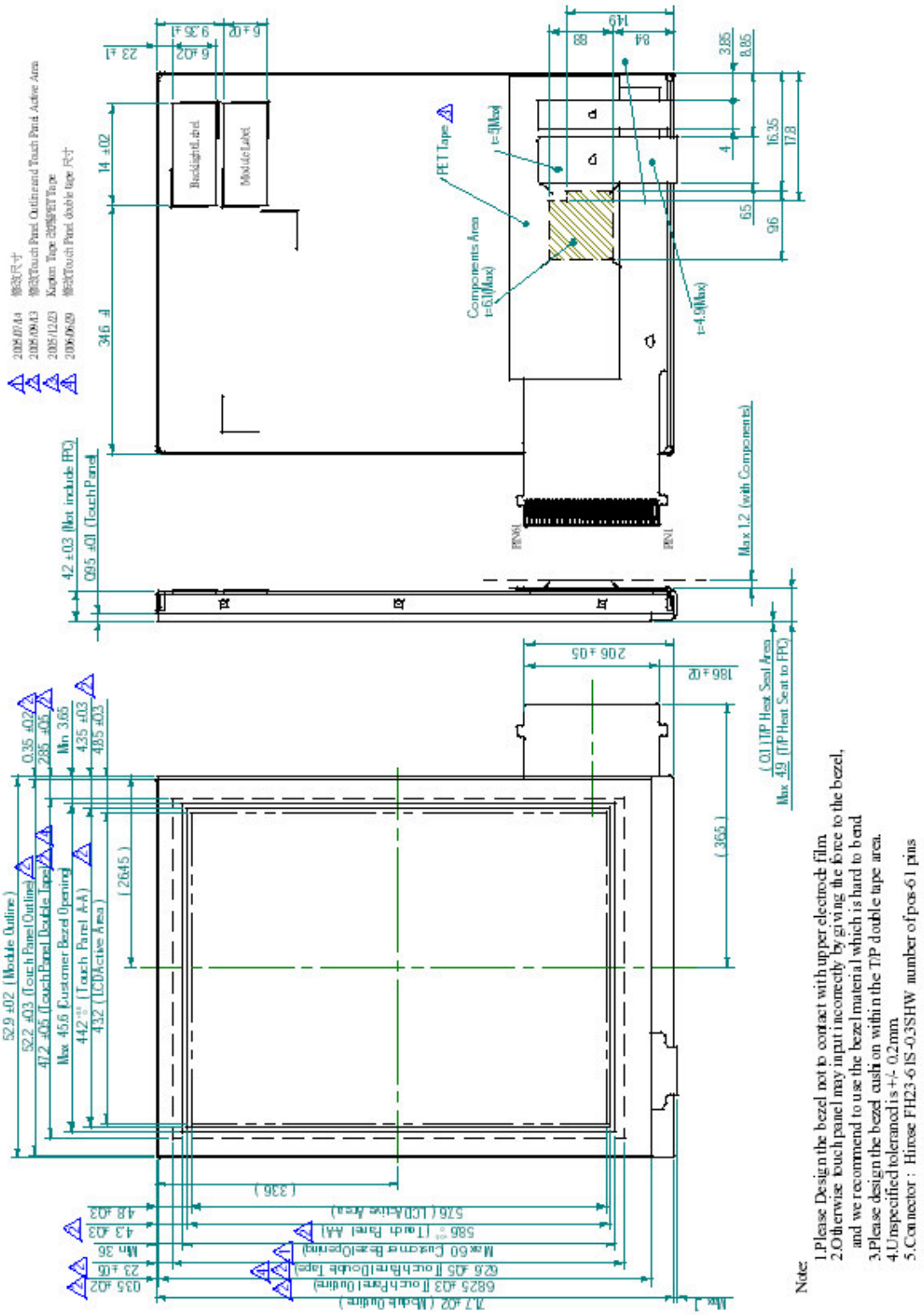
Drawing 1



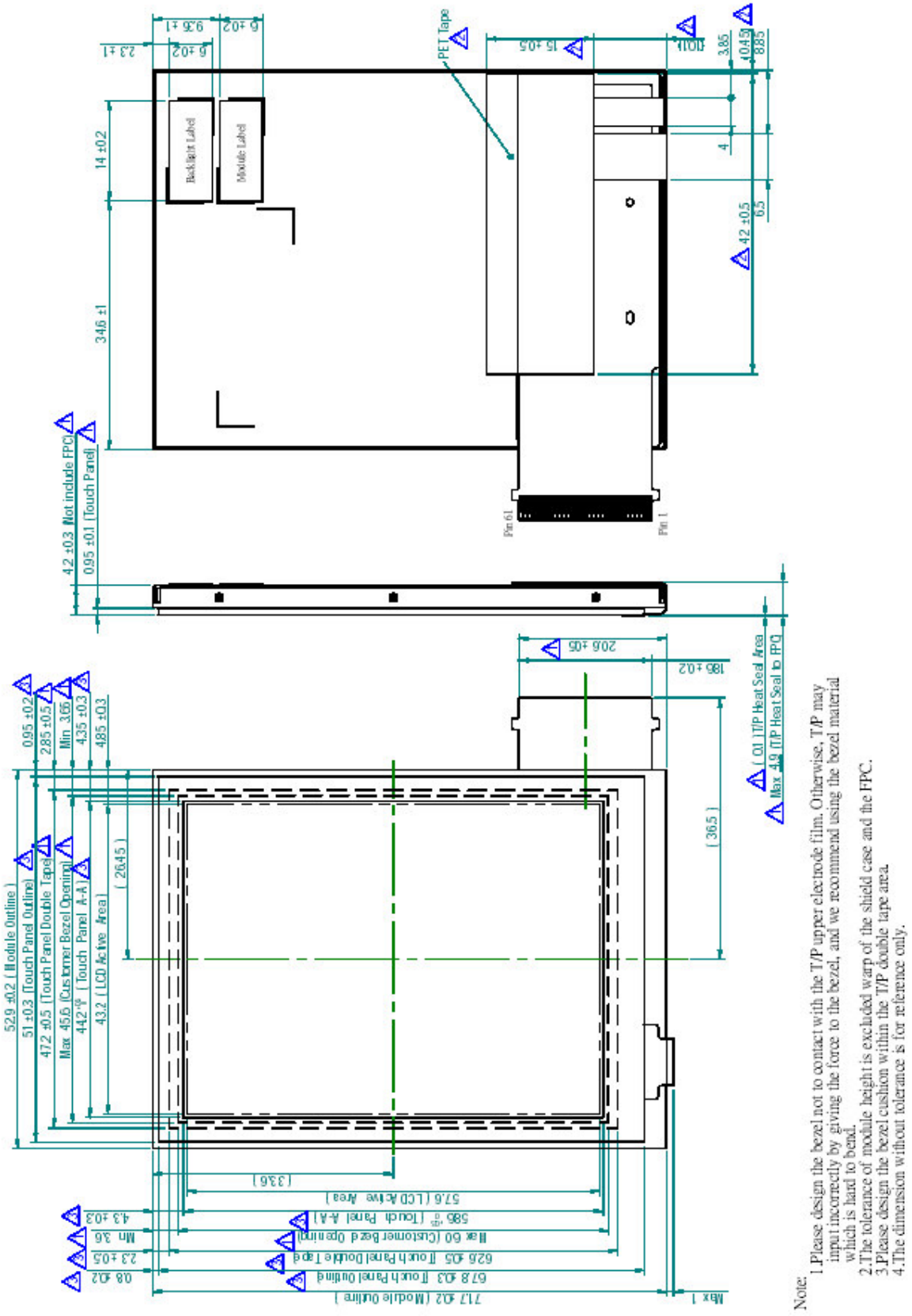
Drawing 2

12. Mechanical Drawing

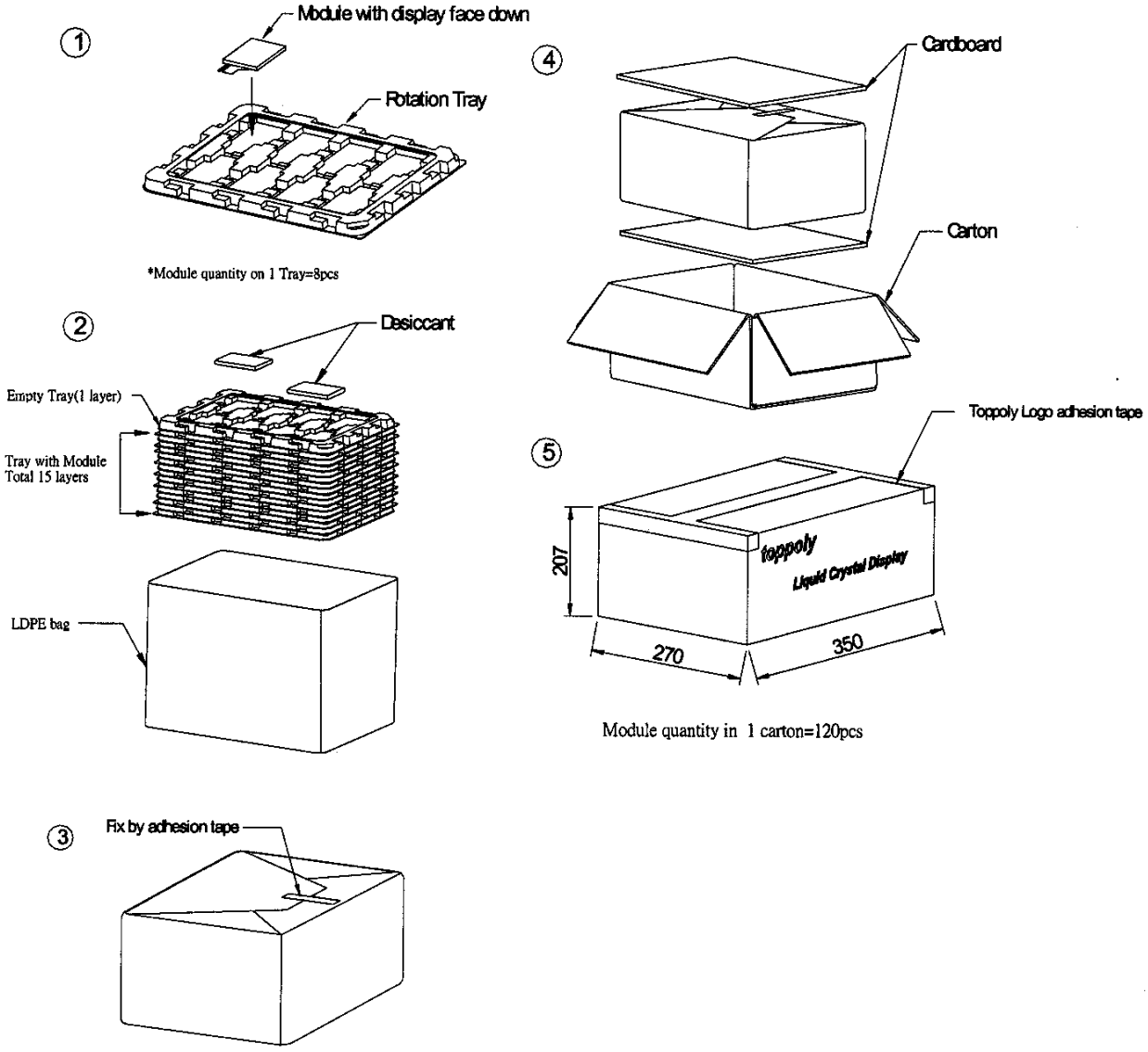
12.1 with source A T/P



12.2 with source B T/P



13. Packing Drawing



TD028STEB2 Module Delivery Packing Instruction:

(1) Module packed into tray cavity with panel face down.

(2) Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
Then put 2pcs desiccant above the empty tray.

(3) Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4) Put 1pcs cardboard inside the carton bottom, and pack the finished package into the carton.
Then put 1pcs cardboard above the packing finished good.

(5) Carton sealing with adhesive tap.