Tentative

LTPS LCD Specification

Model Name: TD028THEB1

Customer Signature
Date

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issue Date	Description
0.00	Jun 30, 2006	New create.
0.01	Aug. 9, 2006	Page 8, Modify backlight driving reference table
0.02	Sep. 6, 2006	Page 29, Modify module drawing
0.03	Sep. 18, 2006	Page 29, Modify module drawing

1 FEATURES

The 2.8” LCD module is the active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel.
Both of horizontal and vertical scan are reversible and controlled by the serial interface commands.
The product is designed for the requirement of the green product, and the specification complies with Toppoly’s “Green Product Chemical Substance Specification Standard Hand Book”.

2 GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	2.8	Inch
Display Type	Transmissive	-
Active Area (HxV)	56.19 x 41.76	mm
Number of Dots (HxV)	960 x 240	dot
Dot Pitch (HxV)	0.0585x0.174	mm
Color Arrangement	RGB Delta	-
Color Numbers	16Million	-
Outline Dimension (HxVxT) *	66.3x48.5x2.68	mm
Weight	16.8+/-1	g
Panel surface treatment	Hard Coating (3H)	-

*Exclude FPC and protrusions.

3 INPUT/OUTPUT TERMINALS

3.1 TFT LCD Panel

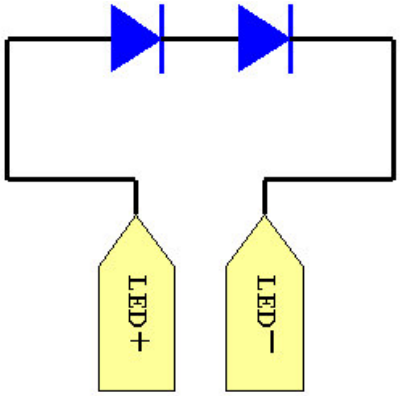
Recommend connector:

Compatible with JAE IL-FHJ-39S-HF-A1

Pin	Symbol	I/O	Description	Remark
1	CP3	C	Capacitor for power setting	
2	CP4	C	Capacitor for power setting	
3	CP5	C	Capacitor for charge pump	
4	CP6	C	Capacitor for charge pump	
5	CP7	C	Capacitor for charge pump	
6	CP8	C	Capacitor for charge pump	
7	DUMMY	--	Dummy	
8	DUMMY	--	Dummy	
9	PCD	C	Capacitor for pre-charge data signal high	
10	VCOML	C	Capacitor for VCOM low	
11	VCOMH	C	Capacitor for VCOM high	
12	AGND	--	Analog ground	
13	DUMMY	--	Dummy	
14	AVDD	C	Regulation capacitor for analog voltage	
15	CP1	C	Capacitor for charge pump	
16	CP2	C	Capacitor for charge pump	
17	PWM	O	Power transistor gate signal for the boost converter	
18	FB	I	Main boost regulator feedback input.	
19	LED-	--	LED power: cathode	
20	LED+	--	LED power: anode	
21	DUMMY	--	Dummy	
22	GND	--	Ground	
23	VCC	--	Power supply for digital circuit and charge pump circuit	
24	VSYNC	I	Vertical sync input. Negative polarity	
25	HSYNC	I	Horizontal sync input. Negative polarity	
26	DCLK	I	Clock signal, latch data onto line latches at the rising edge	
27	DIN0	I	Data input	
28	DIN1	I	Data input	
29	DIN2	I	Data input	
30	DIN3	I	Data input	
31	DIN4	I	Data input	

32	DIN5	I	Data input	
33	DIN6	I	Data input	
34	DIN7	I	Data input	
35	SDA	I/O	Serial interface data line	
36	SCL	I	Serial interface clock line	
37	SCEN	I	Serial interface chip enable line	
38	SHDB	I	Shutdown input	
39	GREST	I	System reset pin	

Note 3-1: The figure below shows the connection of backlight LED.



4. ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

Item	Symbol	MIN	MAX	Unit	Remark
Logic Power Supply Voltage	V_{CC}	-0.5	4.5	V	
Input Signal Voltage	V_{IN1}	0	V_{CC}	V	VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB
Back Light Forward Current	I_F	--	25	mA	
Operating Temperature	T_{OPR}	-10	+60	℃	
Storage Temperature	T_{STG}	-30	+80	℃	

5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		V_{CC}	2.7	3.0	3.6	V	Note 5-1
Input Signal Voltage	Low Level	V_{IL}	GND	-	0.2x Vcc*	V	VSYNC, HSYNC, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, nRESET
	High Level	V_{IH}	0.8x Vcc*	-	V_{CC}*	V	
PWM Output Voltage Level		V_{PWM}	0	-	V_{CC}*	V	
Feedback Voltage		V_{FB}	0.55	0.6	0.65	V	Note 5-2
Panel Power Consumption		W_P	-	50	-	mW	

Vcc* =Vcc(TYP)

Note 5-1: The Vcc power is provided for overall panel module supply voltage.

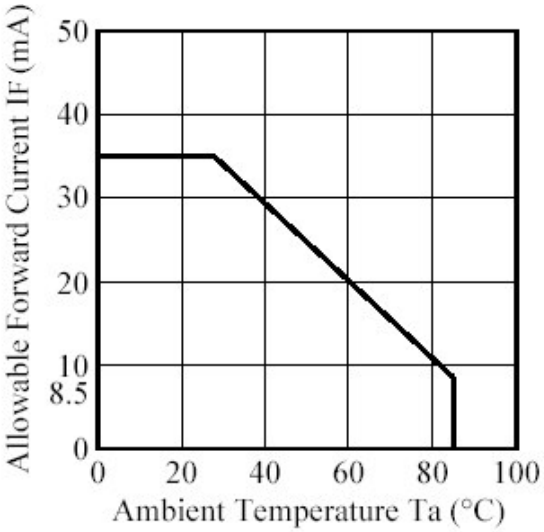
Note 5-2: DC/DC feedback control voltage

5.2 Driving Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	23	25	mA	Note 5-3
Forward Voltage	V_F	--	6.4	7	V	
Backlight Power Consumption	W_{BL}	--	147.2	175	mW	

Note 5-3: Backlight driving circuit is recommended as the fix current circuit.



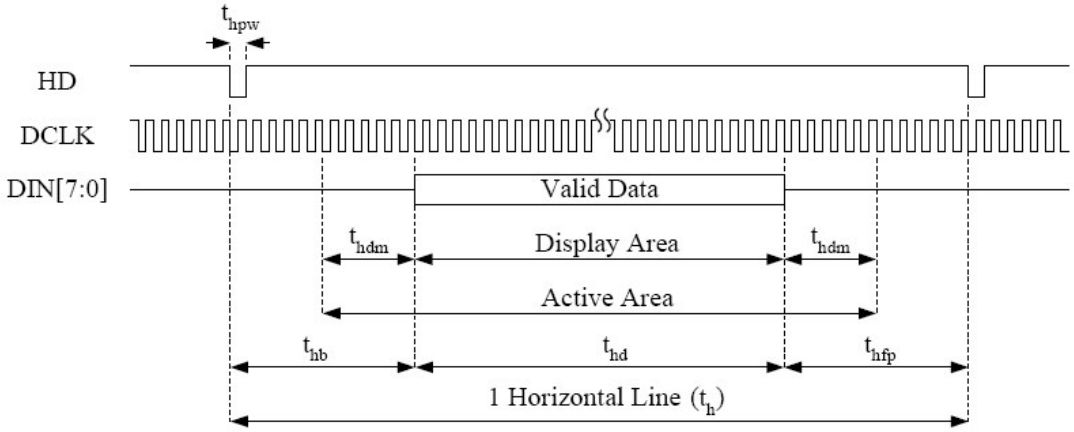
* Ta: Ambient Temperature

* High temperature operation: Test current refers the diagram as following.

* High Temperature & High Humidity Operation: Test current is 15mA.

6. TIMING CHART

6.1 Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Horizontal



(1) YUV Mode: ITUR601-NTSC

Item	Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	F_{DCLK}	-	27	-	MHz
Horizontal Display Active	t_{hd}	-	1440	-	DCLK
Horizontal Total Time	t_h	-	1716	-	DCLK
HSYNC Pulse Width	t_{hpw}	-	1	-	DCLK
Horizontal Back Porch	t_{hp}	-	240	-	DCLK
Horizontal Front Porch	t_{hfp}	-	36	-	DCLK
Dummy	t_{hdm}	-	0	-	DCLK

Item	Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	F_{DCLK}	-	24.54	-	MHz
Horizontal Display Active	t_{hd}	-	1280	-	DCLK
Horizontal Total Time	t_h	-	1560	-	DCLK
HSYNC Pulse Width	t_{hpw}	-	1	-	DCLK
Horizontal Back Porch	t_{hp}	-	240	-	DCLK
Horizontal Front Porch	t_{hfp}	-	40	-	DCLK
Dummy	t_{hdm}	-	0	-	DCLK

(2) YUV Mode: ITUR601-PAL

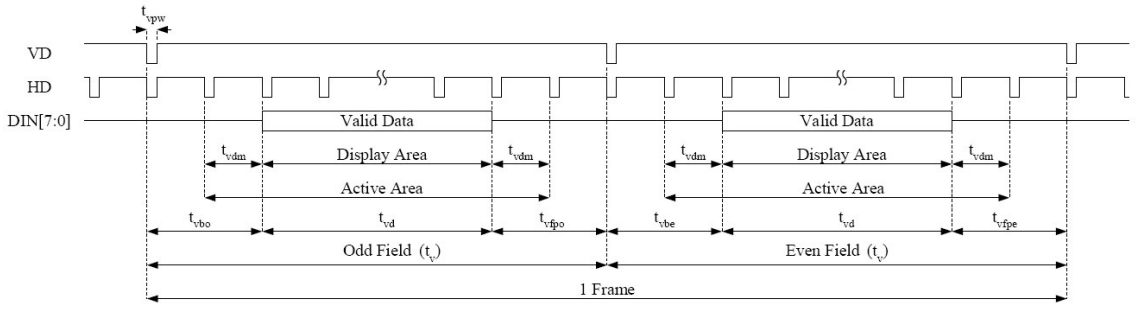
Item	Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	F_{DCLK}	-	27	-	MHz
Horizontal Display Active	t_{hd}	-	1440	-	DCLK
Horizontal Total Time	t_h	-	1728	-	DCLK
HSYNC Pulse Width	t_{hpw}	-	1	-	DCLK
Horizontal Back Porch	t_{hp}	-	240	-	DCLK
Horizontal Front Porch	t_{hfp}	-	48	-	DCLK
Dummy	t_{hdm}	-	0	-	DCLK

Item	Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	F_{DCLK}	-	24.38	-	MHz
Horizontal Display Active	t_{hd}	-	1280	-	DCLK
Horizontal Total Time	t_h	-	1560	-	DCLK
HSYNC Pulse Width	t_{hpw}	-	1	-	DCLK
Horizontal Back Porch	t_{hp}	-	240	-	DCLK
Horizontal Front Porch	t_{hfp}	-	40	-	DCLK
Dummy	t_{hdm}	-	0	-	DCLK

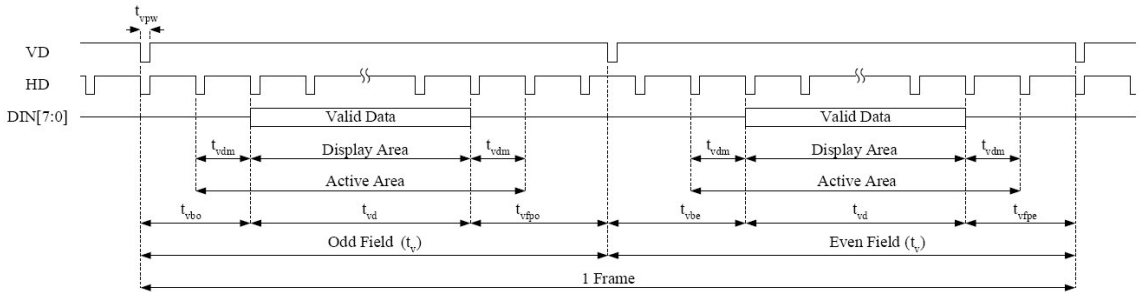
(3) RGB Dummy Mode

Item		Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	QVGA	F_{DCLK}	-	25	-	MHz
	NTSC		-	24.54	-	
	PAL		-	24.38	-	
Horizontal Display Active		t_{hd}	-	1280	-	DCLK
Horizontal Total Time		t_h	-	1560	-	DCLK
HSYNC Pulse Width		t_{hpw}	-	1	-	DCLK
Horizontal Back Porch		t_{hp}	-	240	-	DCLK
Horizontal Front Porch		t_{hfp}	-	40	-	DCLK
Dummy		t_{hdm}	-	0	-	DCLK

6.2 Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Vertical



Non-interlace Mode



Interlace Mode

(1) Non-Interlace Mode: NTSC/QVGA

Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	240	-	Line
Vertical Total Time		t_{v}	-	262	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	21	-	Line
	Even Field	t_{vbe}		21		Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	1	-	Line
	Even Field	t_{vfpe}		1		Line

(2) Non-Interlace Mode: PAL

Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	288	-	Line
Vertical Total Time		t_{v}	-	312	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	24	-	Line
	Even Field	t_{vbe}		24		Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	0	-	Line
	Even Field	t_{vfpe}		0		Line

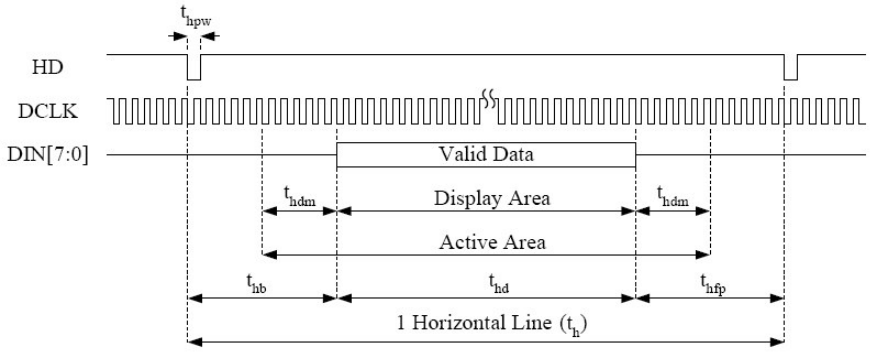
(3) Interlace Mode: NTSC/QVGA

Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	240	-	Line
Vertical Total Time		t_{v}	-	262.5	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	21	-	Line
	Even Field	t_{vbe}		21.5		Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	1.5	-	Line
	Even Field	t_{vfpe}		1		Line

(4) Interlace Mode: PAL

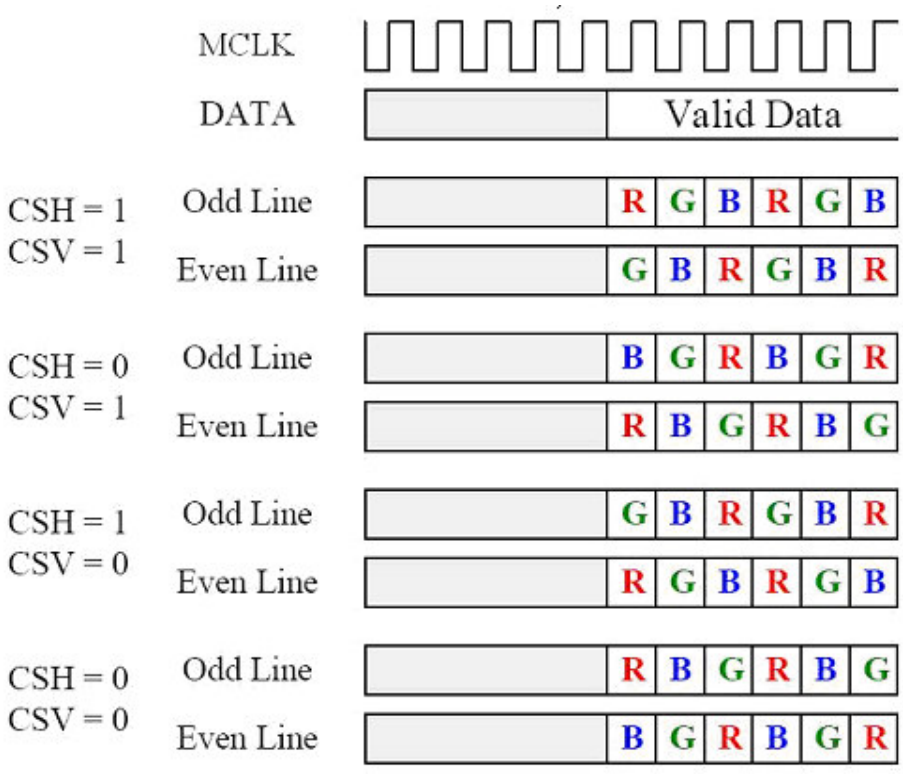
Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	288	-	Line
Vertical Total Time		t_{v}	-	312.5	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	24	-	Line
	Even Field	t_{vbe}	-	24.5	-	Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	0.5	-	Line
	Even Field	t_{vfpe}	-	0	-	Line

6.3 Through Mode: Horizontal

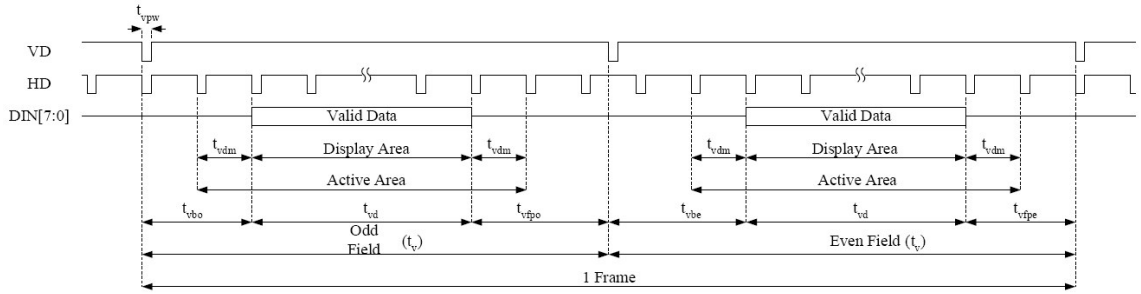


Item	Symbol	MIN	TYP	MAX	Unit
Dot Clock Frequency	F_{DCLK}	-	18.42	-	MHz
Horizontal Display Active	t_{hd}	-	960	-	DCLK
Horizontal Total Time	t_h	-	1171	-	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	-	DCLK
Horizontal Back Porch	t_{hp}	-	152	-	DCLK
Horizontal Front Porch	t_{hfp}	-	59	-	DCLK
Dummy	t_{hdm}	-	0	-	DCLK

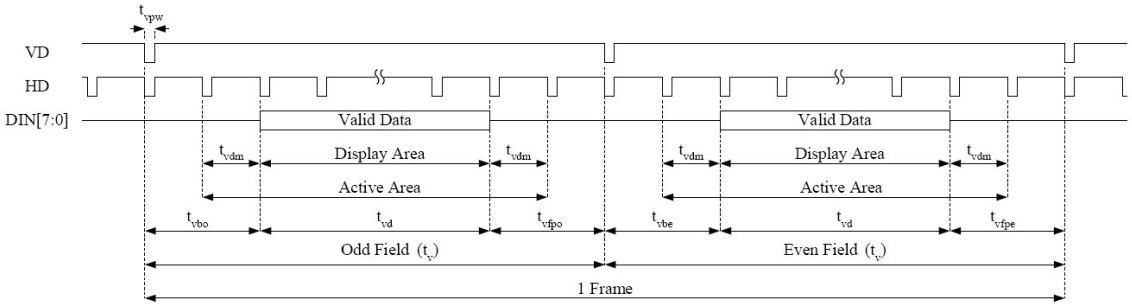
6.4 RGB Input Data Sequence



6.5 Through Mode: Vertical



Interlace Mode



Non-Interlace Mode

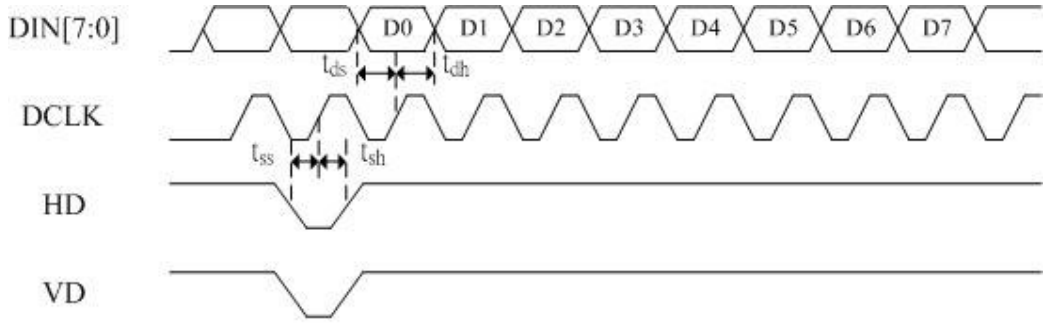
(1) Non-Interlace Mode

Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	240	-	Line
Vertical Total Time		t_v	-	262	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	14	-	Line
	Even Field	t_{vbe}	-	14	-	Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	8	-	Line
	Even Field	t_{vfpe}	-	8	-	Line

(2) Interlace Mode

Item		Symbol	MIN	TYP	MAX	Unit
Vertical Display Active		t_{vd}	-	240	-	Line
Vertical Total Time		t_v	-	262.5	-	Line
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vertical Back Porch	Odd Field	t_{vbo}	-	14	-	Line
	Even Field	t_{vbe}	-	14.5	-	Line
Vertical Front Porch	Odd Field	t_{vfpo}	-	8.5	-	Line
	Even Field	t_{vfpe}	-	8		Line

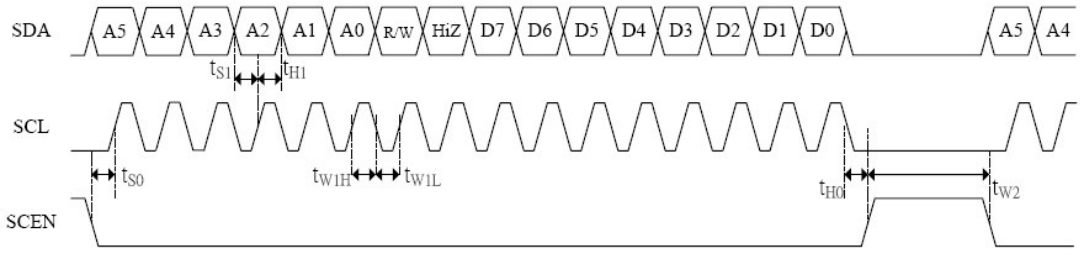
6.6 Setup Time and Hold Time



Item	Symbol	MIN	TYP	MAX	Unit
DCLK Duty Ratio	Duty	40	-	60	%
Data Setup Time	t_{ds}	12	-	-	ns
Data Hold Time	t_{dh}	12	-	-	ns
Control Signal Setup Time	t_{ss}	12	-	-	ns
Control Signal Hold Time	t_{sh}	12	-	-	ns

7. SERIAL INTERFACE

3.1 3 wires Serial data transfer format



Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDA Setup Time	t_{S0}	SCEN to SCL	150			ns
	t_{S1}	SDA to SCL	150			ns
SDA Hold Time	t_{H0}	SCEN to SCL	150			ns
	t_{H1}	SDA to SCL	150			ns
Pulse Width	t_{W1L}	SCL pulse width	160			ns
	t_{W1H}	SCL pulse width	160			ns
	t_{W2}	SCEN pulse width	1.0			us
Clock duty			40	50	60	%

Remark:

1) Only when SCL is input in 16-bit clock while LOAD is in the "Low" period, DATA is accepted at rise of LOAD.
2) If SCL is in 15-bit or 17-bit clock while SCEN is in the "Low" period, SDA is not accepted.
   It is necessary DCLK input for SDA setting
3) Items are set at fall of the vertical sync.

3-wire control register list

Address	Default	Read/Write	Meaning
0x01	0xC1	R	[7:4]: Chip ID [3:0]: Chip version
0x02	0x09	R/W	[1:0]: Input data format [2]: format standard [3]: Valid data for RGBDm or YUV mode [4]: Input clock latch data edge [5]: HD polarity [6]: VD polarity
0x03	0x00	R/W	[0]: Select of interlace mode [1]: Select of field mix

			[3:2]: YCbCr sequence [7:6]:VCOM inversion method selection
0x04	0x0F	R/W	[0]: Power management [1]: CP_CLK output on/off [2]: PWM output on/off [3]: Pr-charge on/off [5:4]: Output driver capability
0x05	0x2B	R/W	[0]: Horizontal reverse mode [1]: Vertical reverse mode [2]: Color filter selection for 960x240 [6:3]: Sample and hold phase
0x06	0x18	R/W	[5:0]: Horizontal start position for through mode
0x07	0x68	R/W	[3:0]: Vertical start position for through mode [6:4]: Resolution selection [7]: Resolution select for Hardware or Software. (0:Hardware, 1:Software)
0x08	0x00	R/W	[5:0]: ENB negative position
0x09	0x20	R/W	[5:0]: Gain of contrast
0x0A	0x20	R/W	[5:0]: R gain of sub-contrast
0x0B	0x20	R/W	[5:0]: B gain of sub-contrast
0x0C	0x10	R/W	[5:0]: Offset of brightness
0x0D	0x00	R/W	[3:0]: Last Channel Gray Level Offset
0x10	0x35	R/W	[5:0]: Vcom high level
0x11	0x38	R/W	[5:0]: Vcom low level
0x12	0x1D	R/W	[5:0]: PCD level
0x14	0x98	R/W	[3:0]: GAMAA0 of gamma Correction [7:4]: GAMA28 of gamma Correction
0x15	0x9A	R/W	[3:0]: GAMA60 of gamma Correction [7:4]: GAMA93 of gamma Correction
0x16	0xA9	R/W	[3:0]: GAMA125 of gamma Correction [7:4]: GAMA157 of gamma Correction
0x17	0x99	R/W	[3:0]: GAMA190 of gamma Correction [7:4]: GAMA222 of gamma Correction
0x18	0x08	R/W	[3:0]: GAMA255 of gamma Correction

<Input format standard>

R02[1:0]	0	1(Default)	2
Input Format	RGBDummy	YUV	Through mode

R02[2]	0(Default)	1
Format standard	NTSC/QVGA	PAL

R02[3]	0	1(Default)
Valid data for RGBDm or YUV	1280	1440

<Input data and clock>

R02[4]	0(Default)	1
Latch data edge	Positive Edge	Negative

R02[5]	0(Default)	1
HD Polarity	Low pulse	High pulse

R02[6]	0(Default)	1
VD Polarity	Low pulse	High pulse

R03[0]	0(Default)	1
Interlace Mode	Interlace	Non-interlace

R03[1]	0(Default)	1
Even Field Blanking	L2=L1	L2=L1-1

R03[3:2]	0(Default)	1	2	3
YcbCr sequence	CbYCrY	YcrYCb	CrYCbY	YcbYCr

YUV input transfer matrix

$$\begin{cases} R=1.16(Y-16)+1.60(Cr-128) \\ G=1.16(Y-16)-0.81(Cr-128)-0.39(Cb-128); \ [Y=16\sim235, Cr \ \&Cb=16\sim240] \\ B=1.16(Y-16)+2.02(Cb-128) \end{cases}$$

<VCOM inversion method selection>

R03[7:6]	0(Default)	1	2	3
VCOM inversion method	One Line inversion	Two Line inversion1	One Line in-version2	Mix inversion mode

<Power management>

R04[0]	0	1(Default)
Low power mode	Standby	Normal

Function pin	DOUT[24:1],PCD, VCOM, PWM	CP_CLK1, CP_CLK2	CKV, CKH, ENB	STV, STH, XCKH, PCG

Standby	LOW	CP_CLK1=”AVDD”, CP_CLK2=”L”	High	Low

R04[1]	0	1(Default)
CP_CLK	Disable	Enable
* Disable: CP_CLK1 = “H”, CP_CLK2 = “L”		

R04[2]	0	1(Default)
PWM	Disable	Enable

R04[3]	0	1(Default)
Pre-charge	Disable	Enable

R04[5:4]	0(Default)	1	2	3
Driver capability	50%	100%	150%	200%

<Direction Control>

R05[0]	0	1(Default)
Horizontal reverse	Reverse	Normal

R05[1]	0	1(Default)
Vertical reverse	Reverse	Normal

<Color filter selection for 960x240>

(Strip mode support for two color 960x240 panel only)

R05[2]	0(Default)	1
Color filter	Delta	Strip

<Output sample and hold phase>

R05[6:3]	0	1	2	3	4	5 (Default)	6	7	8	9	0xA	0xB	0xC	0xD	0xE	0xF
Output phase	Normal	SH1	SH2	SH3	SH4	SH5	SH6	SH7	SH8	SH9	SH10	SH11	SH12	SH13	SH14	SH15

<Shift display area>

R06[5:0]	0x0	0x18(Default)	0x2D
STH phase	Advance 24 MCLK	Center	Delay left 21 MCLK
Display position	Screen scroll left	Center	Screen scroll Light

R07[3:0]	0x0	0x8(Default)	0xF
STV phase	Advance 8 H	Center	Delay 7H
Display position	Screen scroll up	Center	Screen scroll down

<Resolution Selection>

R07[7]	0x0(Default)	0x01
Function	Hardware	Software

R07[6:4]	0x00	0x02	0x06(Default)	0x07
Resolution	480x240	640x240	960x240(two color)	960x240(same color)

<Gate non-overlap>

R08[5:0]	0x0(Default)	0x3F
ENB negative position	Origin	Shift right 63 DCLK

<Contrast and Brightness>

$D_{contrast} = D_{in} * Gain$, $D_{brightness} = D_{contrast} + Offset$

R09[5:0]	0x00	0x20(Default)	0x3F
Gain of Contrast	0.00000	1.00000	1.96875

R0A[5:0]	0x00	0x20(Default)	0x3F
R gain of Sub-contrast	0.00000	1.00000	1.96875

R0B[5:0]	0x00	0x20(Default)	0x3F
B gain of Sub-contrast	0.00000	1.00000	1.96875

R0C[5:0]	0x00	0x20(Default)	0x3F
B gain of Sub-contrast	0.00000	1.00000	1.96875

<Last channel gray level offset function>

R0D[3:0]	0x00(Default)	0x01	0x02	…	0x0D	0x0E	0x0F
Last channel gray level offset	0	1	2	…	13	14	15

<Voltage level>

$V_{comH} = 2.94 + 0.02 * R10$, $V_{comL} = 1.36 – 0.02 * R11$

R10[5:0]	0x00	0x35(Default)	0x3F
Vcom high level	2.94	4.00	4.20

R11[5:0]	0x00	0x38(Default)	0x3F
Vcom low level	1.32	0.20	0.06

<PCD level>

V_{PCD} = 0.22+ 0.08 * R12

R12[5:0]	0x00	0x1D(Default)	0x2F
PCD level	0.22	2.54	3.98

<Gamma Correction>

$V_{gcH} = V_{gnH} + 0.04*(R_n-8)$, $V_{gcL} = V_{gnL} + 0.04*(8-R_n)$,

R14[3:0]		0x0	0x8(Default)	0xF
GAMA0	VcomH	0.580	0.900	1.180
	VcomL	4.020	3.700	3.420

R14[7:4]		0x0	0x9(Default)	0xF
GAMA28	VcomH	1.237	1.597	1.837
	VcomL	3.363	3.003	2.763

R15[3:0]		0x0	0xA(Default)	0xF
GAMA60	VcomH	1.692	2.092	2.292
	VcomL	2.908	2.508	2.308

R15[7:4]		0x0	0x9(Default)	0xF
GAMA93	VcomH	1.966	2.326	2.566
	VcomL	2.634	2.274	2.034

R16[3:0]		0x0	0x9(Default)	0xF
GAMA125	VcomH	2.174	2.534	2.774
	VcomL	2.426	2.066	1.826

R16[7:4]		0x0	0xA(Default)	0xF
GAMA157	VcomH	2.377	2.777	2.977
	VcomL	2.223	1.823	1.623

R17[3:0]		0x0	0x9(Default)	0xF
GAMA190	VcomH	2.547	2.907	3.147
	VcomL	2.053	1.693	1.453

R17[7:4]		0x0	0x9(Default)	0xF
GAMA222	VcomH	2.759	3.119	3.359
	VcomL	1.841	1.481	1.241

R18[3:0]		0x0	0x8(Default)	0xF
GAMA255	VcomH	3.480	3.800	4.080
	VcomL	1.120	0.800	0.520

8. POWER SEQUENCE

8.1 Power on sequence

Power on (low power mode, global reset) to normal mode sequence

Step1: Wait VCC go stable and then send a low pulse(more then 160us) to GRSTB pad.

A normal command is following GRSTB low pulse.

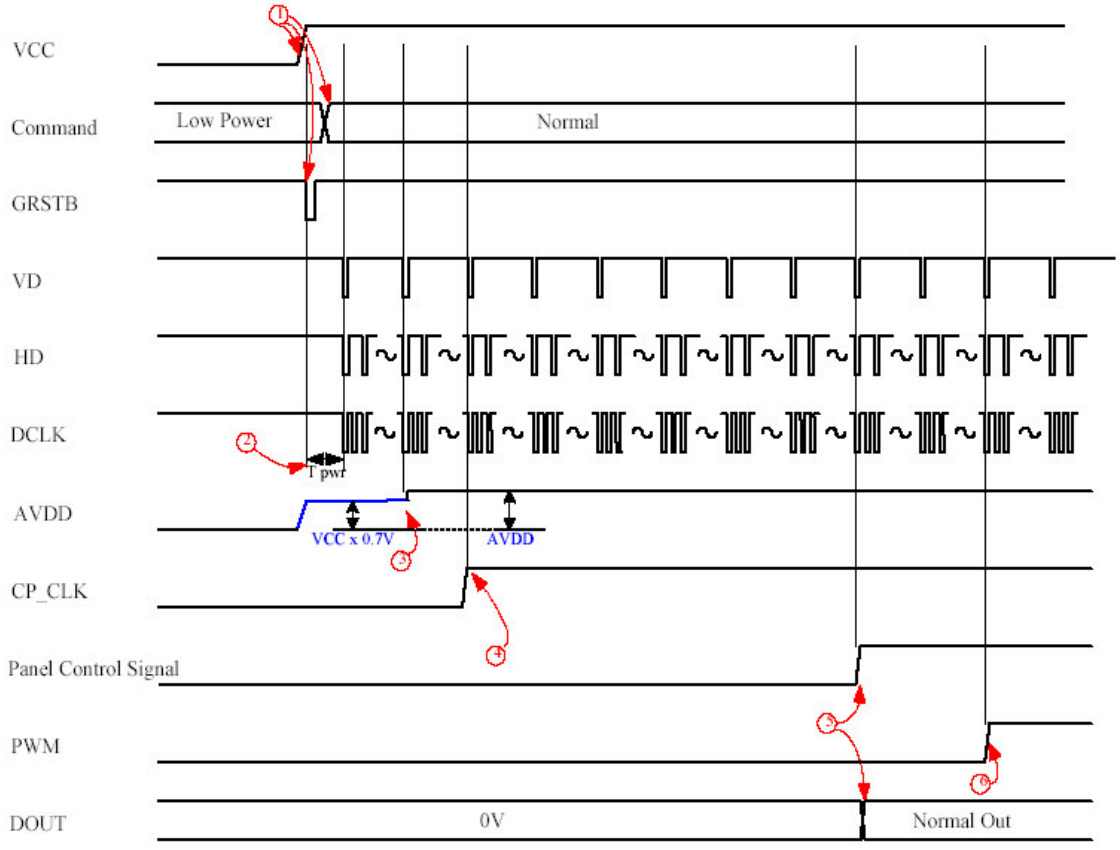
Step2: Before turn on VCC, the VD/HD/DCLK input signal must keep still until Tpwr(2ms).

Step3: AVDD will start when second VD coming.

Step4: CP_CLK will start when third VD coming.

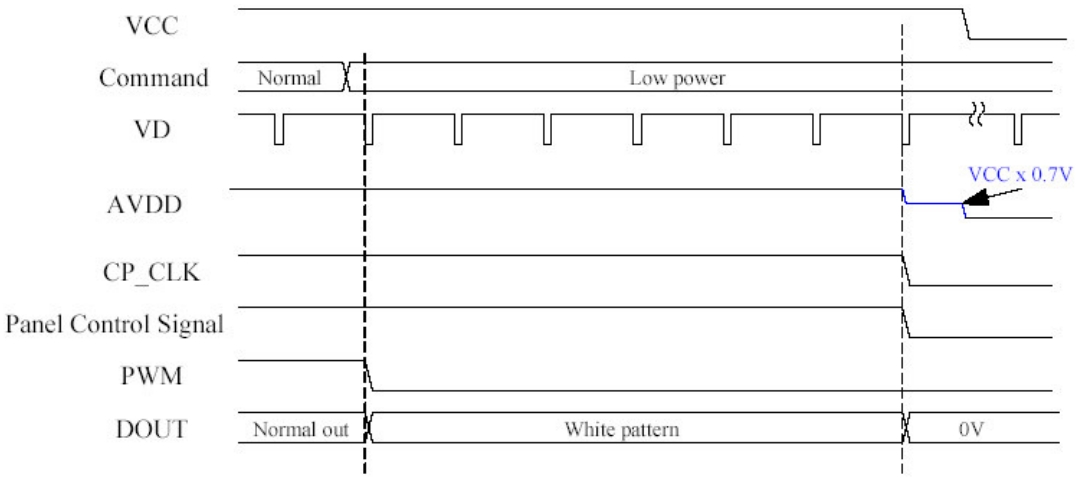
Step5: Panel Control Signal and Normal DOUT will start when ninth VD coming.

Start6: PWM control signal will start when eleventh VD coming.

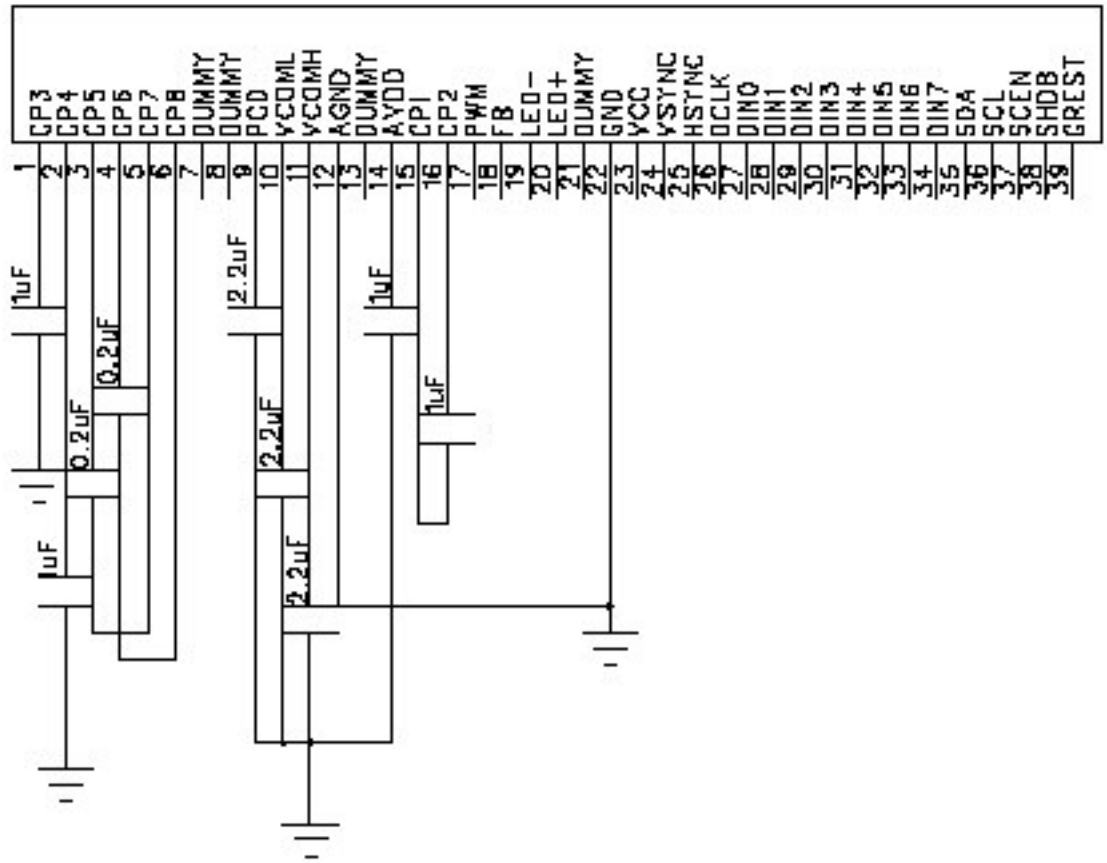


8.2 Power off sequence

(After “Lower Power” command, please keep VCC power on more then 8 VD cycles)



9. APPLICATION CIRCUIT



10. OPTICAL CHARACTERISTICS

10.1 Optical Specification

Ta=25℃

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles		Θ11	CR ≥ 10	30	40	-	Degree	Note 10-1
		Θ12		30	40	-		
		Θ21		15	20	-		
		Θ22		40	50	-		
Contrast Ratio		CR	Θ=0°	200	300	-		Note 10-2
Response Time	Rising	Tr		-	13	20	ms	Note 10-3
	Falling	Tf		-	22	30		
Luminance (I_F=23mA)		L		200	250	-	cd/m^2	Note 10-4
Chromaticity	White	x_W		0.26	0.31	0.36		Note 10-5
		y_W		0.28	0.33	0.38		

10.2 Basic Measure Conditions

(1) Driving voltage

Vcc= 3 V

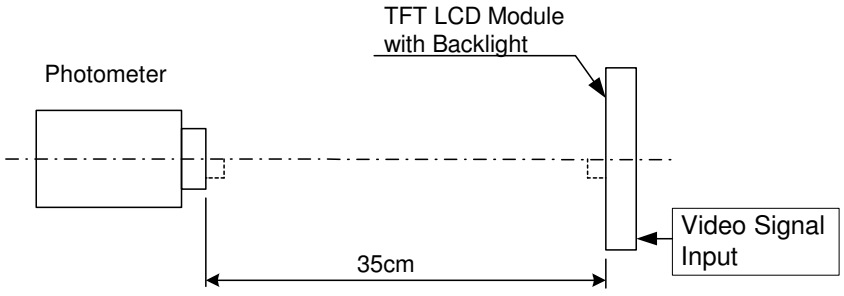
(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle Θ=0°

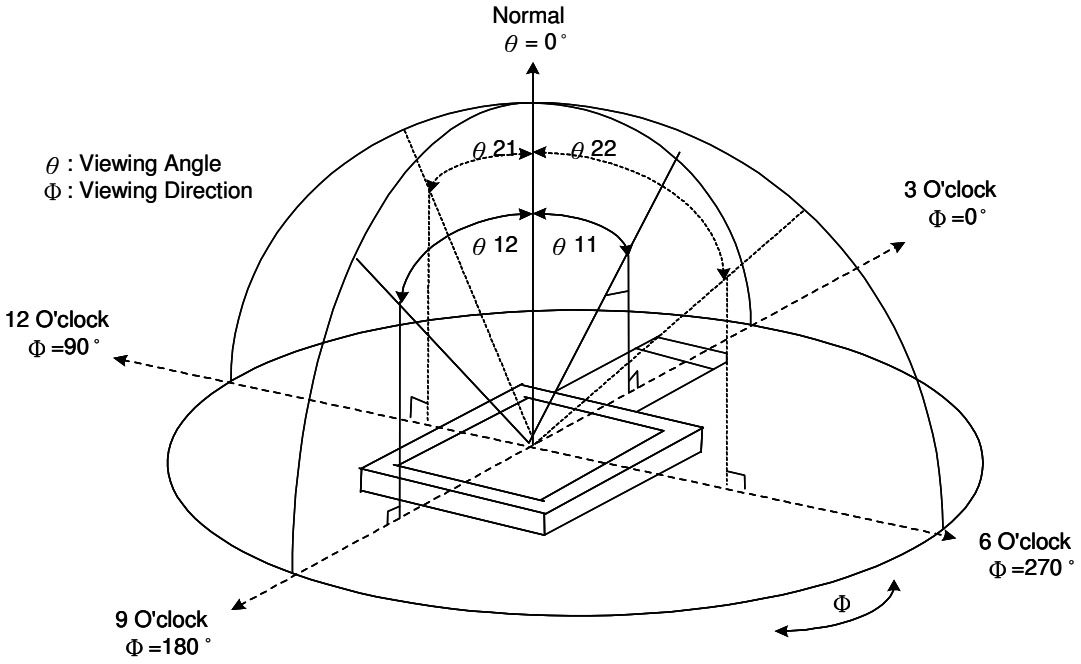
(4) LED Current: I_F=23mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux



Note 10-1: Viewing angle diagrams:

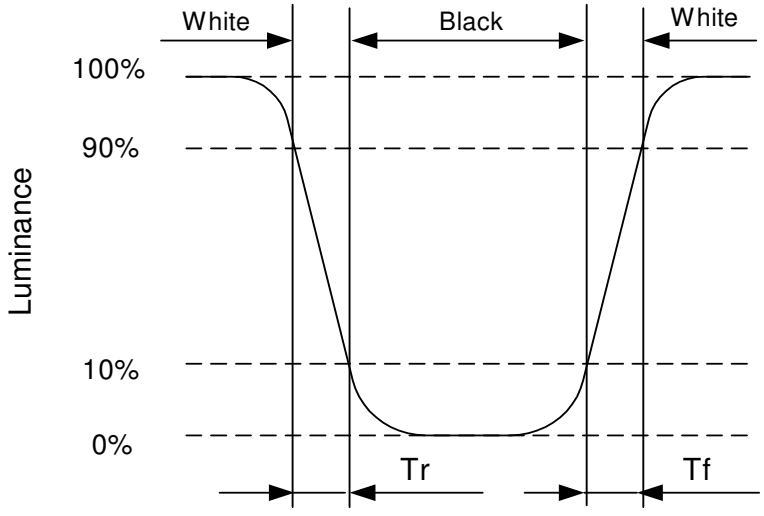


Note 10-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 10-3: Definition of response time:



Note 10-4: Luminance:

Test Point: Display Center

Note 10-5: Chromaticity: The same test condition as Note 10-4.

11. RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta=-10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+80℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta=-30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃←→80℃, 50 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0Ω; Discharge: ±150V 3 times / Terminal
8	Surface Discharge (non-operation)	C=150pF, R=330Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
9	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
10	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Twice

Ta: Ambient Temperature

12. HANDLING CAUTIONS

12.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

12.2 Environment

(1) Working environment of the panel should in the clean room.

(2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

12.3 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

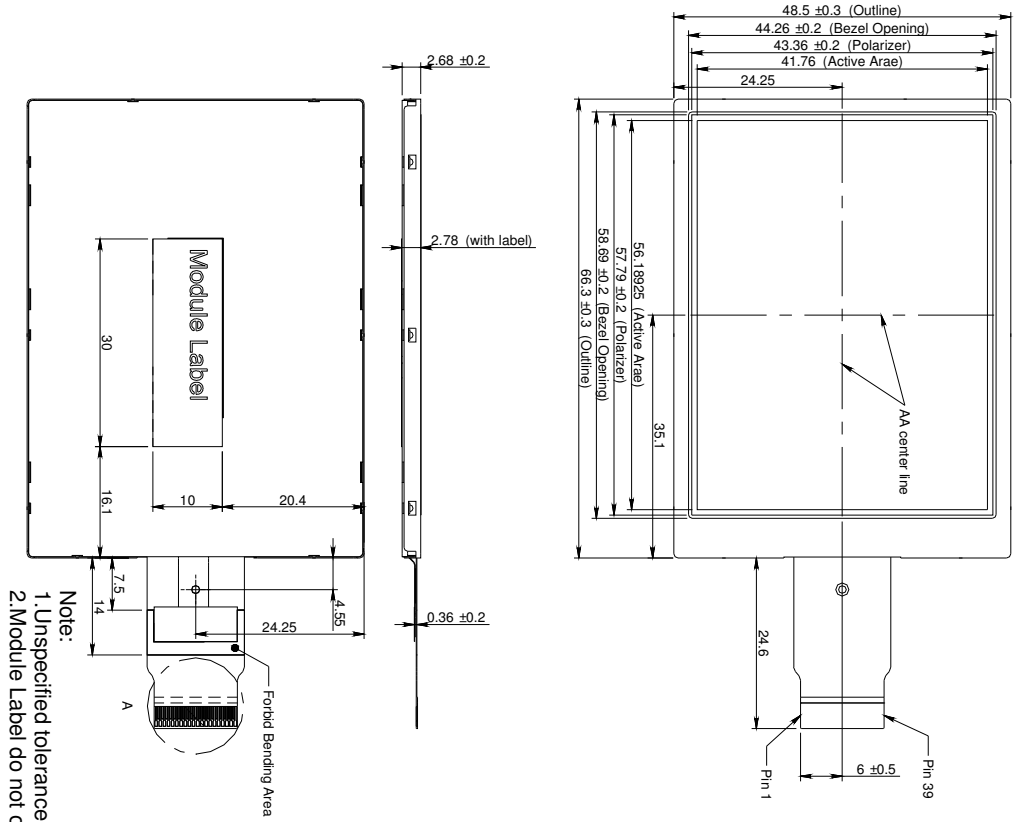
(2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

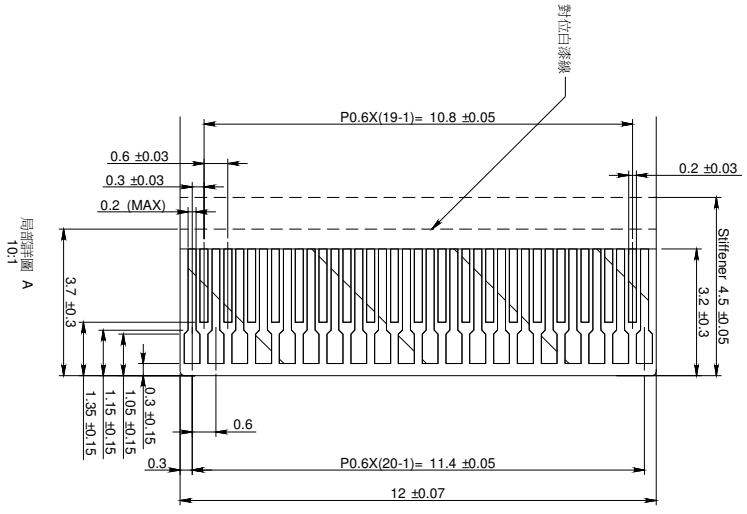
(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

13. MECHANICAL DRAWING

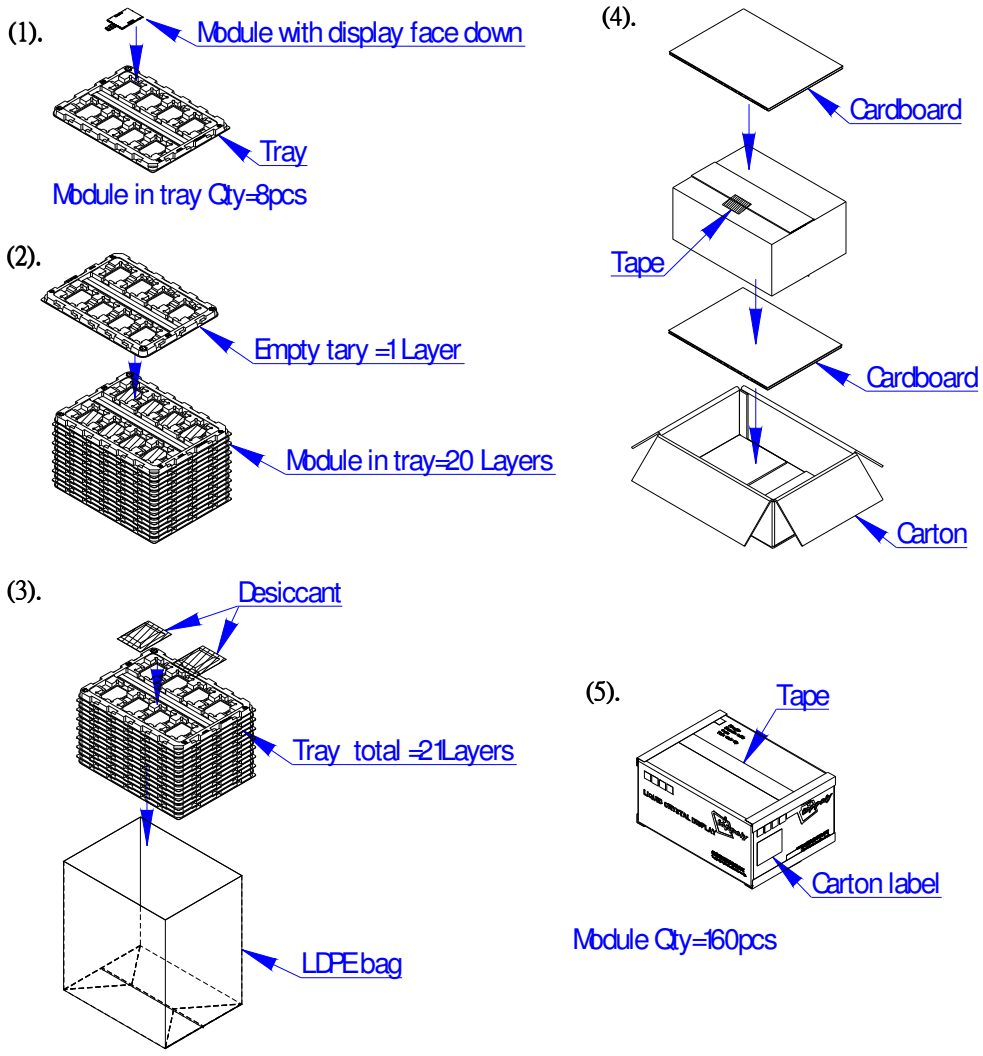


Note:
1.Unspecified tolerance is +/-0.2mm.
2.Module Label do not overlap on the BLU label.



2.8"(real 2.7562")
Resolution:960x240
Dot Pixel:0.0585 mm x 0.174mm

14. Packing Drawing



2.8" module (TD028THEB1) delivery packing method

(1). Module packed into tray cavity (with Module display face down).

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton.
Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.