TFT LCD Specification

Model NO.: TD035STED1

TENTATIVE

Customer Signature
Date

Table of Contents

Record of Reversion

Rev	Issued Date	Description
0.00	DEC, 1,2004	New
0.01	JAN, 7,2005	Update 8.1/8.2 power on/off sequence

1. FEATURES

The 3.5” LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it’s COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (6 bits)	-
Outline Dimension (HxVxT)		64.3 X 87.1X4.35(Max 4.45)*	mm
Weight		47	g
Power consumption	LCD Panel + T-CON + L/S	25 (Typ)	mW
	Backlight	432 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Recommend connector: KYOCERA ELCO 14 5605 060 000 829

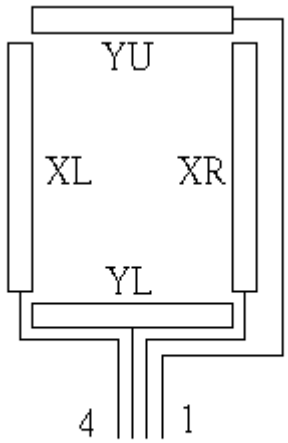
Pin	Symbol	I/O	Description	Remark
1	yU	I	Lower electrode Y (Y-)	
2	xR	I	Lower electrode X (X+)	
3	yL	I	Lower electrode Y (Y+)	
4	xL	I	Lower electrode X (X-)	
5	GND		GND	
6	GND		GND	
7	Vcom_L	O	Negative power output for VCOM	Capacitor for COM voltage
8	Vcom_H	O	Positive power output for VCOM	Capacitor for COM voltage
9	Retain this pin		(ISC)	
10	Retain this pin		(ISVI)	
11	CS	I	Serial interface chip select	
12	Retain this pin		(IV6P)	
13	SDA	I/O	Serial interface data input/output	
14	Vsync	I	Vertical SYNC input	
15	SCL	I	Serial interface clock input	
16	GND		GND	
17	RESETB	I	Reset	P.S. : Reset Circuit (R.C.) , Cap =1uF
18	Hsync	I	Horizontal SYNC input	
19	DC_ENB	I	DC/DC enable/disable select	DC/DC output enable pin L:Enable(on) H:Disable(off) PDA mode
20	VDD1	I	2.8V Input (Logic Supply Voltage)	
21	GND		GND	
22	B00	I	Data Bit Input	
23	B01	I	Data Bit Input	
24	B02	I	Data Bit Input	
25	B03	I	Data Bit Input	
26	B04	I	Data Bit Input	

27	B05	I	Data Bit Input	
28	GND		GND	
29	G00	I	Data Bit Input	
30	G01	I	Data Bit Input	
31	G02	I	Data Bit Input	
32	G03	I	Data Bit Input	
33	G04	I	Data Bit Input	
34	G05	I	Data Bit Input	
35	GND		GND	
36	R00	I	Data Bit Input	
37	R01	I	Data Bit Input	
38	R02	I	Data Bit Input	
39	R03	I	Data Bit Input	
40	R04	I	Data Bit Input	
41	R05	I	Data Bit Input	
42	GND		GND	
43	AVDD	I	5V Input(Source driver)	
44	MCLK	I	Clock signal	
45	VS	O	Positive power output for source driver	Capacitor for VS voltage
46	GND		GND	
47	VS	O	Positive power output for source driver	Capacitor for VS voltage
48	DE	I	Data Enable	
49	GND		GND	
50	GND		GND	
51	CM	I	Full color or partial color mode setup	Full color or partial color mode setup L:262K color H: 8 color partial
52	TB_RL	I	Gate shift direction select and Source shift direction select	Shift direction (Right/Left) H: D1→D240 L: D240→D1 Shift direction (Top/Bottom) H: Top→Bottom L: Bottom→Top
53	INVSEL	I	Driving algorithm select	Invert-mode select L: line inversion H: Frame inversion
54	GND		GND	

55	VDD2	I	2.8V Input(Power supply for booster)	
56	VGH	I	Positive voltalge Positive voltage in pin for Level Shifter I/O	Power Supply (+10V)
57	VVEE	I	Input Voltage for gate off -5.5V	
58	LED(-)	I	Cathode of LED	
59	GND		GND	
60	LED(+)	I	Anode of LED	

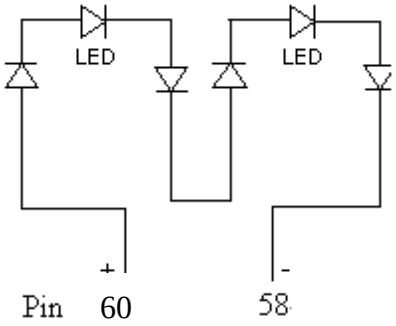
3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	1	YU	Touch Panel Right Side	
2	2	XR	Touch Panel Lower Side	
3	3	YL	Touch Panel Left Side	
4	4	XL	Touch Panel Upper Side	



Pin Assignment for Touch panel

3.3 Back light pin assignment



4. ABSOLUTE MAXIMUM RATINGS

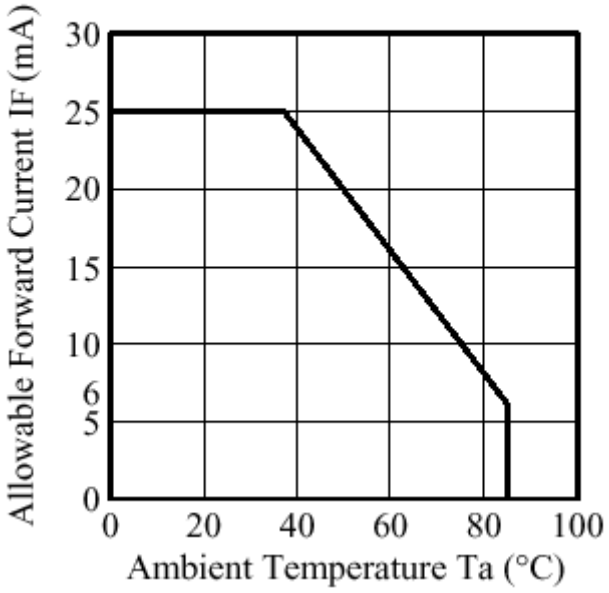
GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD1, VDD2	-0.3	+3.6	V	
	AVDD	-0.3	6	V	
Power Supply for H/V Driver	VGH	-0.3	+19	V	
	VVEE	-5.8	-5.2	V	Note 1
Touch Panel Operation Voltage	V_{Touch}	-	5.5	V	
Backlight LED forward Voltage	V_F	-	24	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	25	mA	Note2
Operating Temperature	Topr	-10	+55	℃	
Storage Temperature	Tstg	-20	+70	℃	

Note1. The operating voltage is between +0.5V and –5.0V at the moment when the power is turned on

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs. Allowable Forward Current



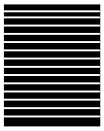
5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

T a=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		VDD1	2.4	2.8	3.0	V	
		VDD2	2.4	2.8	3.0	V	
		AVDD	4.8	5	5.6	V	
Power Supply for H/V Driver		VGH	9.5	10	10.5	V	
		VVEE	-5.8	-5.5	-5.2	V	
Data Input Voltage	High	VIH	0.7VDD1	—	VDD1	V	R[5:0], G[5:0], B[5:0], CLK DE
	Low	VIL	0	—	0.2VDD1		
VDD1,VDD2 Supply Current		I_{VDD1}	-	0.7/0.04	1.7/0.2	mA	Note 1,2
AVDD Supply Current		I_{AVDD}	-	1.65	4.0	mA	Note 3
VGH Supply Current		I_{VDD}	-	0.07	0.2	mA	
VVEE Supply Current		I_{VEE}	-	0.05	0.5	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



Note 2: VDD2 rush current accept 120mA, 500u sec during system booting.

Note 3: Gamma correction voltage is set to achieve the optimum at VCC5=5.0V. Use the voltage at level as close to 5.0V as possible.

5.2 DC/DC Spec

Item	Input voltage			Input Current	Input ripple(Max)	
	MIN	TYP	MAX			
VDD2	2.4V	2.8V	3.0V	0.04	--	
AVDD	4.8V	5V	5.6V	1.65	50 mV	Note 1
VGH	9.5V	10V	10.5V	0.07	150mV	
VVEE	-5.8 V	-5.5 V	-5.2 V	0.05	--	

Note 1: VCC5 is analog voltage supply therefore use as less ripple as possible.

5.3 Driving backlight Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	25	mA	LED/Part
LED Life Time	-	-	10,000	-	Hr	I_F: 15mA
Forward Current Voltage	V_F	-	3.6	4.0	V	I_F: 20mA ,LED/Part

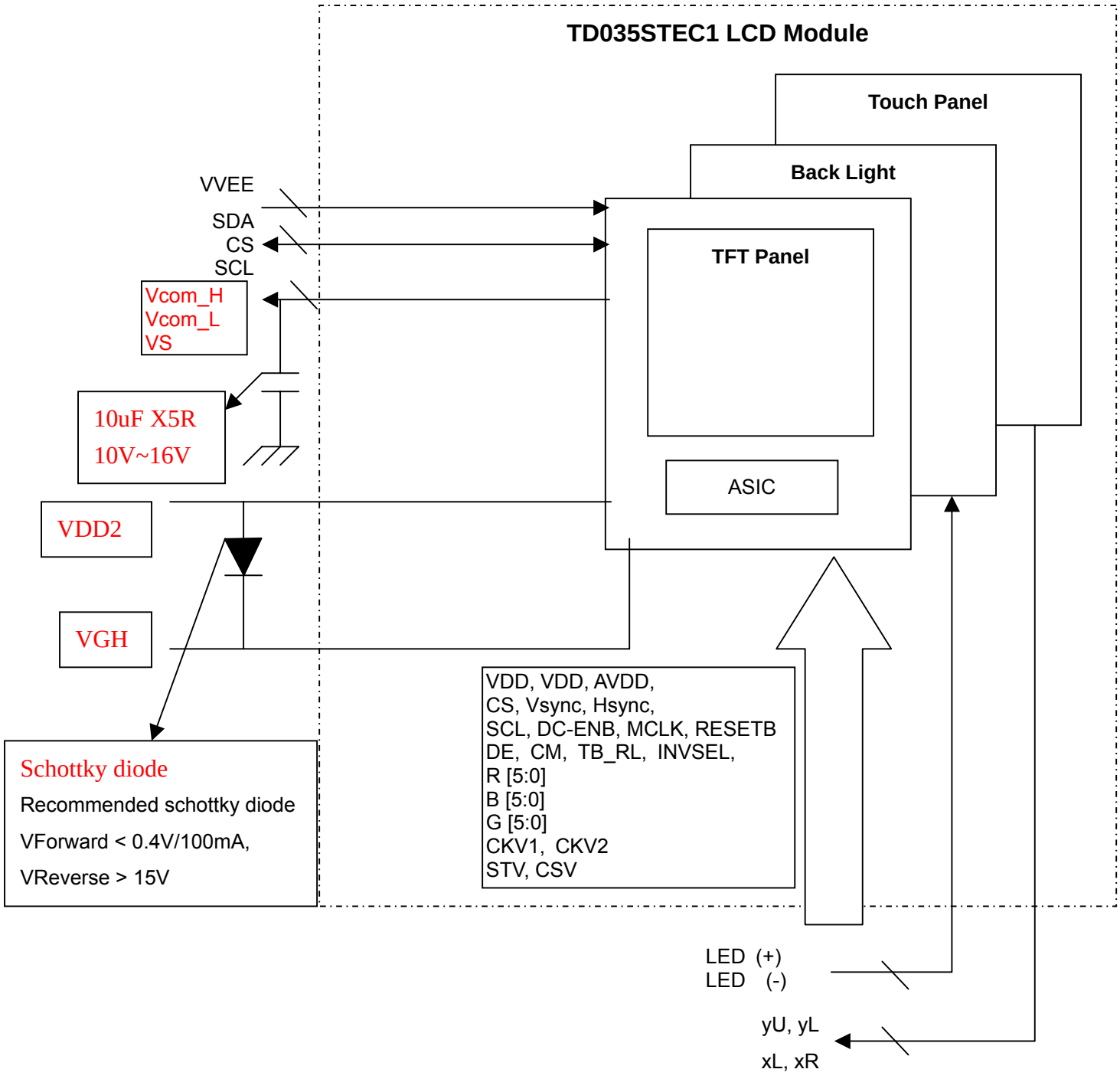
Note : Backlight driving circuit is recommend as the fix current circuit.

5.4 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	100	-	1100	Ω	
Resistor between terminals (YU-YL)	Ry	100	-	1100	Ω	
Operation Voltage	V_{Touch}	-	5	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note 1
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	-	10	ms	
Minimum tension for detecting	-	-	80	-	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note 1. The minimum test force is 80 g.

6. BLOCK DIAGRAM



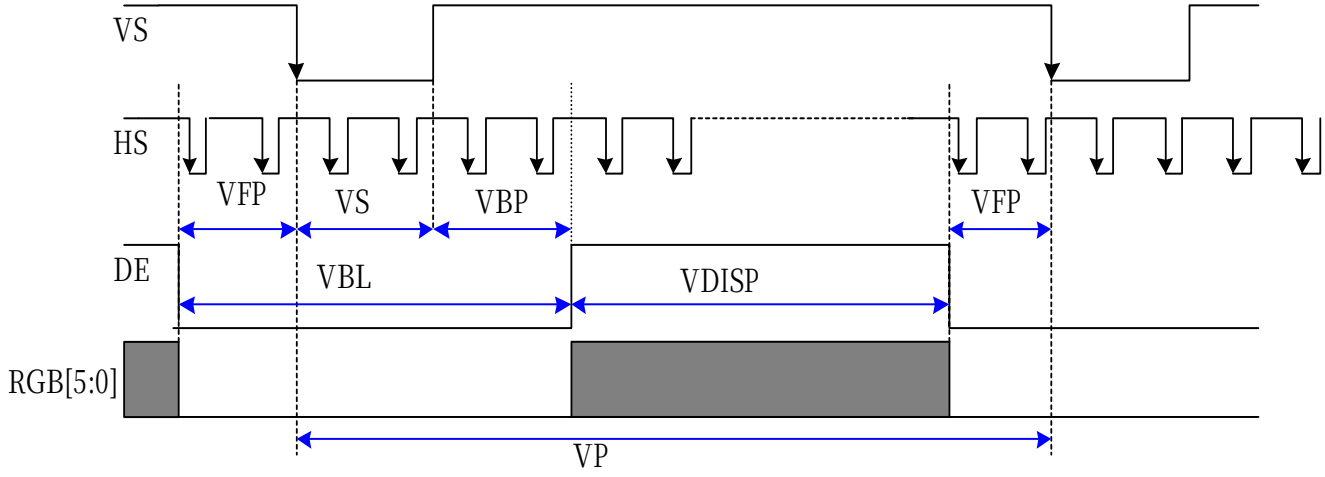
7. TIMING CHART

7.1 Display timing

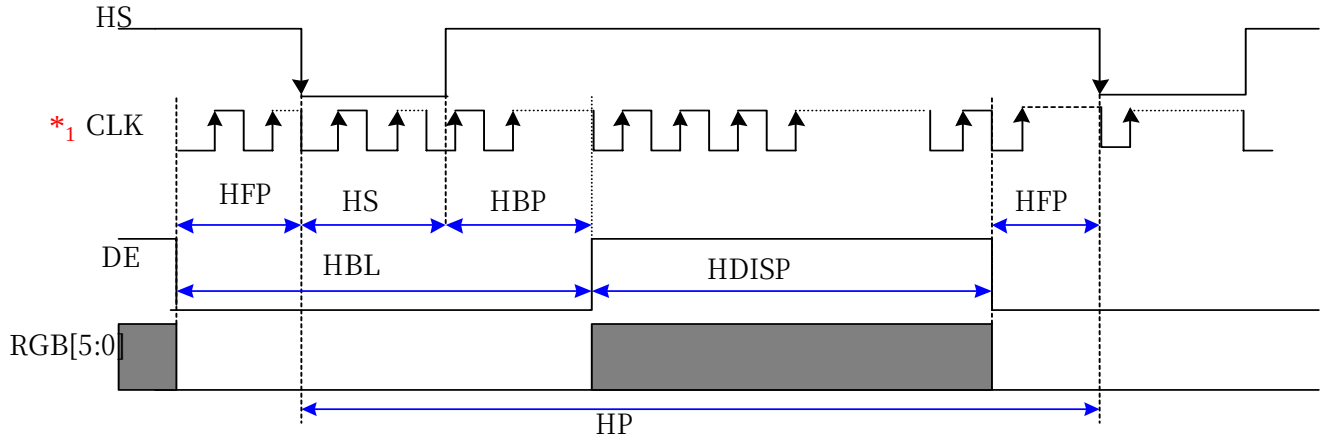
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		323	326	340	Line
	Vertical data start	VDS	VS+VBP	2	4	—	Line
	Vertical front porch	VFP		1	2	—	Line
	Vertical blanking period	VBL	VS+VBP+VFP	3	6	—	Line
	Vertical active area	VDISP		—	320	—	Line
	Horizontal cycle	HP		260	280	300	dot
	Horizontal front porch	HFP		4	10	—	dot
	Horizontal Sync Pulse width	HS		8	10	—	dot
	Horizontal Back porch	HBP		18	20	—	dot
	Horizontal Data start	HDS	HS+HBP	26	30	—	dot
	Horizontal active area	HDISP		240	240	240	dot
	Clock frequency	tclk		4.5	5.44	7.0	MHz
		fclk			184		nS

Input timing chart

＜Vertical Timing chart＞

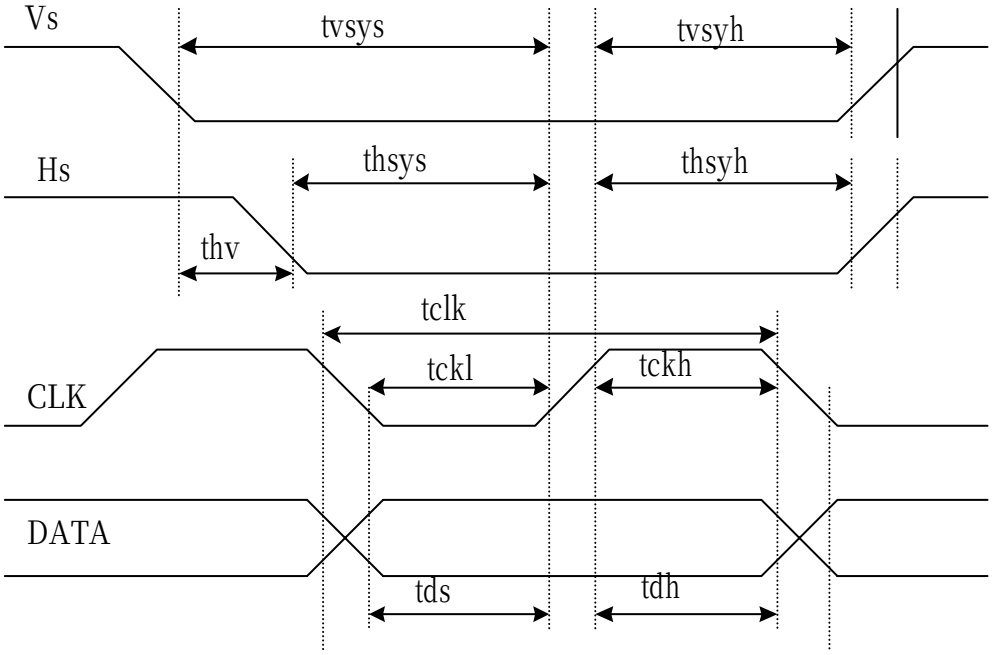


＜Horizontal Timing chart＞



*1 The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

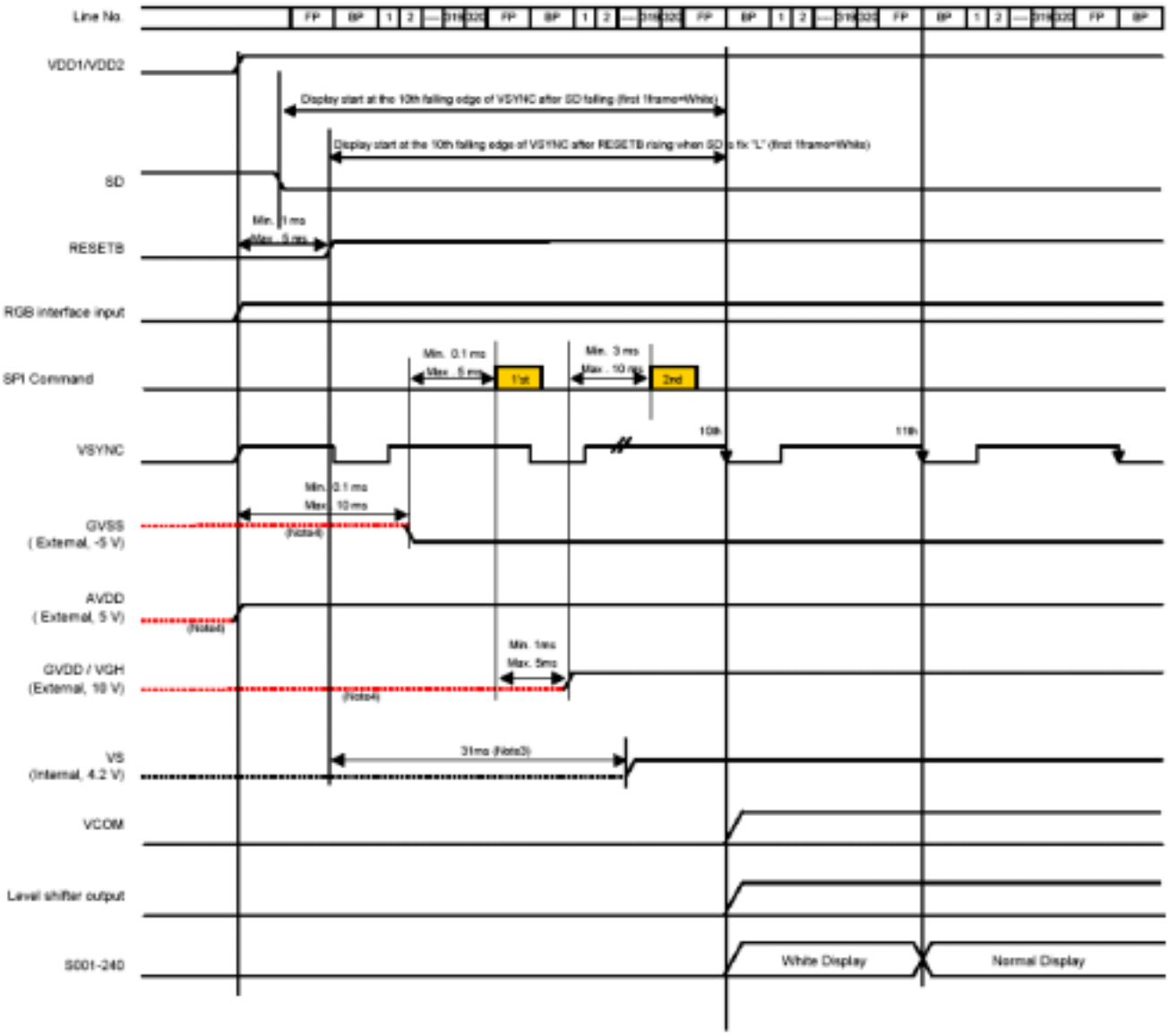
Setup/ Hold Timing chart



Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	—	—	ns
Vertical Sync. Hold time	tvsyh		20	—	—	ns
Horizontal Sync. Setup time	thsys		20	—	—	ns
Horizontal Sync. Hold time	thsyh		20	—	—	ns
Phase difference of Sync. Signal Falling edge	thv	240x320	0	—	239	clk
		176x220	0	—	175	
		128 x160	0	—	127	
		240 x 240	0	—	239	
Clock “L” Period	tckl		30	50	70	%
Clock “H” Period	tckh		30	50	70	%
Data setup time	tds		20	—	—	ns
Data Hold time	tdh		20	—	—	ns
Digital logic input	Trise/Tfall				15	ns

8. Power On/Off Sequence

8.1 Power On Sequence(with DC/DC supply outward & SD fixed at low)



(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBV/CSV)

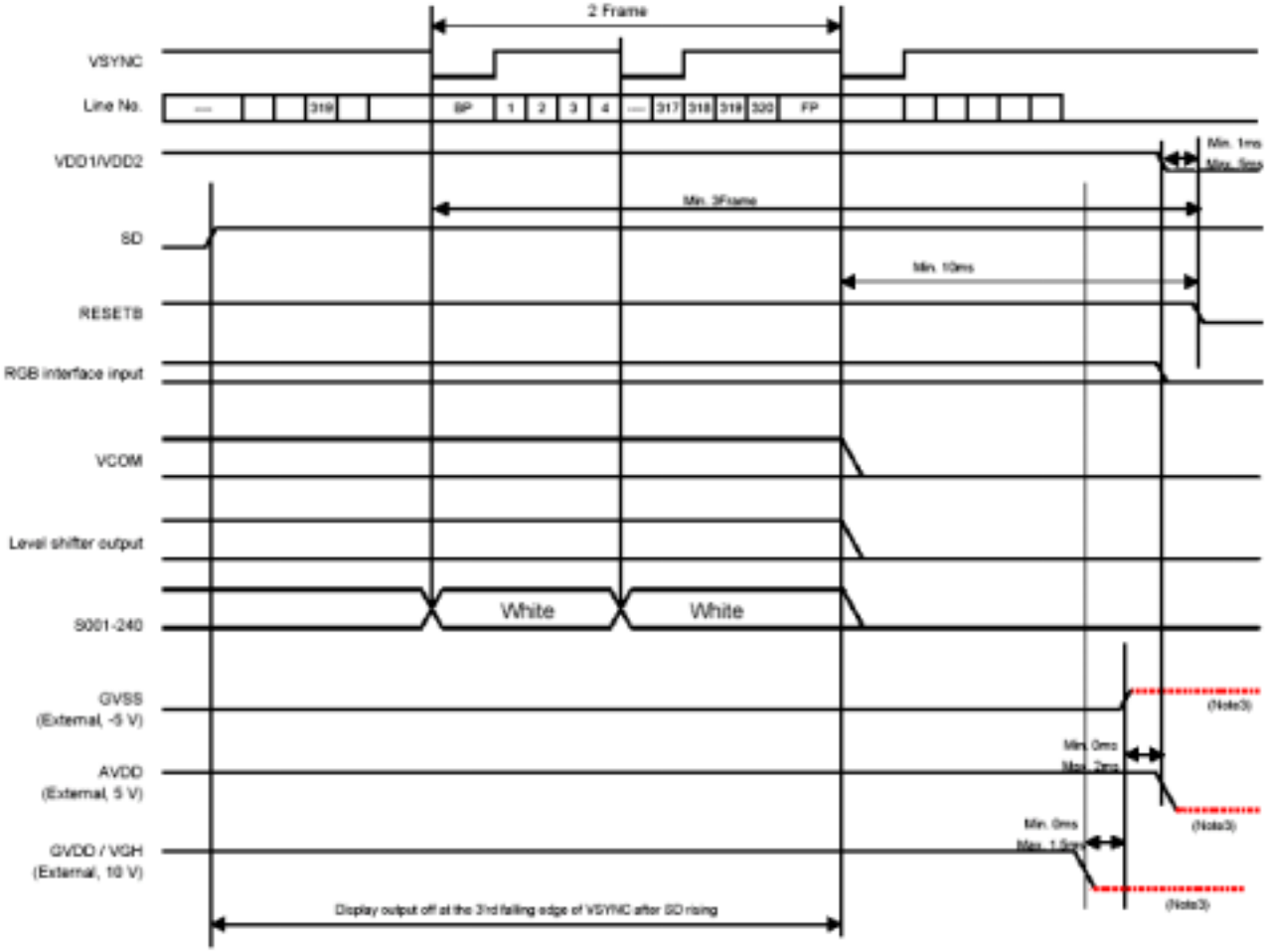
(Note3) Marked time is typical value (Typical values depend on the frequency of VSYNC)

(Note4) GVSS, AVDD and GVDD/VGH should be open before external power on

(Note5) In order to prevent high current due to the latch-up in external power on sequence, shot-key diode should be connected between VGH and VDD2 as shown ***External Component Application2*** *in page5. (Recommended spec of the shot-key diode: VF < 0.4V/100mA, VR > 15V)*

Note: In some application, SD signal fixed at “low” level during power on. ASIC should produce white pattern when receiving10th S. And internal power regulator should function normally.

8.2 Power Off Sequence(with DC/DC supply outward & SD fixed at low)



(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBW/CSV)

(Note3) GVSS, AVDD and GVDD/VGH should be open after external power off

(Note5) In order to prevent high current due to the latch-up in external power on sequence, shot-key diode should be connected between VGH and VDD2 as shown ***External Component Application2*** *in page5. (Recommended spec of the shot-key diode: VF < 0.4V/100mA, VR > 15V)*

Note: When SD fixed at low during power off, user should provide white pattern before power off.

Note: The reset signal should be pulled to the level below VIL to ensure the ASIC will reset normally while power on.

9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off / w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	70	85	-	Degree	Note 9-1
	Θ21+Θ22			75	95	-		
Chromaticity	White	x	Θ=0°	0.25	0.30	0.35	-	Note 9-3
		y		0.28	0.33	0.38	-	
Contrast Ratio	CR		Θ=0°	10:1	15:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	7	10	-	%	Note 9-4

(2) Back Light On /w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	100	120	-	Degree	Note 9-1
	Θ21+Θ22			90	110	-		
Response Time	Tr+Tf		Θ=0°	-	35	40	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	80:1	100:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F=20mA	65	80	-	cd/m^2	Note 9-7
NTSC	-		-	32	36	-	%	Note 9-7
Uniformity	-		-	70	80	-	%	Note 9-8
Chromaticity	White	x	Θ=0°	0.275	0.31	0.345	-	Note 9-3
		y		0.29	0.33	0.37		

9.2 Basic measure condition

(1) Driving voltage

VDD= 12.0V, VEE=-6.5V

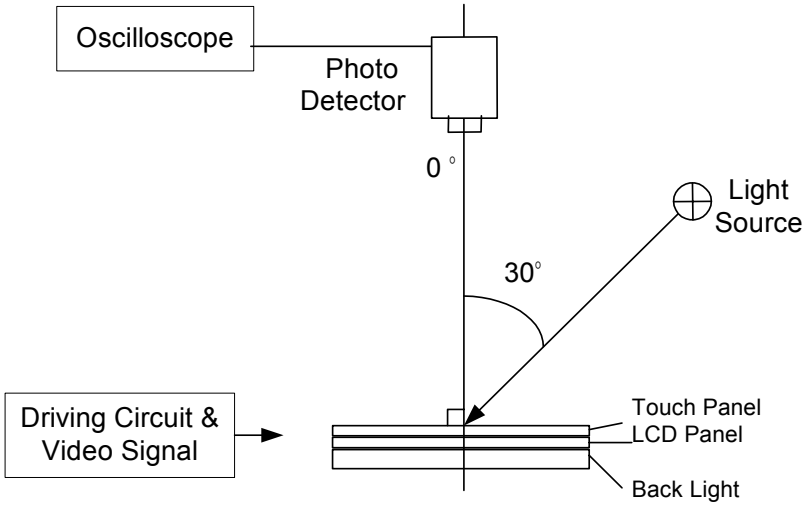
(2) Ambient temperature: Ta=25℃

(3) Testing point: measure in the display center point and the test angle Θ=0°

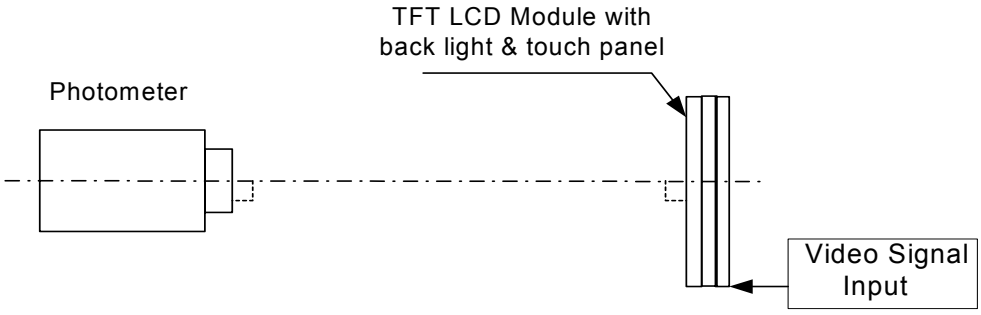
(4) Testing Facility

Environmental illumination: ≤ 10 Lux

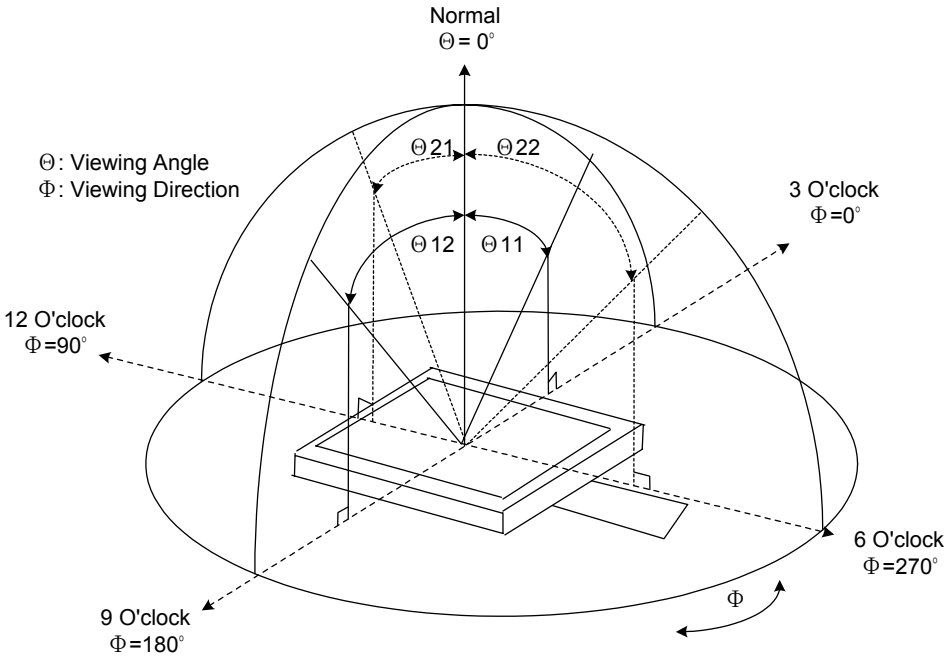
a. System A



b. System B



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

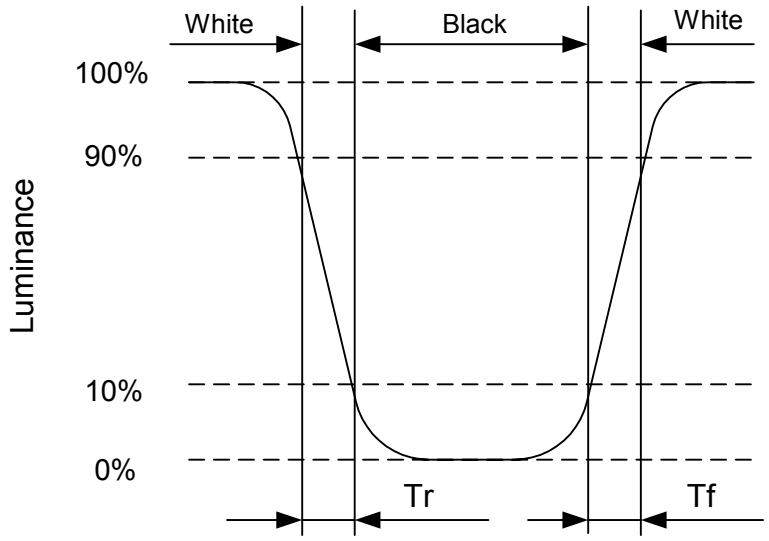
Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system B. calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \times \text{Reflectance factor of reflectance standard}$$

Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

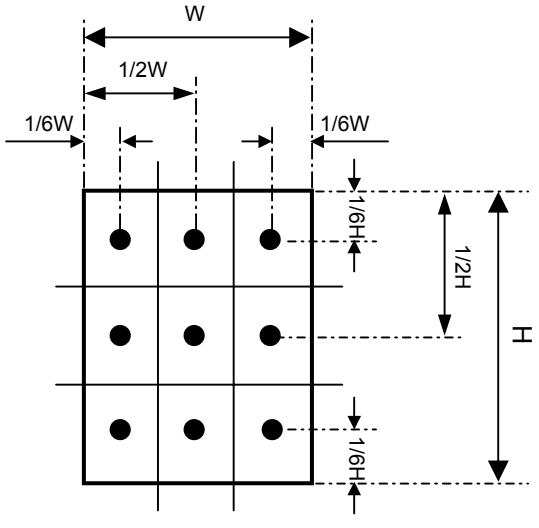
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20℃, 240hrs
6	Thermal Shock (non-operation)	-20℃ ← → 70℃, 50 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0 Ω; Discharge: ±150V 3 times / Terminal
8	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
9	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
10	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times
11	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R8 HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
12	Writing Friction Resistance Test (Touch Panel)	Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35m 100000 times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized air flowing decrease the charge in the environment is necessary.

(4) In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

(1) Working environment should be clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionizer to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a lens cleaner for glasses or something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface when panel is powered on will corrode panel electrode.

(4) Before opening up the packing bag, watch out the environment for the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

11.5 Design notes on touch panel

(1) Explanation of each boundary of touch panel

Ａ.Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

Ｂ.Viewing area

a. Cosmetic inspection to be done for this area.
This area is set as inside of boundary of double-sided adhesive with tolerance.

C.Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

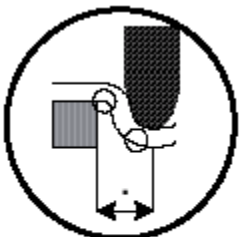
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

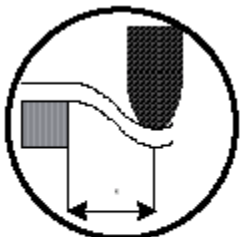
D.Active area

a. This area is where the performance is guaranteed.
This area set as some distance inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.

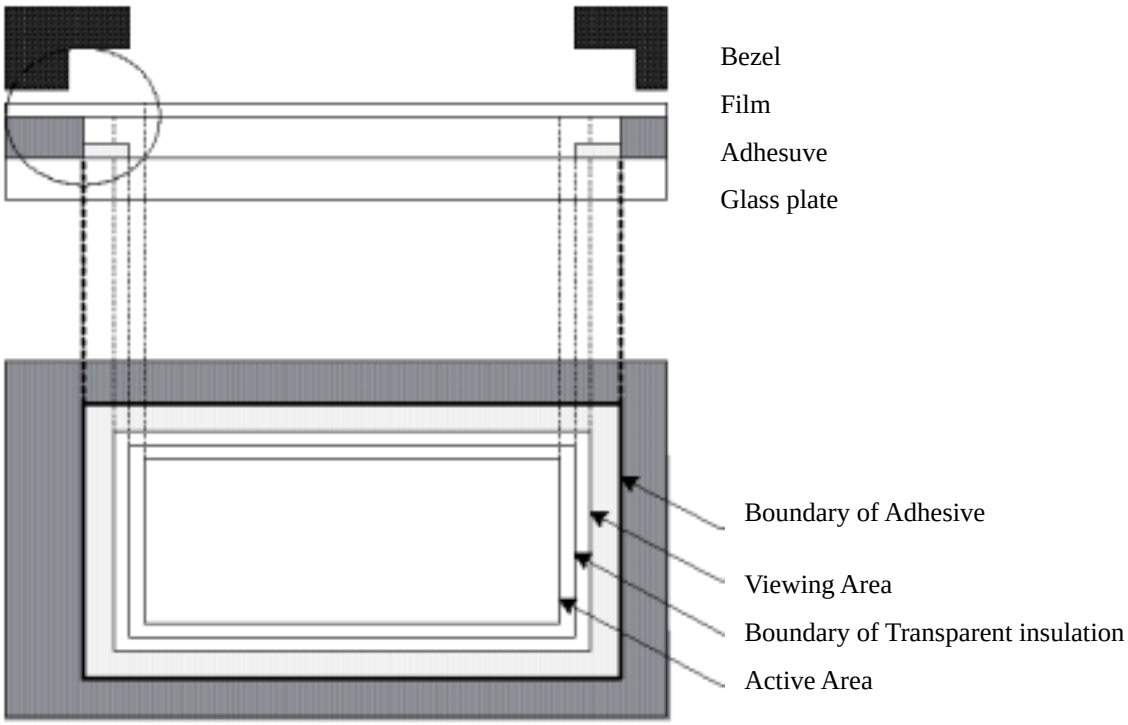
b. Please refer to the attached module drawing for the bezel opening and window size design.



There is some possibility to damage ITO



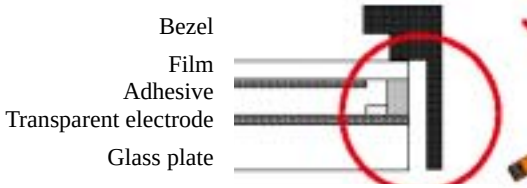
No Damage to ITO



(2) Housing and touch panel

a. Please have clearance between the side of touch panel, and any conductive material such as metal frame.(drawing.1) Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause malfunction.



Drawing 1

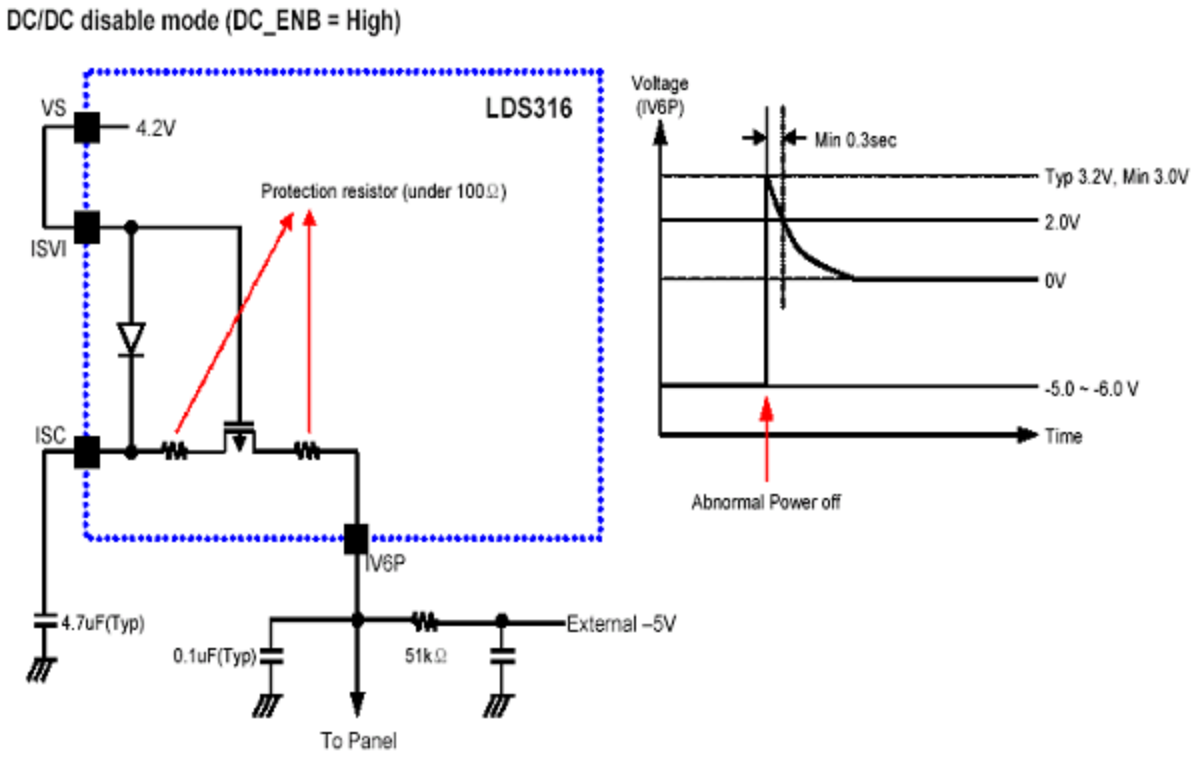
Drawing 2

11.6 Note for image discharge circuit

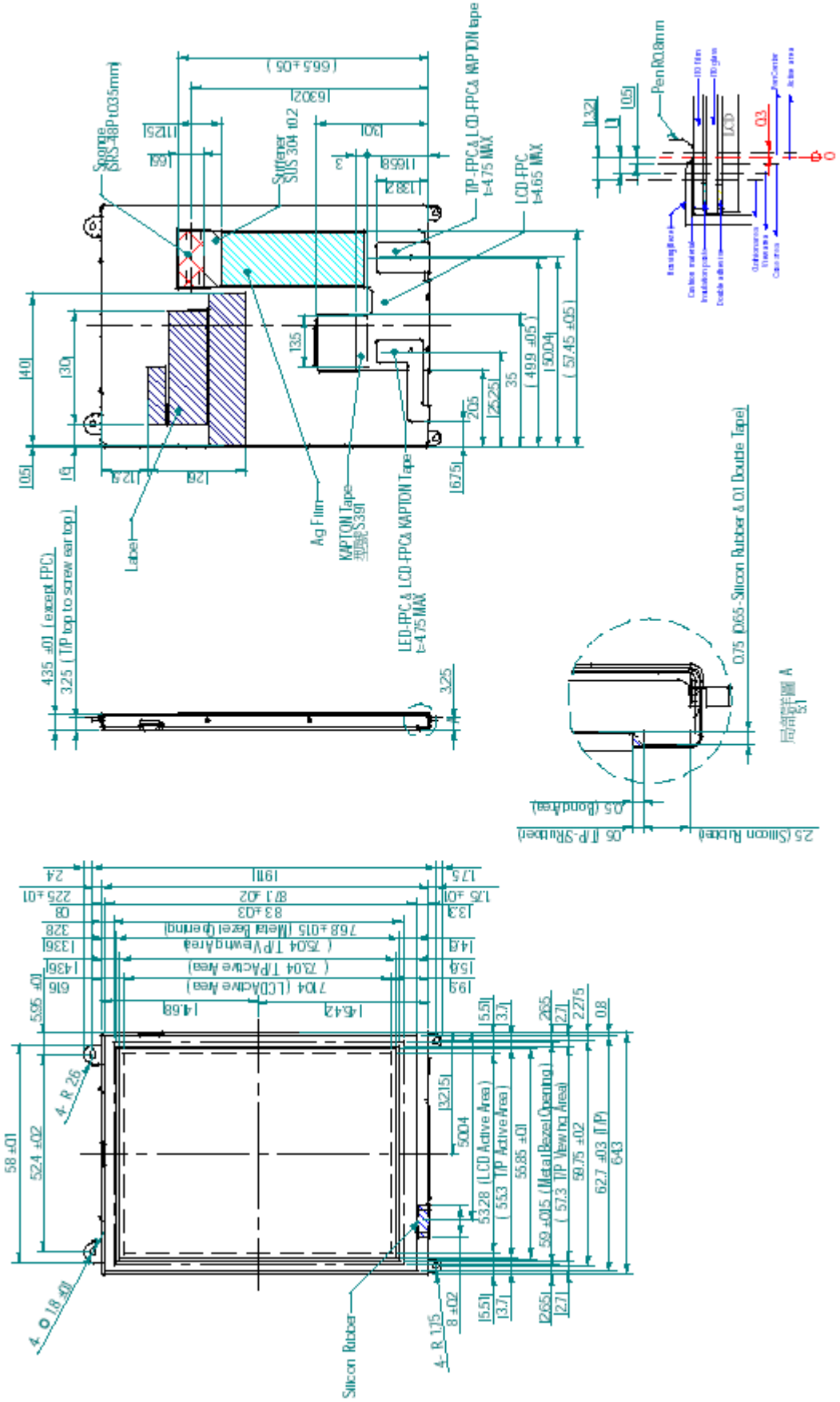
(1) The image will remain on display when the power is suddenly cut off in abnormal condition, ie, unit dropped and battery fell out. The phenomenon is because the electrical charge well be held in pixel, if there is no extra input signal to release it, the residual image occurs.

(2) The imaging discharge circuit is used for clearing the image residual on display. The circuit is designed on panel IC and customer can input signal to driver the function especially in the case that the battery or power supplier unit are removable.

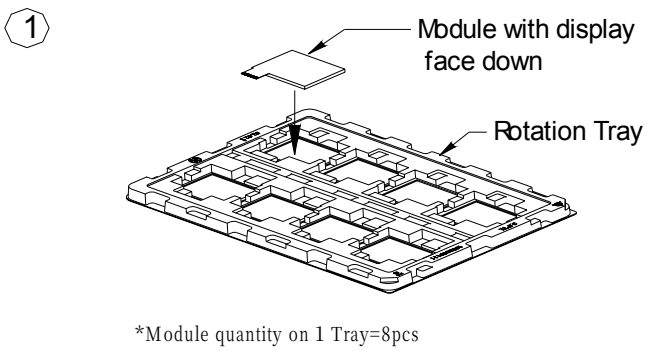
(3) The circuit below is designed on panel IC to avoid image sticking .



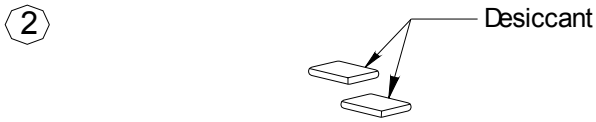
12. Mechanical Drawing

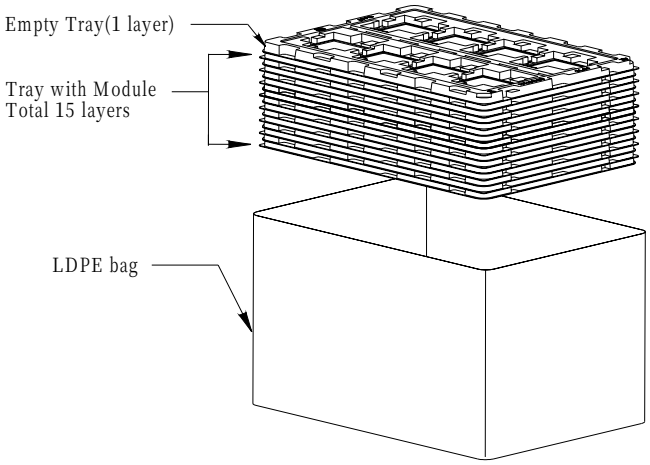


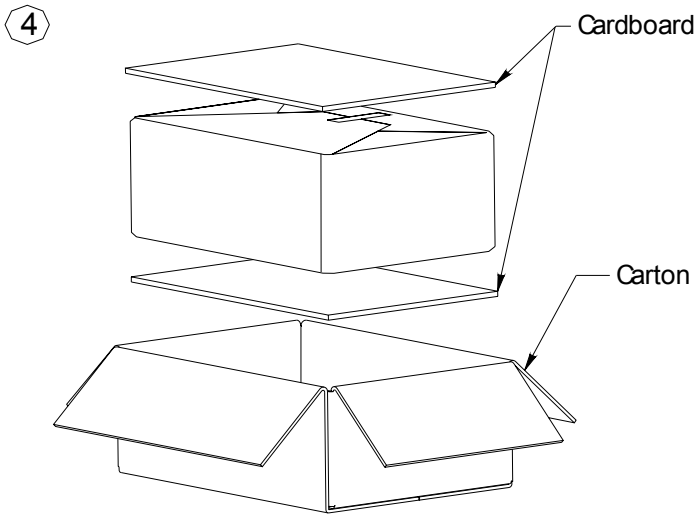
13. Packing Drawing

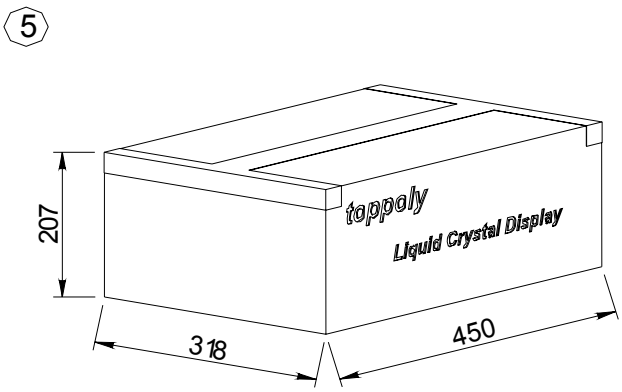


*Module quantity on 1 Tray=8pcs

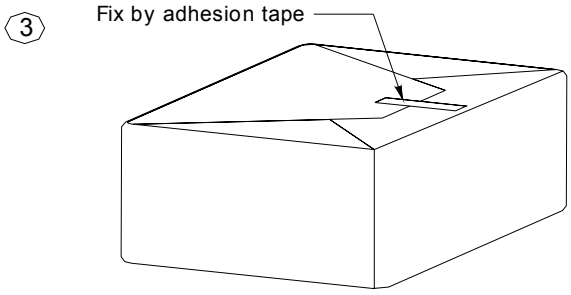








Module quantity in 1 carton=120pcs



TD035STED1 module delivery packing method

(1). Module packed into tray cavity with display face down.

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2 pcs desiccant put above the empty tray.

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4) Put 1pc cardboard inside the carton bottom, then pack the finished package into the carton.

(5). Carton sealing with adhesive tape.