TFT LCD Specification

Model NO.: TD035STED6

TENTATIVE

Customer Signature
Date

Table of Contents

Record of Reversion

Rev	Issued Date	Description
0.00	Mar, 11,2005	New

1. FEATURES

The 3.5" LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it's COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (6 bits)	-
Outline Dimension (HxVxT)		64.3 X 87.1X2.95*	Mm
Weight		TBD	G
Power consumption	LCD Panel + T-CON + L/S	25 (Typ)	MW
	Backlight	288 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

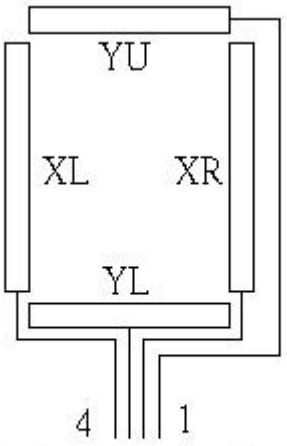
Pin	Symbol	I/O	Description	Remark
1	DE	I	Data Enable Signal	DE
2	MCLK	I	LCM Pixel Clock	MCLK
3	ENABLE	I	IC Reset Signal	ENABLE
4	TSP1	O	TSP Interface Signal YU	TSP1
5	DVSS	I	Digital Ground	DVSS
6	VCOM_I	I	VCOM Input	VCOM_I
7	VCOM_I	I	VCOM Input	VCOM_I
8	AVSS	I	Analog Ground	AVSS
9	VVEE	I	Gate Off Voltage, -5.2V ~ -5.8V, Typ. -5.5V	VVEE
10	VVEE	I	Gate Off Voltage, -5.2V ~ -5.8V, Typ. -5.5V	VVEE
11	VGH	I	Gate On Voltage, 9.5V ~ 10.5V, Typ. 10V	VGH
12	VGH	I	Gate On Voltage, 9.5V ~ 10.5V, Typ. 10V	VGH
13	DVSS	I	Digital Ground	DVSS
14	TSP2	O	TSP Interface Signal XL	TSP2
15	VCOM_H	O	Positive Power Output for VCOM	VCOM_H
16	VCOM_O	O	VCOM Output	VCOM_O
17	VCOM_O	O	VCOM Output	VCOM_O
18	VCOM_L	O	Negative Power Output for VCOM	VCOM_L
19	AVSS	I	Analog Ground	AVSS
20	DVDD	I	Digital Supply Power, 2.7V ~ 3.0V, Typ. 2.85V	DVDD
21	DVDD	I	Digital Supply Power, 2.7V ~ 3.0V, Typ. 2.85V	DVDD
22	AVDD	I	Analog Supply Power, 4.8V ~ 5.6V, Typ. 5.0V	AVDD
23	AVDD	I	Analog Supply Power, 4.8V ~ 5.6V, Typ. 5.0V	AVDD
24	TSP3	O	TSP Interface Signal YL	TSP3
25	DVSS	I	Digital Ground	DVSS

26	IV6P	O	Negative Voltage Output Pad	IV6P
27	TSP4	O	TSP Interface Signal XR	TSP4
28	DVDD (TB_RL)	I	Digital Supply Power, 2.7V ~ 3.0V, Tpy. 2.85V (TB_RL)	DVDD Shift direction (Right/Left) H: D1→D240 L: D240→D1 Shift direction (Top/Bottom) H: Top→Bottom L: Bottom→Top
29	PD17	I	R5 (Red MSB)	PD17
30	PD16	I	R4	PD16
31	PD15	I	R3	PD15
32	PD14	I	R2	PD14
33	PD13	I	R1	PD13
34	PD12	I	R0 (Red LSB)	PD12
35	PD11	I	G5 (Green MSB)	PD11
36	PD10	I	G4	PD10
37	PD9	I	G3	PD9
38	PD8	I	G2	PD8
39	PD7	I	G1	PD7
40	PD6	I	G0 (Green LSB)	PD6
41	PD5	I	B5 (Blue MSB)	PD5
42	PD4	I	B4	PD4
43	PD3	I	B3	PD3
44	PD2	I	B2	PD2
45	PD1	I	B1	PD1
46	PD0	I	B0 (Blue LSB)	PD0
47	ISC	O	Capacitor Connection Pad	ISC
48	DVSS(SCL)	I	Digital Ground(Serial interface clock input)	DVSS(SCL)
49	DVSS(SDA)	I	Digital Ground(Serial interface data input/output)	DVSS(SDA)
50	DVSS(CS)	I	Digital Ground(Serial interface chip select input)	DVSS(CS)
51	DVSS	I	Digital Ground	DVSS
52	HSYNC	I	Horizontal SYNC Input	HSYNC
53	DVSS	I	Digital Ground	DVSS
54	DVSS(CM)	I	Digital Ground(Display mode	DVSS(CM)

			select)	
55	VS	O	Positive Power Output for Source Driver	VS
56	VSYNC	I	Vertical SYNC Input	VSYNC
57	MAIN_LED+	I	LED Power (Anode)	MAIN_LED+
58	MAIN_LED+	I	LED Power (Anode)	MAIN_LED+
59	MAIN_LED-	O	LED Power (Cathode)	MAIN_LED-
60	MAIN_LED-	O	LED Power (Cathode)	MAIN_LED-
61	DVSS	I	Digital Ground	DVSS

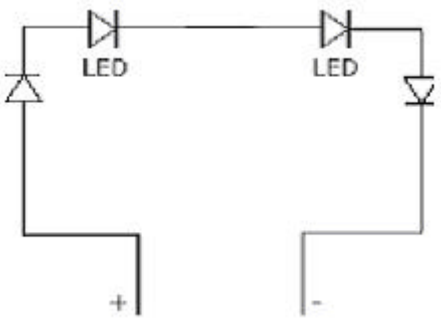
3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	1	YU	Touch Panel Right Side	
2	2	XR	Touch Panel Lower Side	
3	3	YL	Touch Panel Left Side	
4	4	XL	Touch Panel Upper Side	



Pin Assignment for Touch panel

3.3 Back light pin assignment



(57,58) (59,60)

4. ABSOLUTE MAXIMUM RATINGS

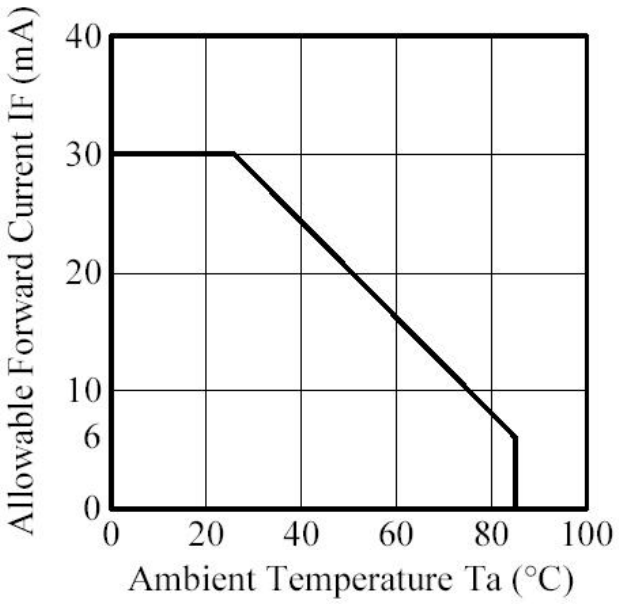
GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD1, VDD2	-0.3	+3.6	V	
	AVDD	-0.3	6	V	
Power Supply for H/V Driver	VGH	-0.3	+19	V	
	VVEE	-5.8	-5.2	V	Note 1
Touch Panel Operation Voltage	V_{Touch}	-	5.5	V	
Backlight LED forward Voltage	V_F	-	4	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	30	mA	Note2
Operating Temperature	Topr	-20	+70	℃	
Storage Temperature	Tstg	-30	+80	℃	

Note1. The operating voltage is between +0.5V and –5.0V at the moment when the power is turned on

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs. Allowable Forward Current



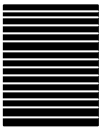
5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

T a=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		VDD1	2.4	2.8	3.3	V	
		VDD2	2.4	2.8	3.3	V	
		AVDD	4.8	5	5.6	V	
Power Supply for H/V Driver		VGH	9.5	10	10.5	V	
		VVEE	-5.8	-5.5	-5.2	V	
Data Input Voltage	High	VIH	0.7VDD1	—	VDD1	V	R[5:0], G[5:0], B[5:0], CLK DE
	Low	VIL	0	—	0.2VDD1		
VDD1,VDD2 Supply Current		I_{VDD1}	-	0.7/0.04	1.7/0.2	mA	Note 1,2
AVDD Supply Current		I_{AVDD}	-	1.65	4.0	mA	Note 3
VGH Supply Current		I_{VDD}	-	0.07	0.2	mA	
VVEE Supply Current		I_{VEE}	-	0.05	0.5	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



Note 2: VDD2 rush current accept 120mA, 500u sec during system booting.

Note 3: Gamma correction voltage is set to achieve the optimum at VCC5=5.0V. Use the voltage at level as close to 5.0V as possible.

5.2 DC/DC Spec

Item	Input voltage			Input Current	Input ripple(Max)	
	MIN	TYP	MAX			
VDD2	2.4V	2.8V	3.3V	0.04	--	
AVDD	4.8V	5V	5.6V	1.65	50 mV	Note 1
VGH	9.5V	10V	10.5V	0.07	150mV	
VVEE	-5.8 V	-5.5 V	-5.2 V	0.05	--	

Note 1: VCC5 is analog voltage supply therefore use as less ripple as possible.

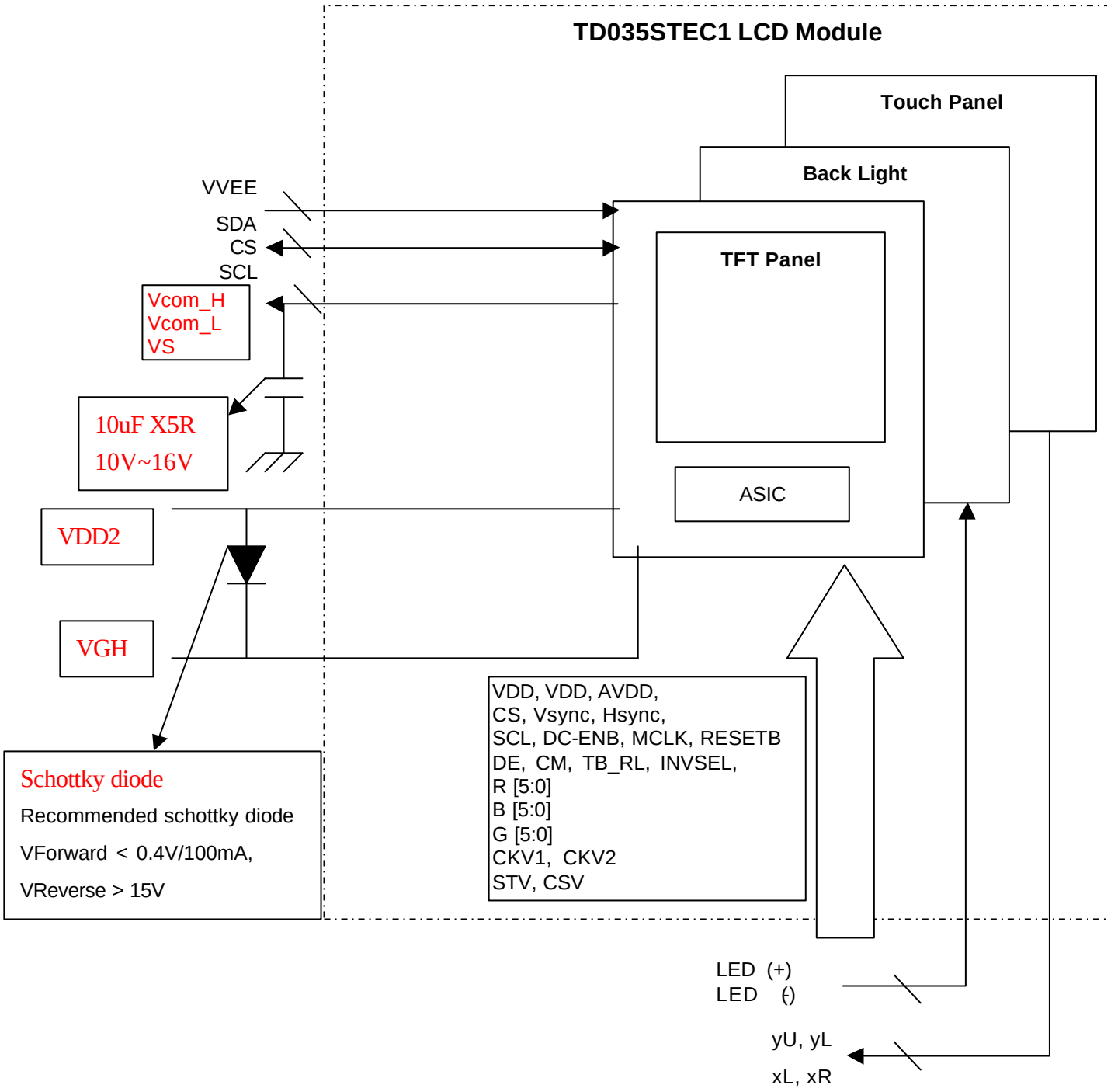
5.3 Driving backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	30	mA	LED/Part
LED Life Time	-	-	10,000	-	Hr	I_F: 15mA
Forward Current Voltage	V_F	-	3.6	4.0	V	I_F: 20mA ,LED/Part

Note : Backlight driving circuit is recommend as the fix current circuit.

6. BLOCK DIAGRAM



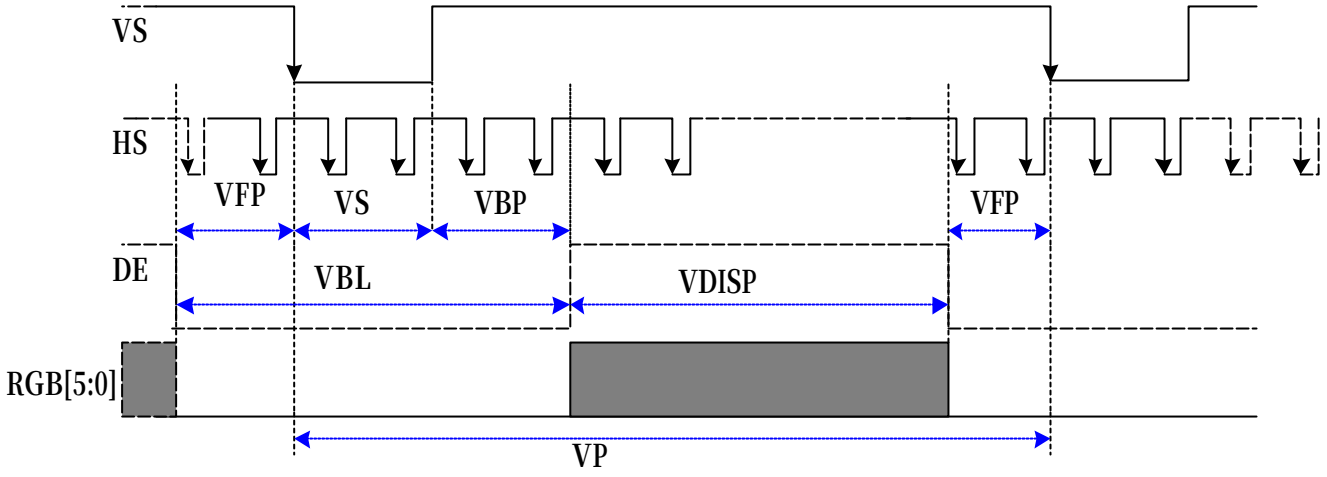
7. TIMING CHART

7.1 Display timing

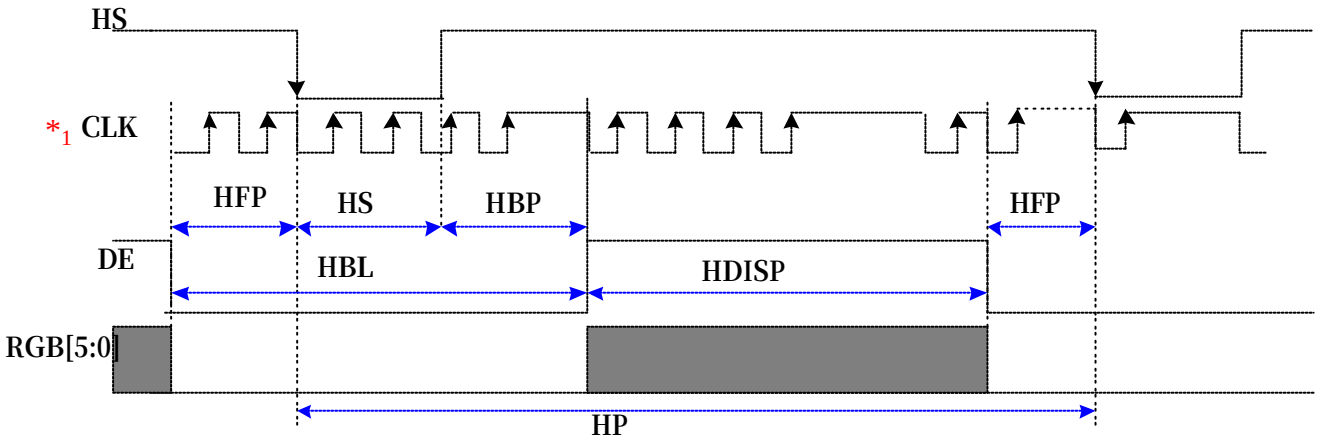
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		323	326	340	Line
	Vertical data start	VDS	VS+VBP	2	4	—	Line
	Vertical front porch	VFP		1	2	—	Line
	Vertical blanking period	VBL	VS+VBP+VFP	3	6	—	Line
	Vertical active area	VDISP		—	320	—	Line
	Horizontal cycle	HP		260	280	300	dot
	Horizontal front porch	HFP		4	10	—	dot
	Horizontal Sync Pulse width	HS		8	10	—	dot
	Horizontal Back porch	HBP		18	20	—	dot
	Horizontal Data start	HDS	HS+HBP	26	30	—	dot
	Horizontal active area	HDISP		240	240	240	dot
	Clock frequency	tclk		4.5	5.44	7.0	MHz
		fclk			184		nS

Input timing chart

＜Vertical Timing chart＞

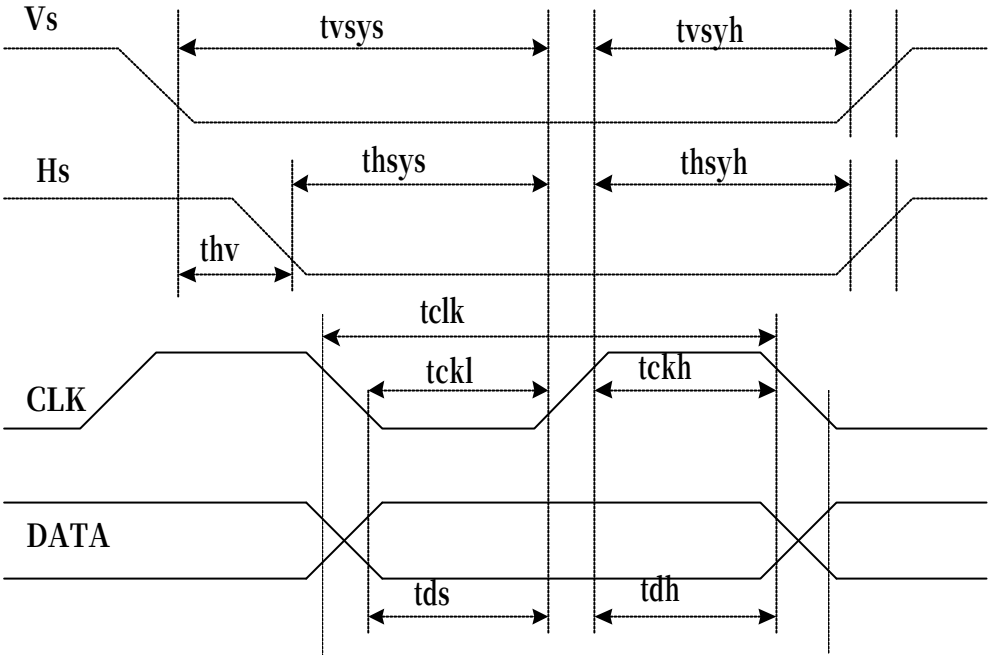


＜Horizontal Timing chart＞



*1 The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

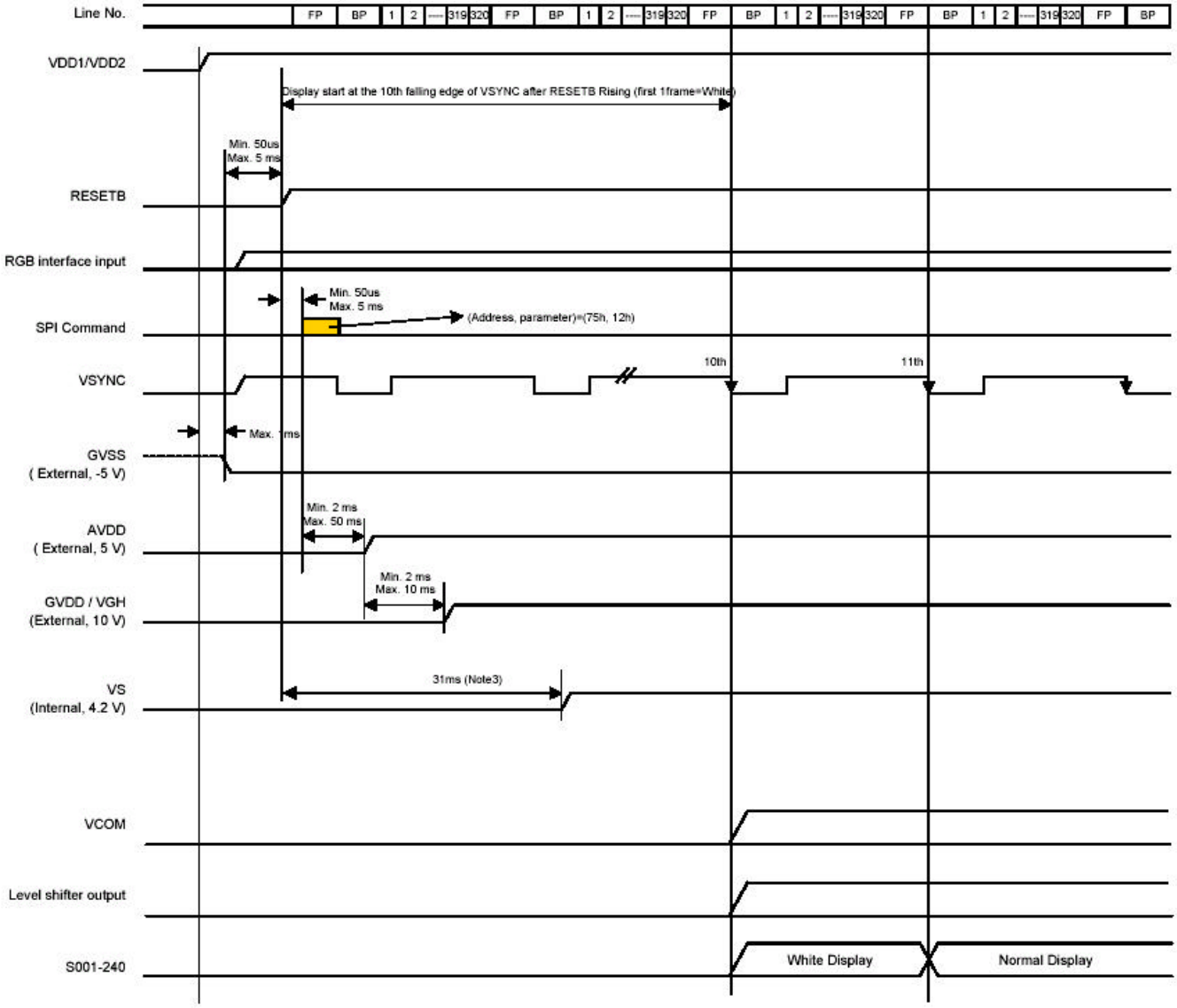
Setup/ Hold Timing chart



Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	—	—	ns
Vertical Sync. Hold time	tvsyh		20	—	—	ns
Horizontal Sync. Setup time	thsys		20	—	—	ns
Horizontal Sync. Hold time	thsyh		20	—	—	ns
Phase difference of Sync. Signal Falling edge	thv	240x320	0	—	239	clk
		176x220	0	—	175	
		128 x160	0	—	127	
		240 x 240	0	—	239	
Clock “L” Period	tckl		30	50	70	%
Clock “H” Period	tckh		30	50	70	%
Data setup time	tds		20	—	—	ns
Data Hold time	tdh		20	—	—	ns
Digital logic input	Trise/Tfall				15	ns

8. Power On/Off Sequence

8.1 Power On Sequence(with DC/DC supply outward & SD fixed at low)



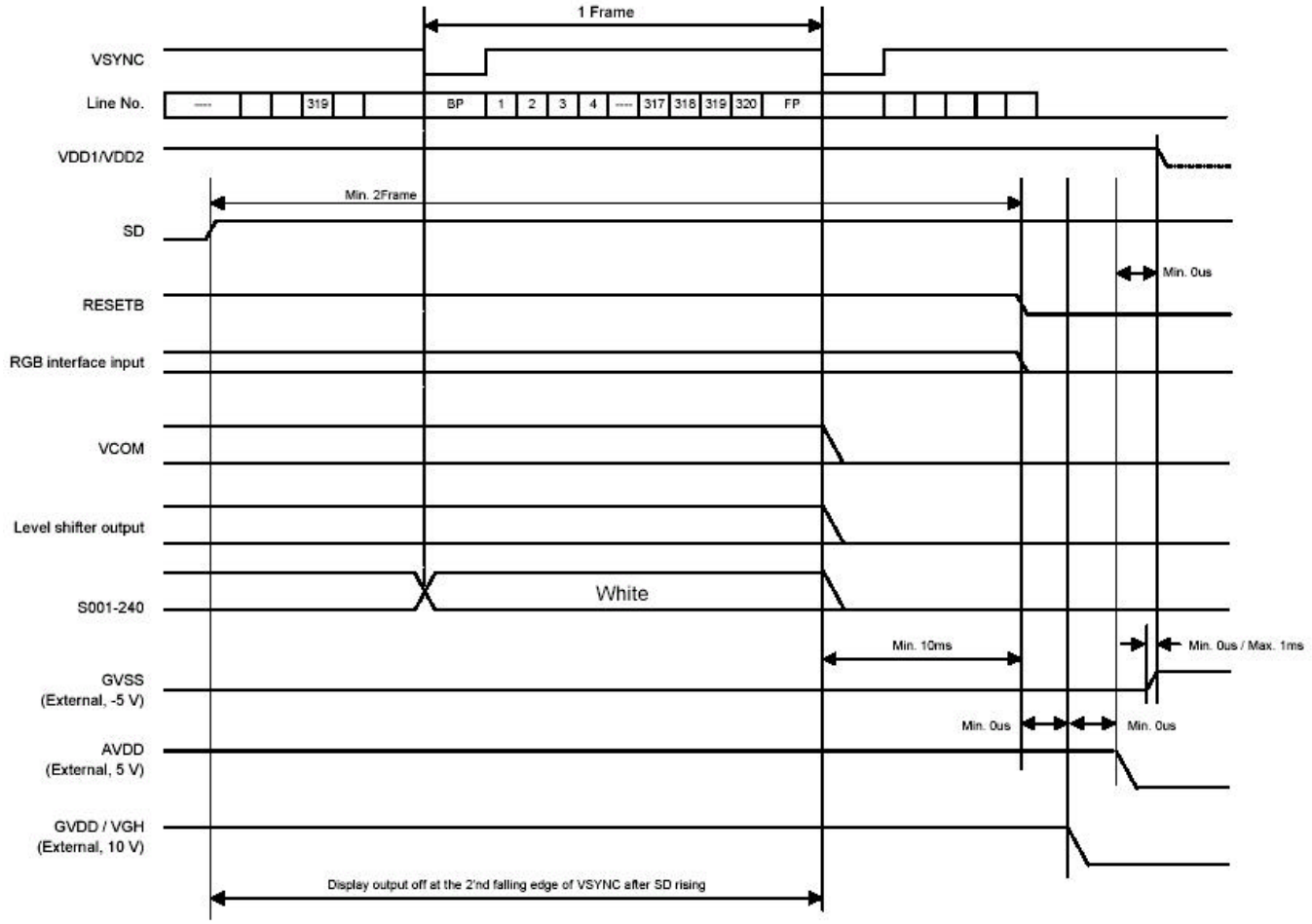
(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBV/CSV)

(Note3) Marked time is typical value (Typical values depend on the frequency of VSYNC)

Note: In some application, SD signal fixed at “low” level during power on. ASIC should produce white pattern when receiving10th S. And internal power regulator should function normally.

8.2 Power Off Sequence(with DC/DC supply outward & SD fixed at low)



(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBV/CSV)

Note: When SD fixed at low during power off, user should provide white pattern before power off.

Note: The reset signal should be pulled to the level below VIL to ensure the ASIC will reset normally while power on.

9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off / w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR = 2	70	85	-	Degree	Note 9-1
	Θ21+Θ22			75	95	-		
Chromaticity	White	x	Θ=0°	-	-	-	-	Note 9-3
		y		-	-	-	-	
Contrast Ratio	CR		Θ=0°	10:1	15:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	TBD	TBD	-	%	Note 9-4

(2) Back Light On /w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR = 2	100	120	-	Degree	Note 9-1
	Θ21+Θ22			90	110	-		
Response Time	Tr+Tf		Θ=0°	-	35	40	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	80:1	100:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F=20mA	-	135	-	cd/m^2	Note 9-7
NTSC	-		-	32	36	-	%	Note 9-7
Uniformity	-		-	70	80	-	%	Note 9-8
Chromaticity	White	x	Θ=0°	-	0.31	-	-	Note 9-3
		y		-	0.33	-		

9.2 Basic measure condition

(1) Driving voltage

VDD= 12.0V, VEE=-6.5V

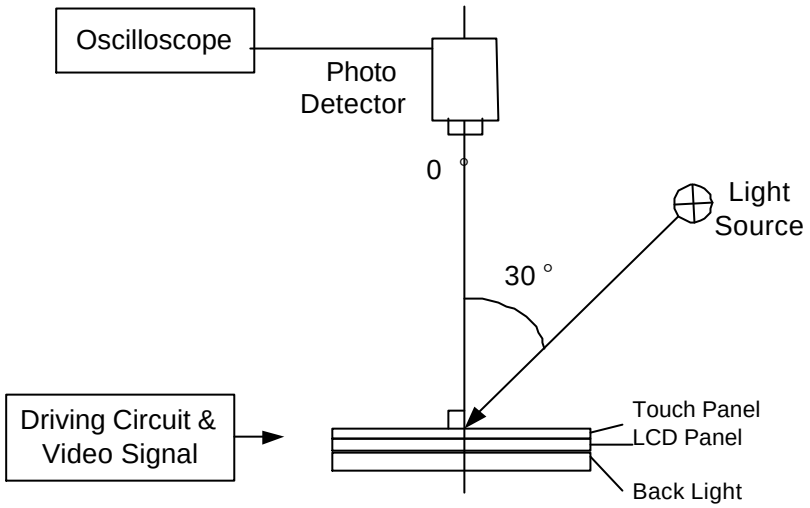
(2) Ambient temperature: Ta=25℃

(3) Testing point: measure in the display center point and the test angle Θ=0 °

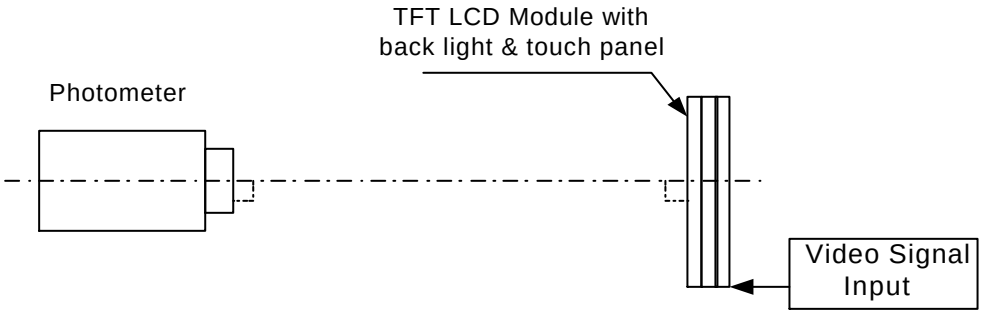
(4) Testing Facility

Environmental illumination: = 10 Lux

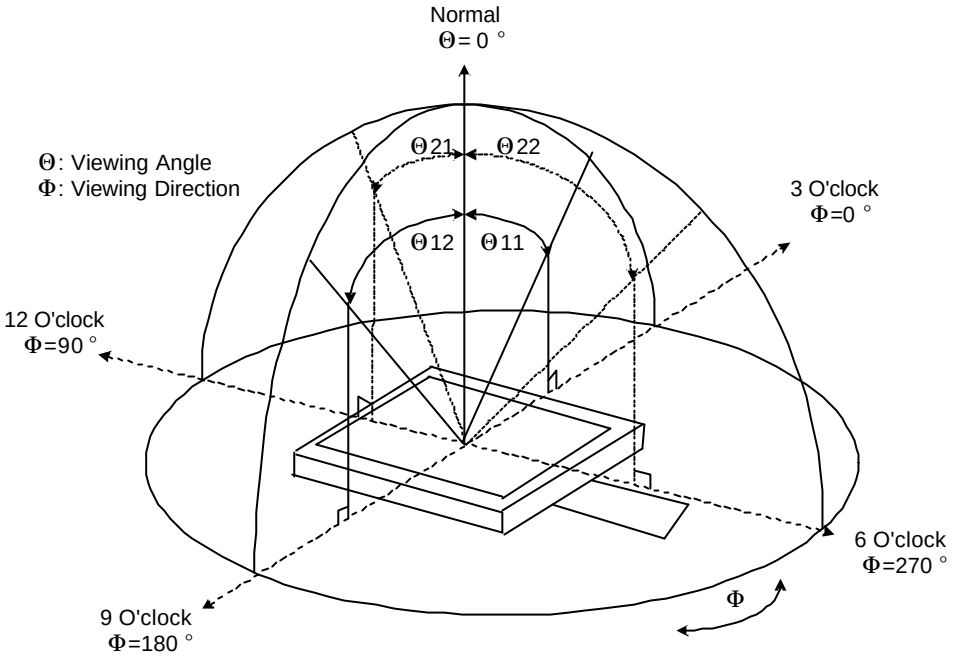
a. System A



b. System B



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

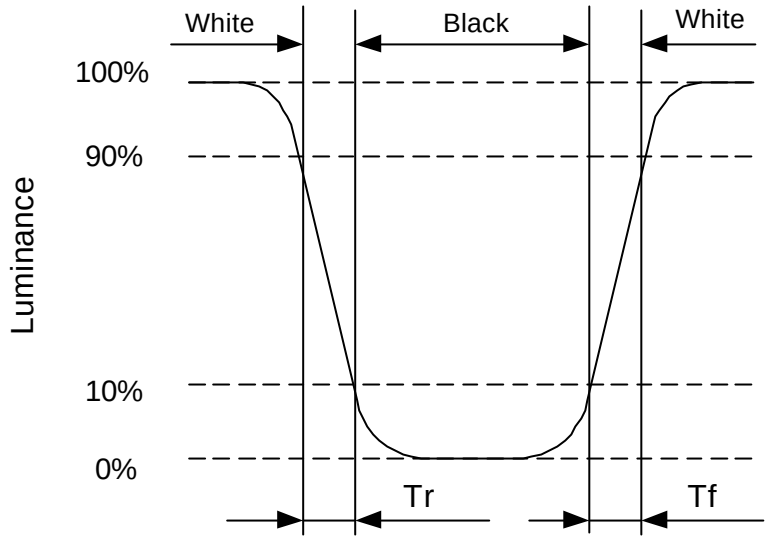
Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system B. calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \times \text{Reflectance factor of reflectance standard}$$

Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

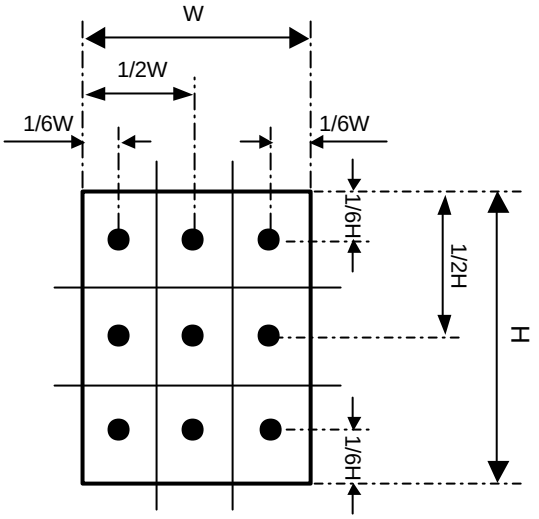
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60°C, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40°C, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10°C, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70°C, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20°C, 240hrs
6	Thermal Shock (non-operation)	-20°C ← → 70°C,30 cycles 30 min 30 min
7	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized air flowing decrease the charge in the environment is necessary.

(4) In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

(1) Working environment should be clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionizer to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a lens cleaner for glasses or something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface when panel is powered on will corrode panel electrode.

(4) Before opening up the packing bag, watch out the environment for the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

11.5 Design notes on touch panel

(1) Explanation of each boundary of touch panel

「१.Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

「२.Viewing area

a. Cosmetic inspection to be done for this area.
This area is set as inside of boundary of double-sided adhesive with tolerance.

「ㄴ.Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

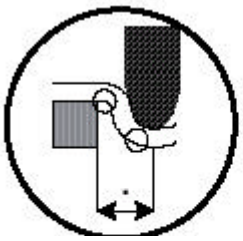
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

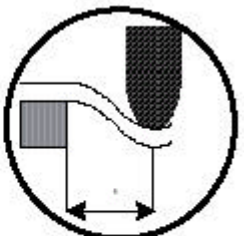
「ㄨ.Active area

a. This area is where the performance is guaranteed.
This area set as some distance inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.

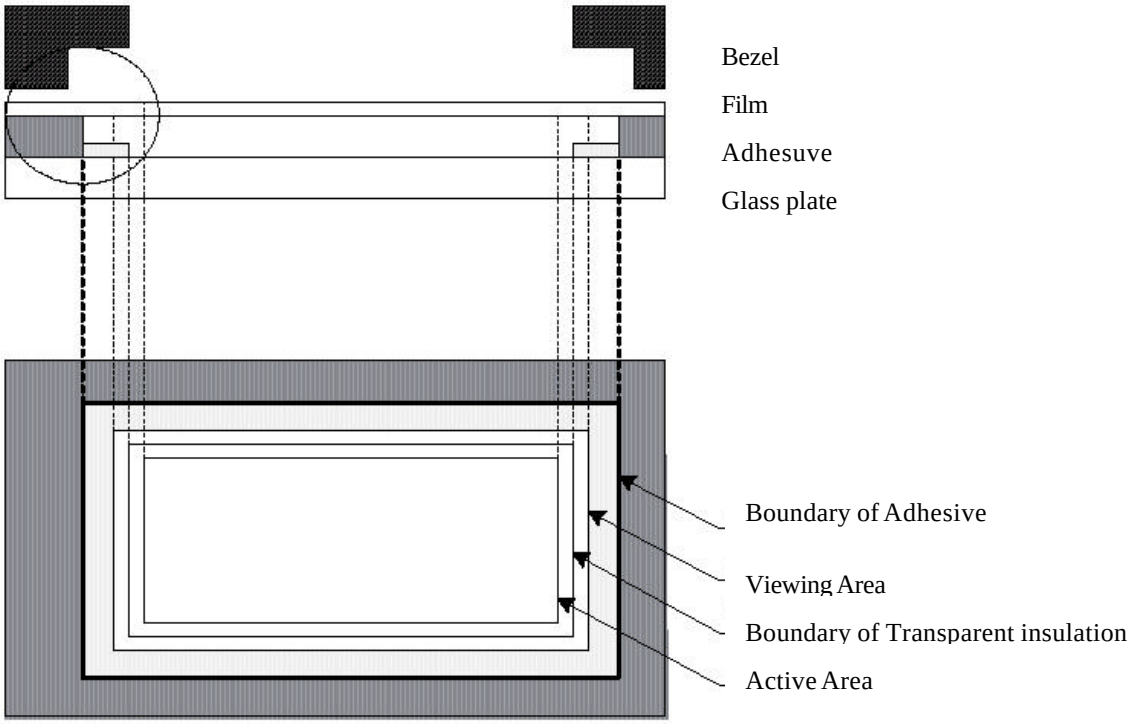
b. Please refer to the attached module drawing for the bezel opening and window size design.



There is some possibility to damage ITO



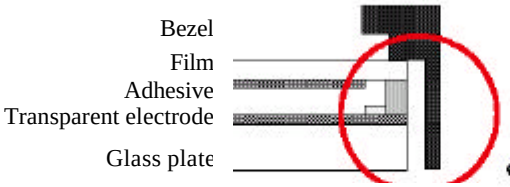
No Damage to ITO



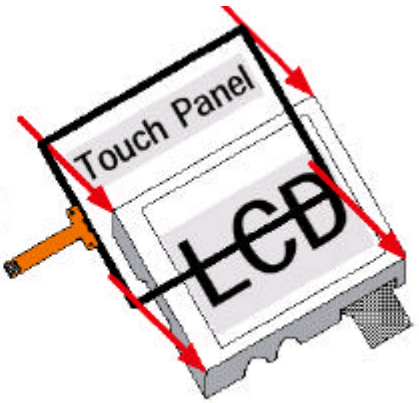
(2) Housing and touch panel

a. Please have clearance between the side of touch panel, and any conductive material such as metal frame.(drawing.1) Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause malfunction.



Drawing 1



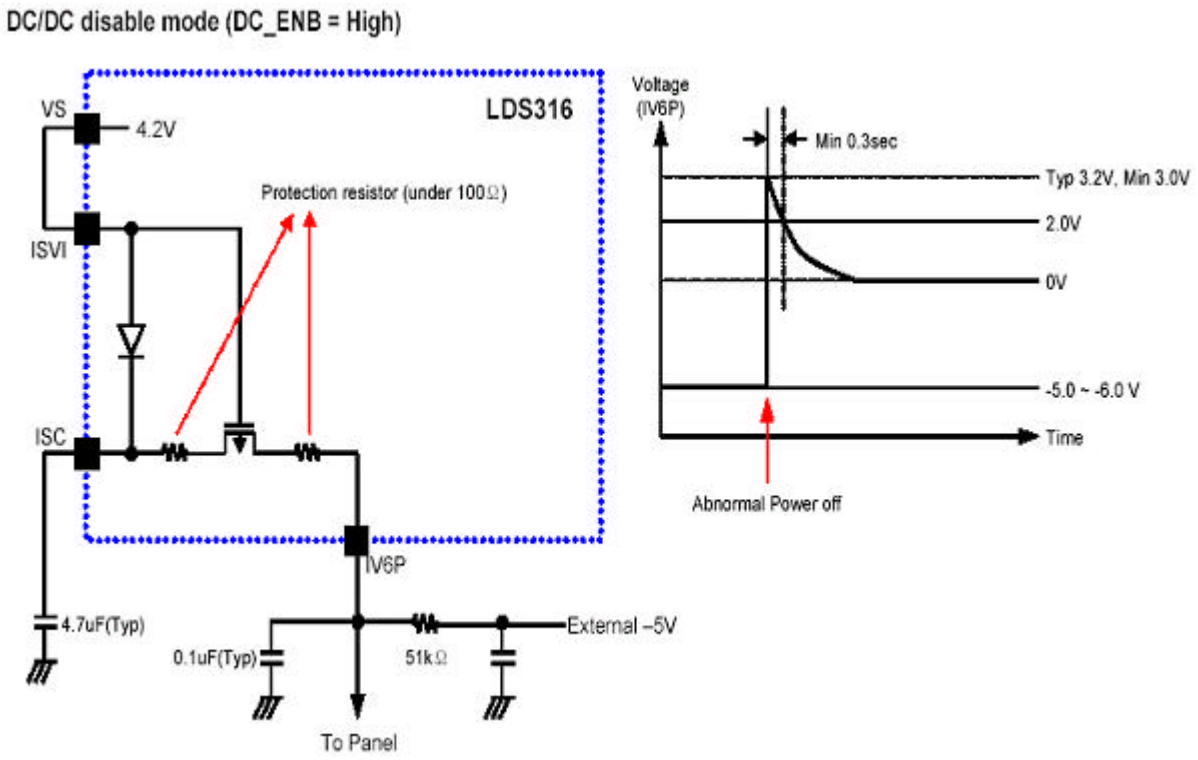
Drawing 2

11.6 Note for image discharge circuit

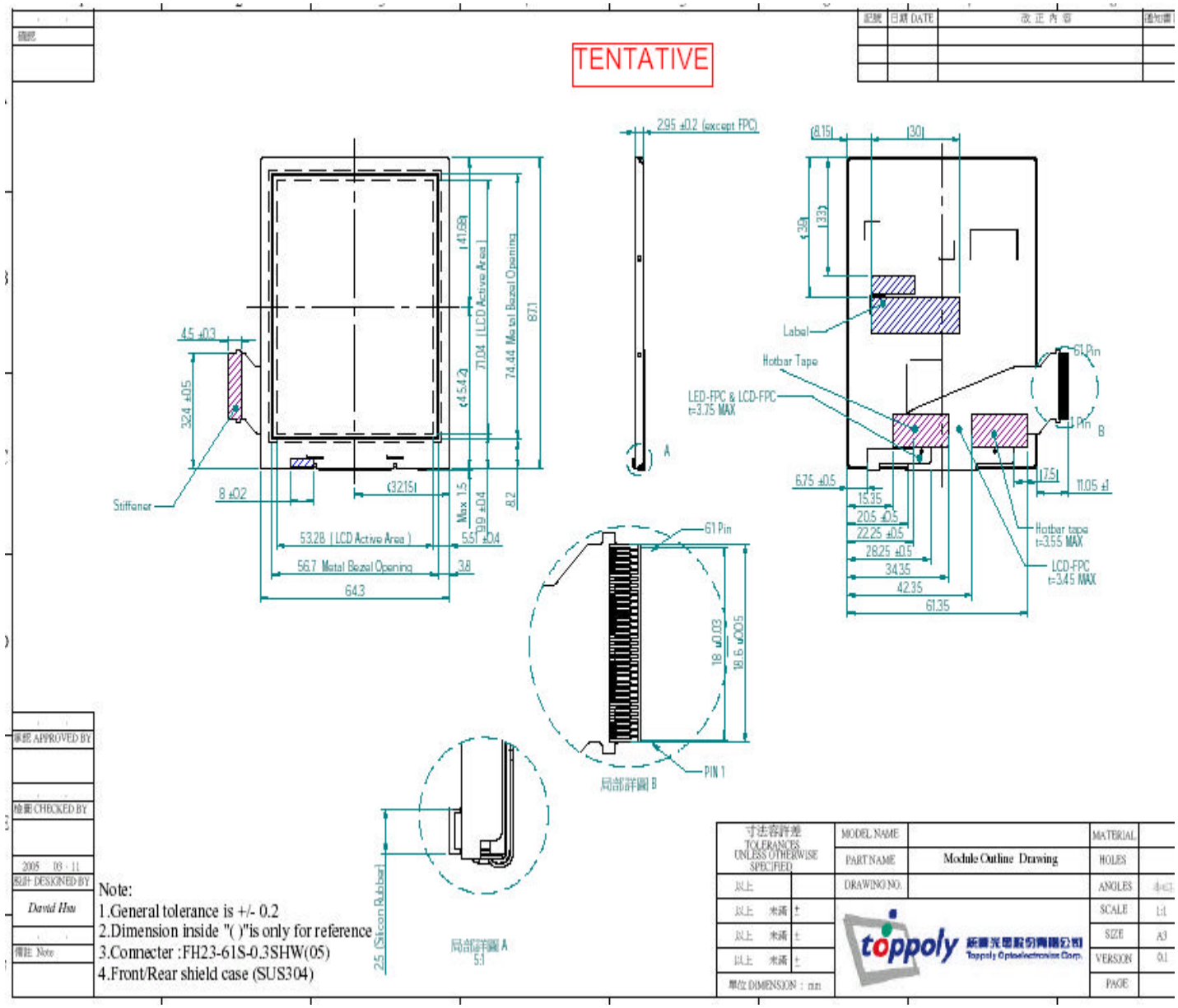
(1) The image will remain on display when the power is suddenly cut off in abnormal condition, ie, unit dropped and battery fell out. The phenomenon is because the electrical charge well be held in pixel, if there is no extra input signal to release it, the residual image occurs.

(2) The imaging discharge circuit is used for clearing the image residual on display. The circuit is designed on panel IC and customer can input signal to driver the function especially in the case that the battery or power supplier unit are removable.

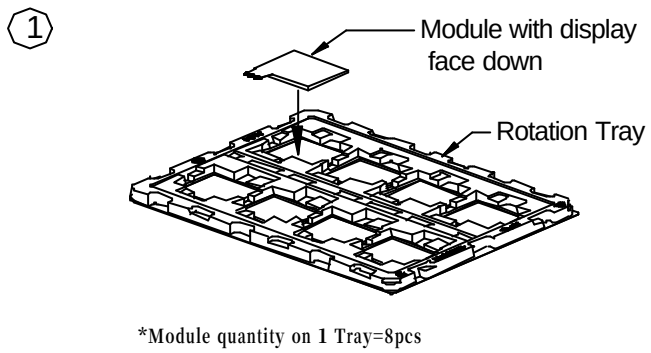
(3) The circuit below is designed on panel IC to avoid image sticking ..

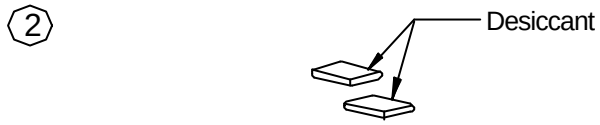


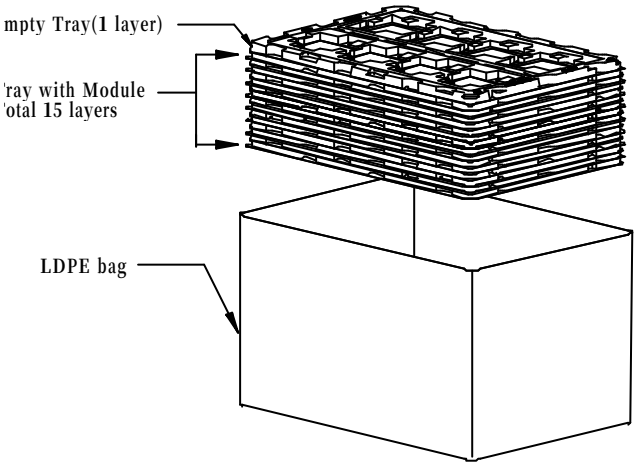
12. Mechanical Drawing

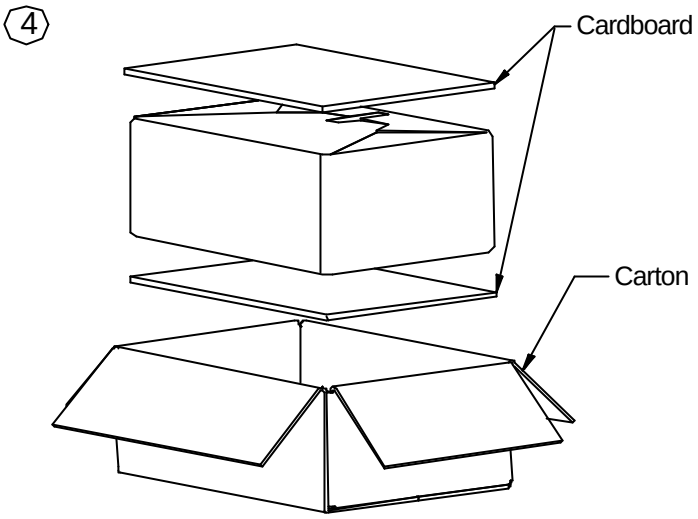


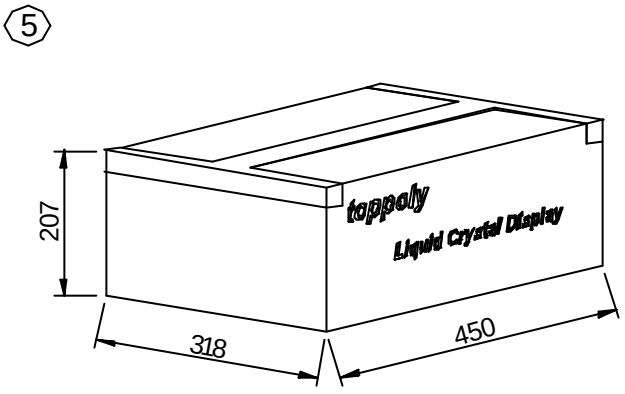
13. Packing Drawing



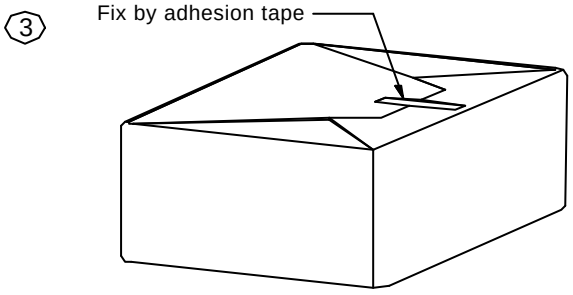








Module quantity in 1 carton=120pcs



TD035STED6 module delivery packing method

(1). Module packed into tray cavity with display face down.

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2 pcs desiccant put above the empty tray.

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4) Put 1pc cardboard inside the carton bottom, then pack the finished package into the carton.

(5). Carton sealing with adhesive tape.