TFT LCD Specification

Model NO.: TD035STED7

Customer Signature
Date

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Record of Reversion

Rev	Issued Date	Description
0.1	Feb, 25,2006	New
0.2	May,19 , 2006	Page 31 Modify pin #48 DE to NC,
1.0	Aug, 24, 2006	Modify 2 General information - Power consumption 3.1 TFT LCD module - pin #55 5.1 Driving TFT LCD Panel - Power Supply for H/V Driver, DVDD Supply Current, AVDD Supply Current, VGH Supply Current, VVEE Supply Current 5.2 DC/DC Spec

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1. FEATURES

The 3.5” LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it’s COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		64.0 X 85.0X4.10(Max 4.4)*	mm
Weight		47	g
Power consumption	LCD Panel + T-CON + L/S	15(Typ.)	mW
	Backlight	432 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

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3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Recommend connector:NAIS-AXK6F60345YJ

Pin	Symbol	I/O	Description	Remark
1	GND	-	Ground	
2	YU	O	Touch Panel Upper Side	
3	XR	O	Touch Panel Right Side	
4	YL	O	Touch Panel Lower Side	
5	XL	O	Touch Panel Left Side	
6	GND	-	Ground	
7	VCOM_I	I	VCOM Signal Input for LCD Panel	
8	VCOM_I	I	VCOM Signal Input for LCD Panel	
9	GND	-	Ground	
10	VCOM_L	O	Negative power output for VCOM	Connect capacitor (4.7~10uF/6V or more)
11	VGH	I	Positive voltage Positive voltage in pin for Level Shifter I/O	Power Supply (+10V)
12	VCOM_O	O	VCOM Signal of IC Output	
13	VCOM_O	O	VCOM Signal of IC Output	
14	VCOM_H	O	Positive power output for VCOM	Connect capacitor (4.7~10uF/6V or more)
15	GND	-	Ground	
16	AVDD	I	5V Input (Source driver)	
17	RESET	I	Reset signal	
18	ISC	-	NA	
19	IV6P	-	NA	
20	VDD2	I	2.8V Input(Power supply for booster)	Power Supply (+2.8V)
21	GND	-	Ground	
22	B00	I	Data Bit Input	
23	B01	I	Data Bit Input	
24	B02	I	Data Bit Input	
25	B03	I	Data Bit Input	
26	B04	I	Data Bit Input	
27	B05	I	Data Bit Input	
28	GND	-	Ground	
29	G00	I	Data Bit Input	

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30	G01	I	Data Bit Input	
31	G02	I	Data Bit Input	
32	G03	I	Data Bit Input	
33	G04	I	Data Bit Input	
34	G05	I	Data Bit Input	
35	GND	-	Ground	
36	R00	I	Data Bit Input	
37	R01	I	Data Bit Input	
38	R02	I	Data Bit Input	
39	R03	I	Data Bit Input	
40	R04	I	Data Bit Input	
41	R05	I	Data Bit Input	
42	GND	-	Ground	
43	VDD1	I	2.8V Input (Logic Supply Voltage)	Power Supply (+2.8V)
44	VS	O	Positive power output for source driver	Connect capacitor (4.7~10uF/6V or more)
45	GND	-	Ground	
46	MCLK	I	Clock signal	
47	GND	-	Ground	
48	NC	-	NA	
49	GND	-	Ground	
50	CS	I	Serial interface chip select	
51	SDA	I/O	Serial interface data input/output	
52	TB_RL	I	Gate shift direction select and Source shift direction select	
53	SCL	I	Serial interface clock input	
54	VSYNC	I	Vertical SYNC input	
55	HSYNC	I	Horizontal SYNC input	
56	VGH	I	Positive voltalge Positive voltage in pin for Level Shifter I/O	Power Supply (+10V)
57	VVEE	I	Input Voltage for gate off (-5.0V)	Power Supply (-5.0V)
58	LED-	I	Cathode of LED	
59	LED+	I	Anode of LED	
60	GND	-	Ground	

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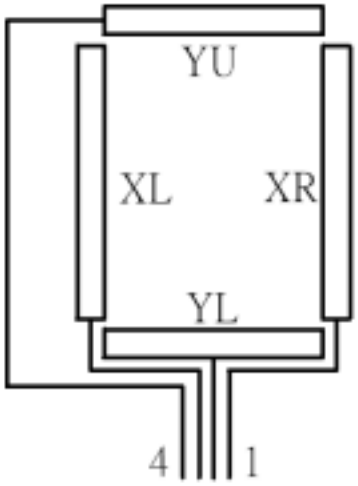
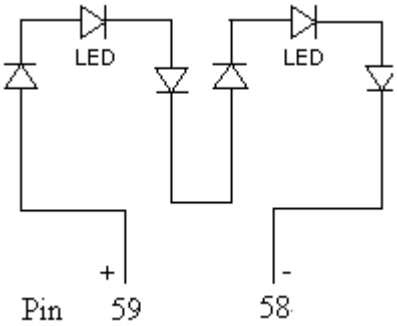
3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	3	XR	Touch Panel Right Side	
2	4	YL	Touch Panel Lower Side	
3	5	XL	Touch Panel Left Side	
4	2	YU	Touch Panel Upper Side	



3.3 Back light pin assignment



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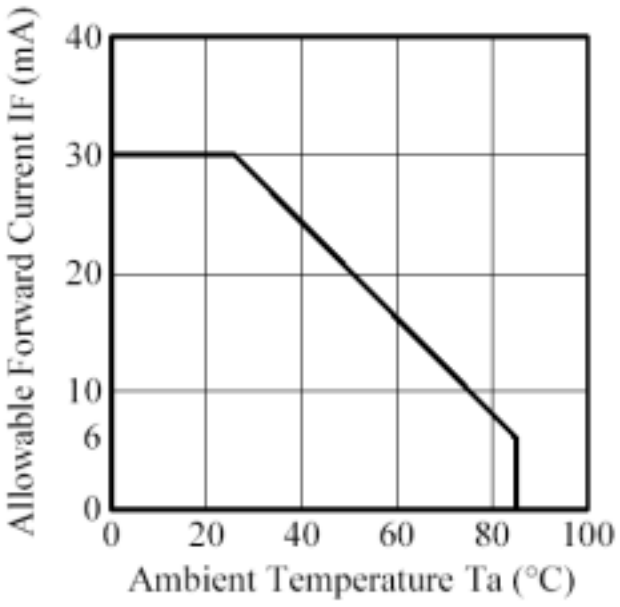
4. ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD1, VDD2	-0.3	+3.6	V	
	AVDD	-0.3	6	V	
Power Supply for H/V Driver	VGH	-0.3	+19	V	
	VVEE	-5.8	0	V	
Touch Panel Operation Voltage	V_{Touch}	-	5.5	V	
Backlight LED forward Voltage	V_F	-	4	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	25	mA	Note1
Operating Temperature	Topr	-10	+55	℃	
Storage Temperature	Tstg	-20	+70	℃	

Note 1. Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs. Allowable Forward Current



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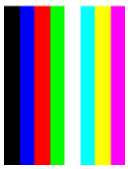
5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		VDD1	2.5	2.8	3.6	V	
		VDD2	2.5	2.8	3.6	V	
		AVDD	4.8	5.0	5.6	V	
Power Supply for H/V Driver		VGH	9.5	10	10.5	V	
		VVEE	-5.5	-5.0	-4.5	V	
Logic Input Voltage	High	VIH	0.8VDD1	—	VDD1	V	MCLK,HSYNC, VSYNC,DE,Data
	Low	VIL	VSS	—	0.2VDD1		
Leakage current		IL	-1	—	1	uA	
VDD1 Supply Current		I_{VDD1}	-	0.62	0.9	mA	Note 1
AVDD Supply Current		I_{AVDD}	-	2.5	3.0	mA	Note 2
VGH Supply Current		I_{VGH}	-	0.11	0.21	mA	
VVEE Supply Current		I_{VVEE}	-	0.05	0.15	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern:



Note 2: Gamma correction voltage is set to achieve the optimum at AVDD=5.0V. Use the voltage at level as close to 5.0V as possible.

5.2 DC/DC Spec

Item	Input voltage			Input Current	Input ripple(Max)	
	MIN	TYP	MAX			
VDD2	2.5V	2.8V	3.6V	0.62	50mV	
AVDD	4.8V	5.0V	5.6V	2.5	50 mV	Note 1
VGH	9.5V	10V	10.5V	0.11	150mV	
VVEE	-5.5 V	-5.0 V	-4.5 V	0.05	150mV	

Note 1: AVDD is analog voltage supply therefore use as less ripple as possible.

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5.3 Driving backlight Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	-	25	mA	LED/Part
Forward Current Voltage	V_F	-	(3.75)	4.2	V	I_F: 20mA ,LED/Part

Note : Backlight driving circuit is recommend as the fix current circuit.

5.4 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	100	-	1100	Ω	
Resistor between terminals (YU-YL)	Ry	100	-	1100	Ω	
Operation Voltage	V_{Touch}	-	5	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note 1
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	-	10	ms	
Minimum tension for detecting	-	-	80	-	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note 1. The minimum test force is 80 g.

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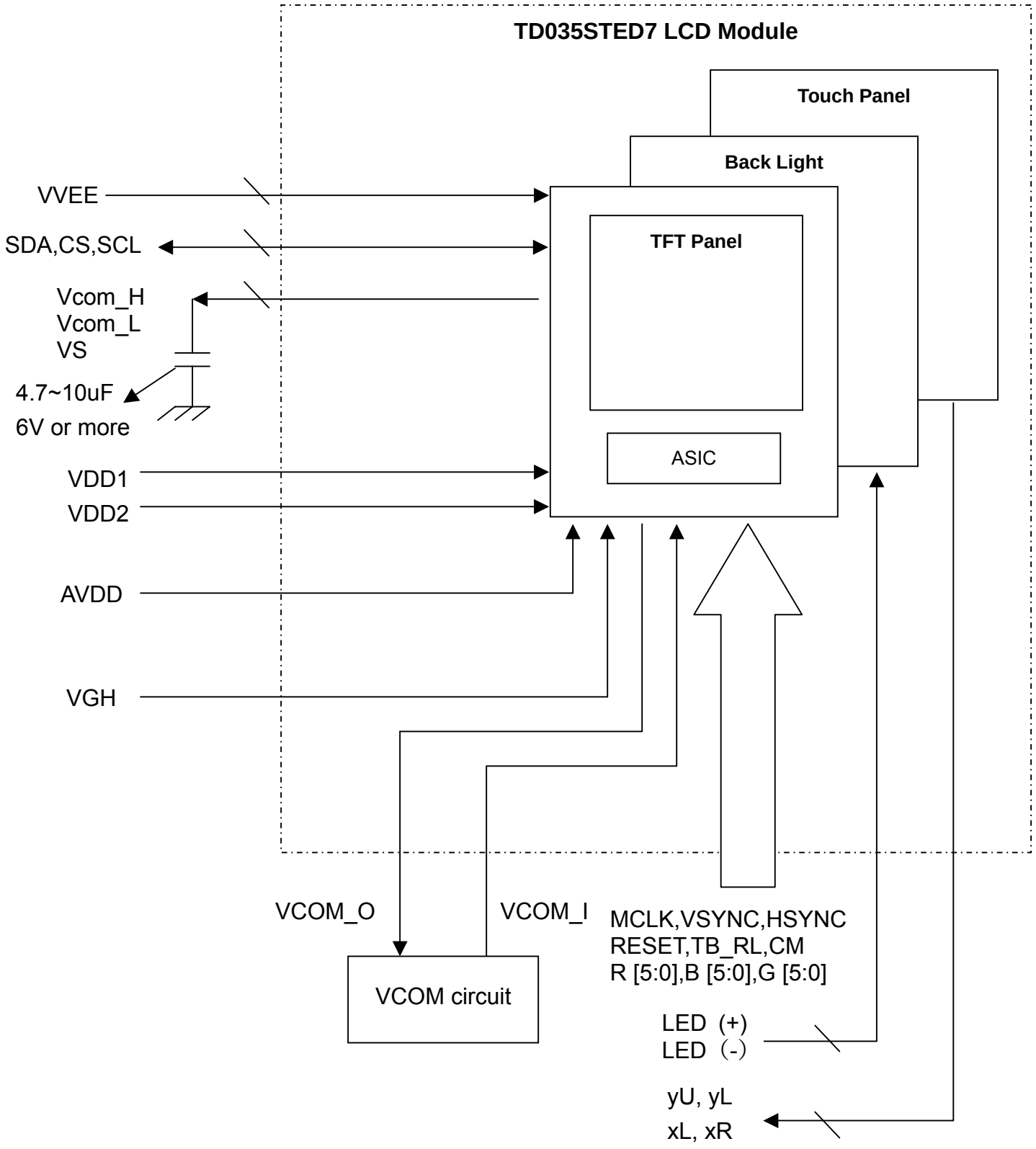
6. BLOCK DIAGRAM



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7. TIMING CHART

7.1 Display timing

Display Mode	Parameter	Symbol	Conditions	Ratings			Unit	Remark
				MIN	TYP	MAX		
Normal	Vertical cycle	VP		323	326	340	Line	
	Vertical data start	VDS	VS+VBP	2	4	—	Line	*Note1
	Vertical front porch	VFP		1	2	—	Line	
	Vertical blanking period	VBL	VS+VBP+VFP	3	6	—	Line	
	Vertical active area	VDISP		—	320	—	Line	
	Horizontal cycle	HP		260	280	300	dot	
	Horizontal front porch	HFP		4	10	—	dot	
	Horizontal Sync Pulse width	HS		8	10	—	dot	
	Horizontal Back porch	HBP		18	20	—	dot	
	Horizontal Data start	HDS	HS+HBP	26	30	—	dot	*Note2
	Horizontal active area	HDISP		240	240	240	dot	
	Clock frequency	fclk		5.02	6.39	6.85	MHz	
		tclk		199	156	146	nS	

(Note1) Please change the register R3 via SPI command to modify the VDS.

(Note2) Please change the register R4 via SPI command to modify the HDS.

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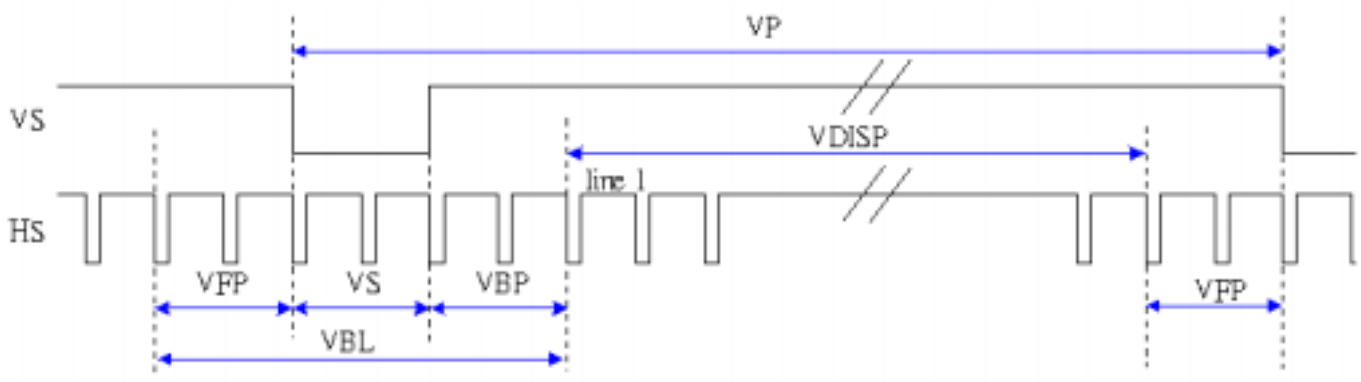
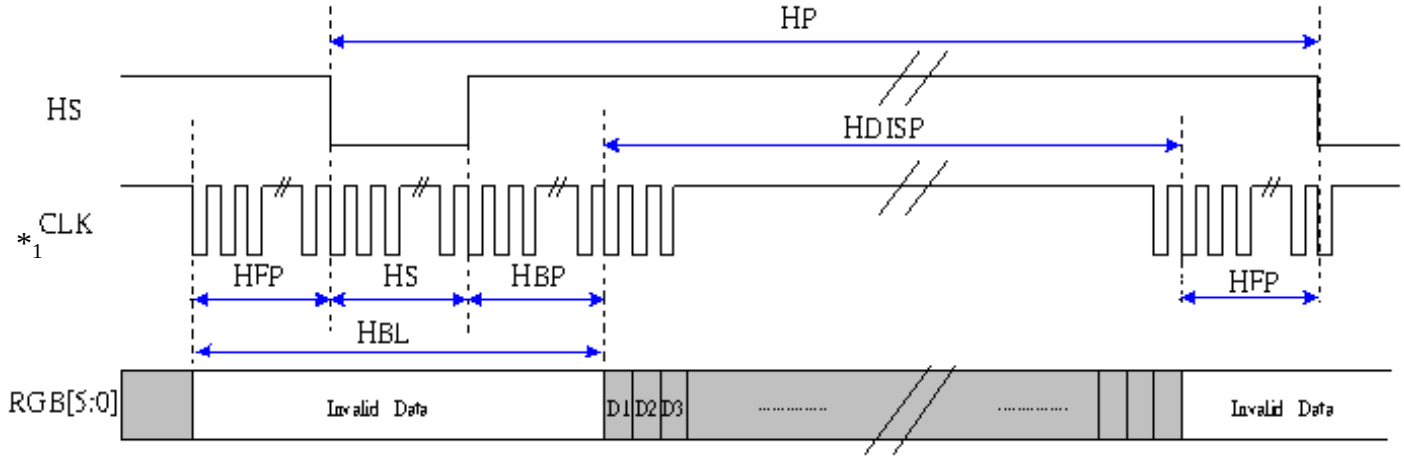
Input timing chart

＜Vertical Timing chart＞



＜Horizontal Timing chart＞



*1 The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

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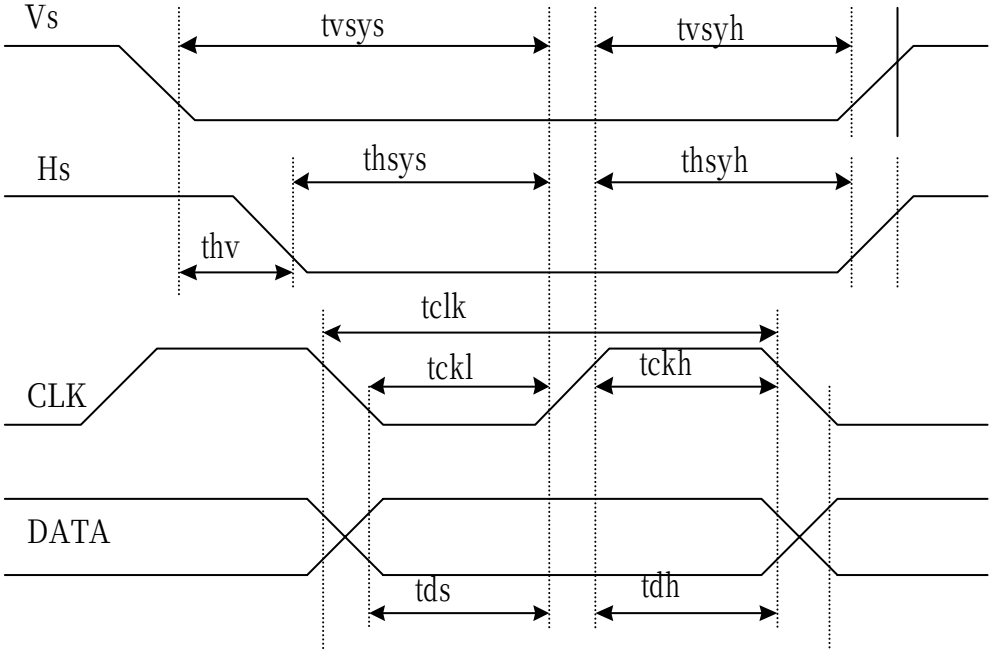
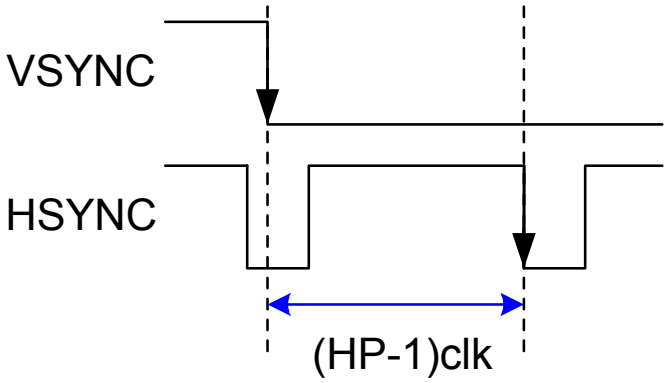
Setup/ Hold Timing chart

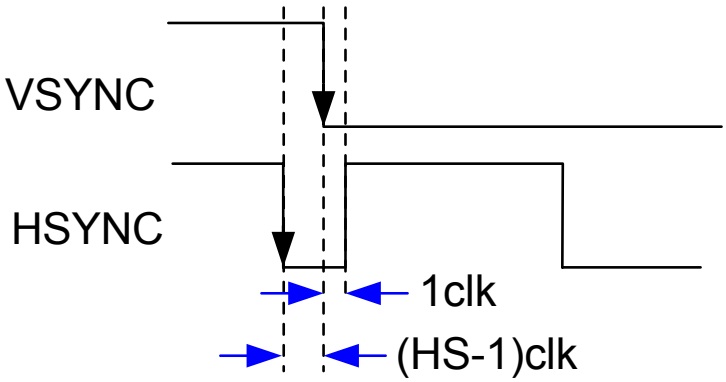


Phase difference of Sync.

Maximum Timing chart：



Minimum Timing chart:



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AC Characteristics:

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	—	—	ns
Vertical Sync. Hold time	tvsyh		20	—	—	ns
Horizontal Sync. Setup time	thsys		20	—	—	ns
Horizontal Sync. Hold time	thsyh		20	—	—	ns
Phase difference of Sync. Signal Falling edge	thv		-(HS-1)	—	1HP-1	clk
Clock “L” Period	tCKL		30	50	70	%
Clock “H” Period	tCKH		30	50	70	%
Data setup time	tds		20	—	—	ns
Data Hold time	tdh		20	—	—	ns
Digital logic input	Trise/Tfall				15	ns

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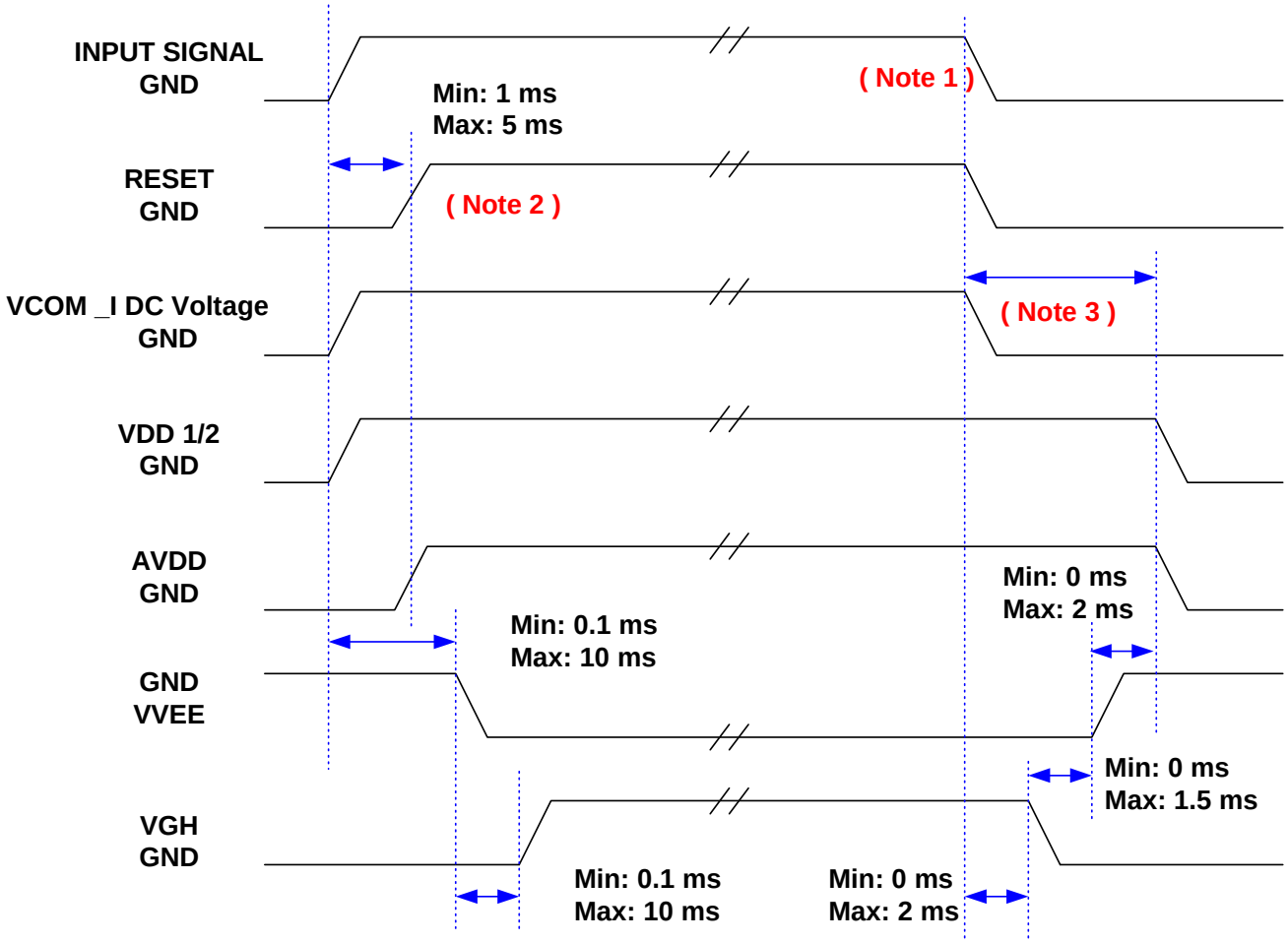
8. Power On/Off Sequence



(Note 1) The VCOM_I DC voltage can be shut down between this area.

(Note 2) Display start at the 10th falling edge of VSYNC after RESET rising (first 1 frame=white)

(Note 3) To avoid image retention , please input white image for two frame before power off.

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9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off / w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	70	85	-	Degree	Note 9-1
	Θ21+Θ22			75	95	-		
Chromaticity	White	x	Θ=0°	0.26	0.31	0.36	-	Note 9-3
		y		0.30	0.35	0.40	-	
Contrast Ratio	CR		Θ=0°	10:1	15:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	7	10	-	%	Note 9-4

(2) Back Light On /w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	100	120	-	Degree	Note 9-1
	Θ21+Θ22			90	110	-		
Response Time	Tr+Tf		Θ=0°	-	35	45	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	80:1	100:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F =20mA	90	115	-	cd/m^2	Note 9-7
NTSC	-		-	32	36	-	%	Note 9-7
Uniformity	-		-	70	80	-	%	Note 9-8
Chromaticity	White	x	Θ=0°	0.260	0.310	0.360	-	Note 9-3
		y		0.280	0.330	0.380		
	R	x		0.500	0.550	0.600	-	
		y		0.270	0.320	0.370		
	G	x		0.270	0.320	0.370	-	
		y		0.490	0.540	0.590		
	B	x		0.100	0.150	0.200	-	
		y		0.070	0.120	0.170		

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9.2 Basic measure condition

(1) Driving voltage

VDD= 10.0V, VEE=-5.5V

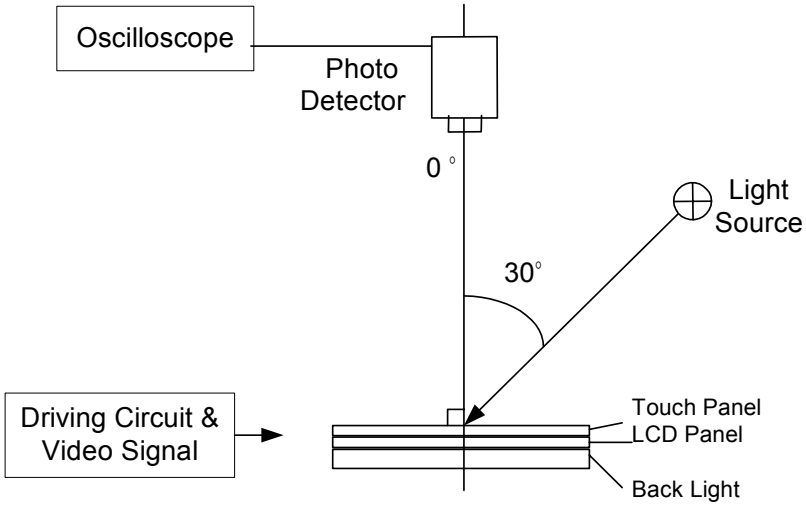
(2) Ambient temperature: Ta=25℃

(3) Testing point: measure in the display center point and the test angle Θ=0°

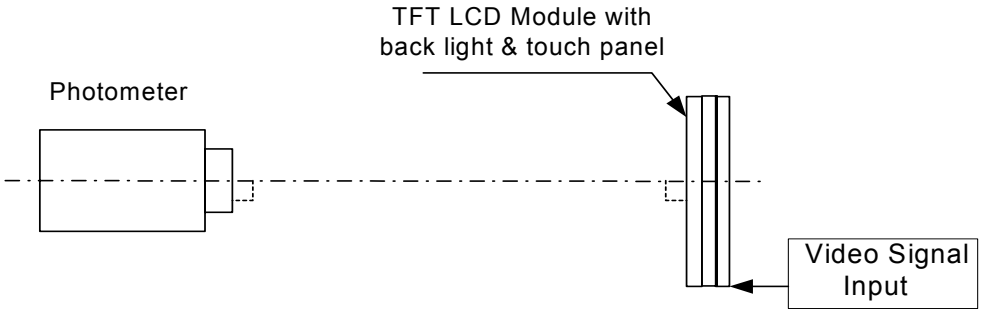
(4) Testing Facility

Environmental illumination: ≤ 10 Lux

a. System A



b. System B



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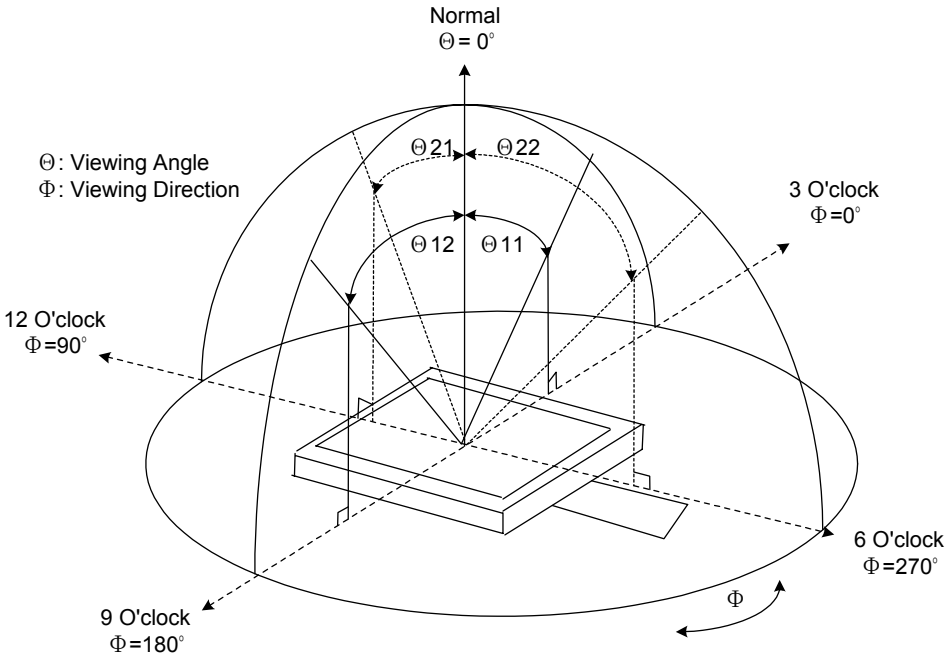
Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 9-3: White chromaticity as back light off: (Measure System A),

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system B. calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \text{ X } \text{Reflectance factor of reflectance standard}$$

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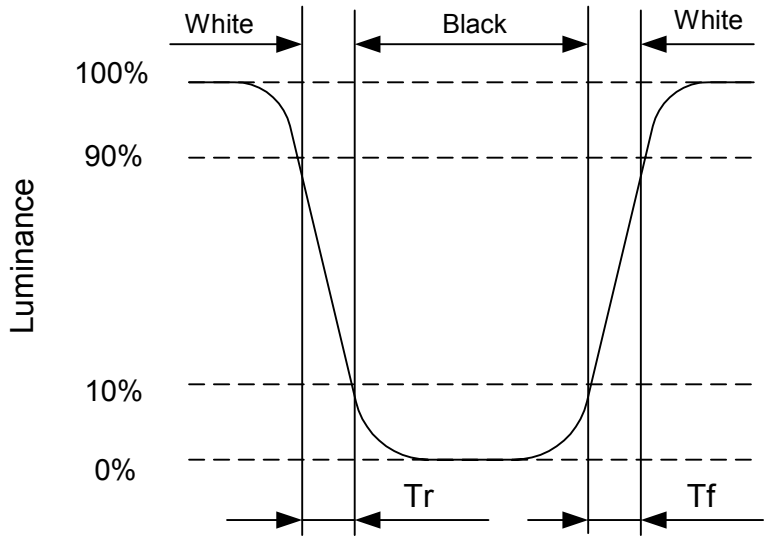
Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

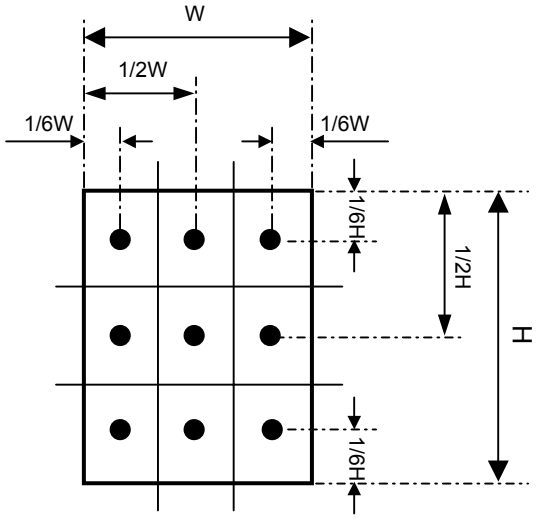
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

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10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20℃, 240hrs
6	Thermal Shock (non-operation)	-20℃ ← → 70℃,30 cycles 30 min 30 min
7	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times
9	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R0.8, HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
10	Writing Friction Resistance Test (Touch Panel)	Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35m 100000 times

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11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.
(2) The machine and working table for the panel should have ESD protection strategy.
(3) In handling the panel, ionized air flowing decrease the charge in the environment is necessary.
(4) In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

(1) Working environment should be clean room.
(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionizer to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.
(2) When any dust or stain is observed on a film surface, clean it using a lens cleaner for glasses or something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.
(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.
(3) Water drop on the surface when panel is powered on will corrode panel electrode.
(4) Before opening up the packing bag, watch out the environment for the panel storage. High temperature and high humidity environment is prohibited.
(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

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12. Application Note

12.1 Design notes on touch panel

(1) Explanation of each boundary of touch panel

A.Boundary of Double-sided adhesive

a. Electrically detectable within this zone.
When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B.Viewing area

a. Cosmetic inspection to be done for this area.
This area is set as inside of boundary of double-sided adhesive with tolerance.

C.Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

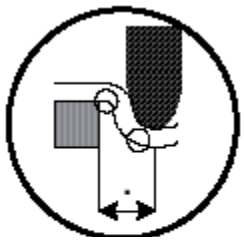
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

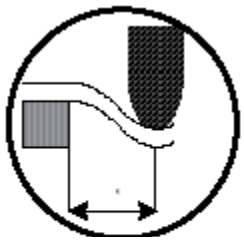
D.Active area

a. This area is where the performance is guaranteed.
This area set as some distance inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.

b. Please refer to the attached module drawing for the bezel opening and window size design.



There is some possibility to damage ITO



No Damage to ITO

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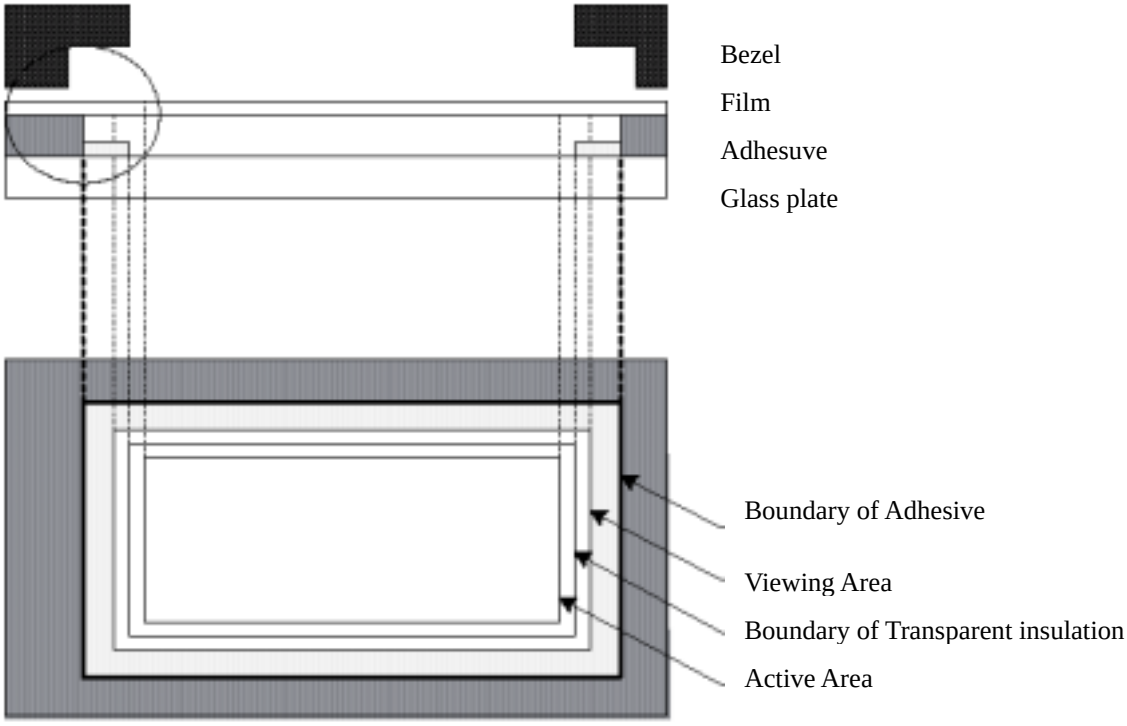
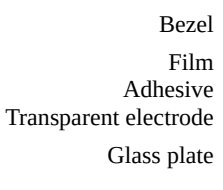


(2) Housing and touch panel

a. Please have clearance between the side of touch panel, and any conductive material such as metal frame.(drawing.1) Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause malfunction.



Drawing 1

Drawing 2

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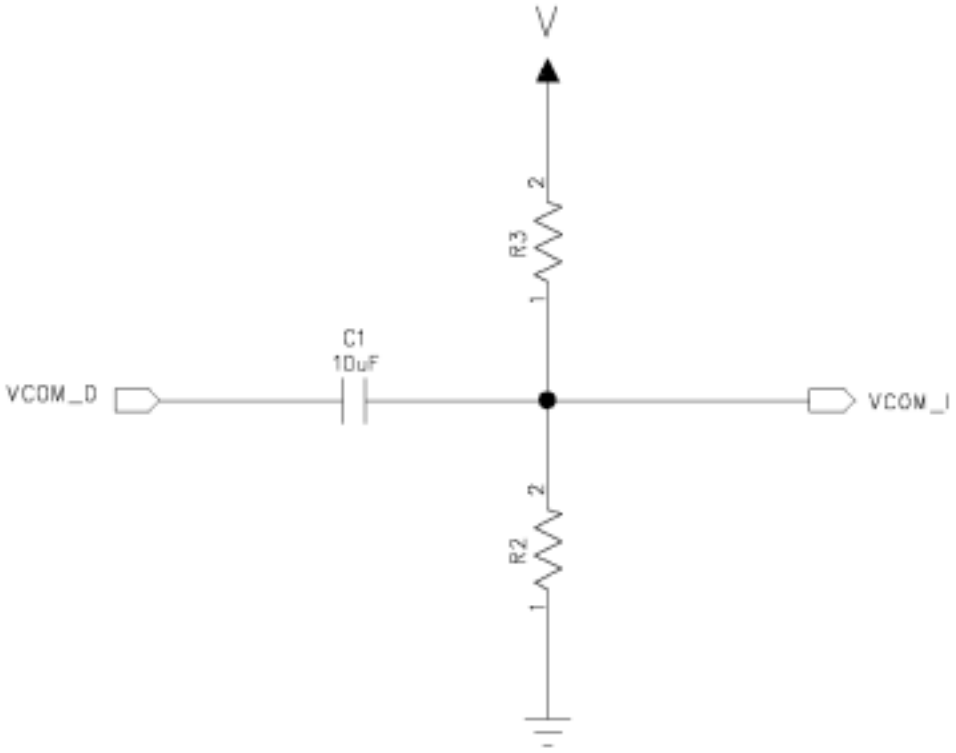
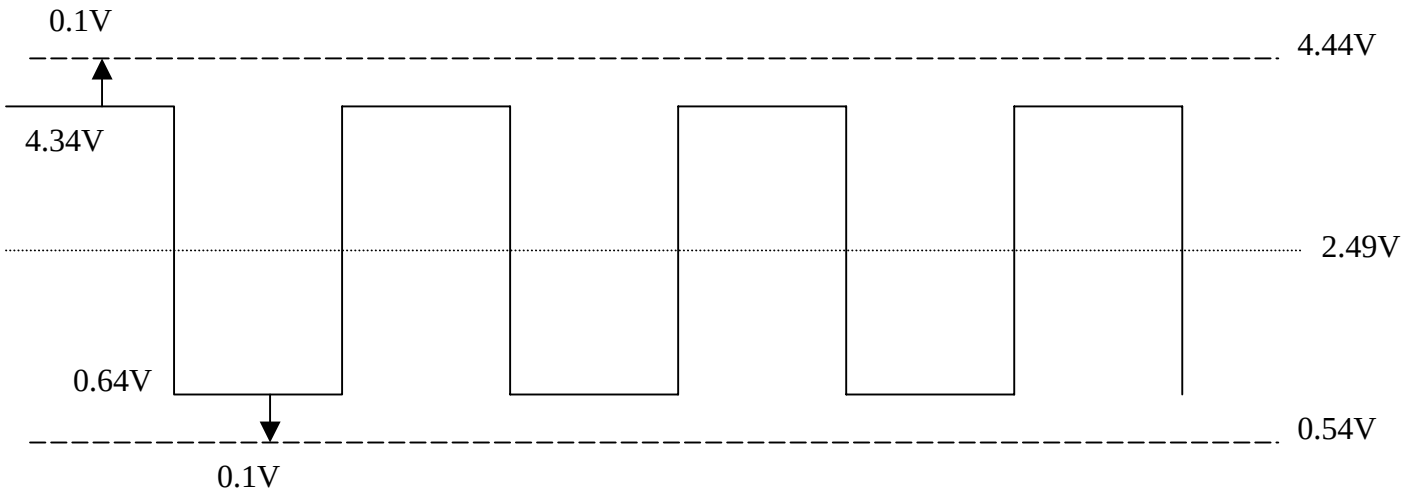
12.2 Note for Vcom circuit

The circuit is designed for V-com fine-tune, please refer the circuit below to design application circuit.



VCOM_I :



Note:

V：5 V

R2：10~30 K Ohm

R3：10~30 K Ohm

Resistors tolerance：0.5~1 %

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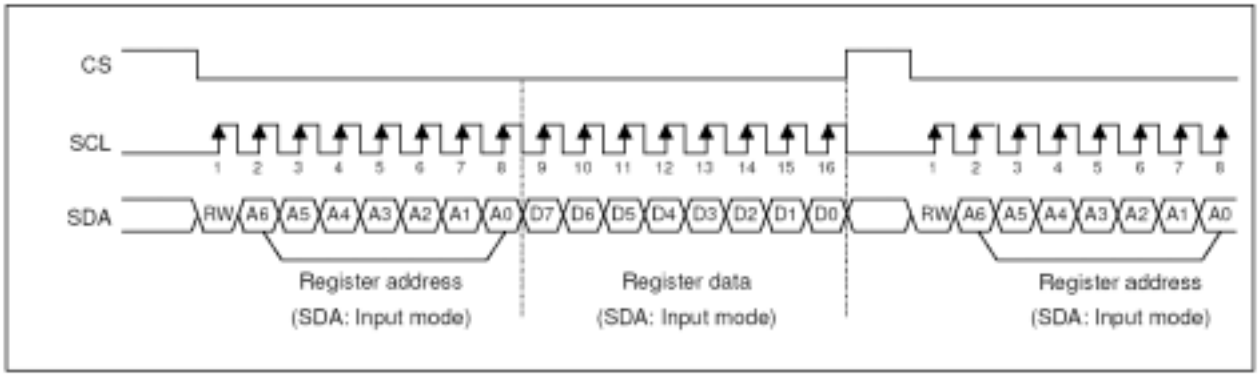
12.3 Note for SPI command

The LCM support the 3-pin serial interface to set internal register. Read/Write bit RW, Serial address A6 to A0 and serial data D7 to D0 are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

Serial Interface Signal Timing Chart

Write Mode (RW=L)



The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommand checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then LCM will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.

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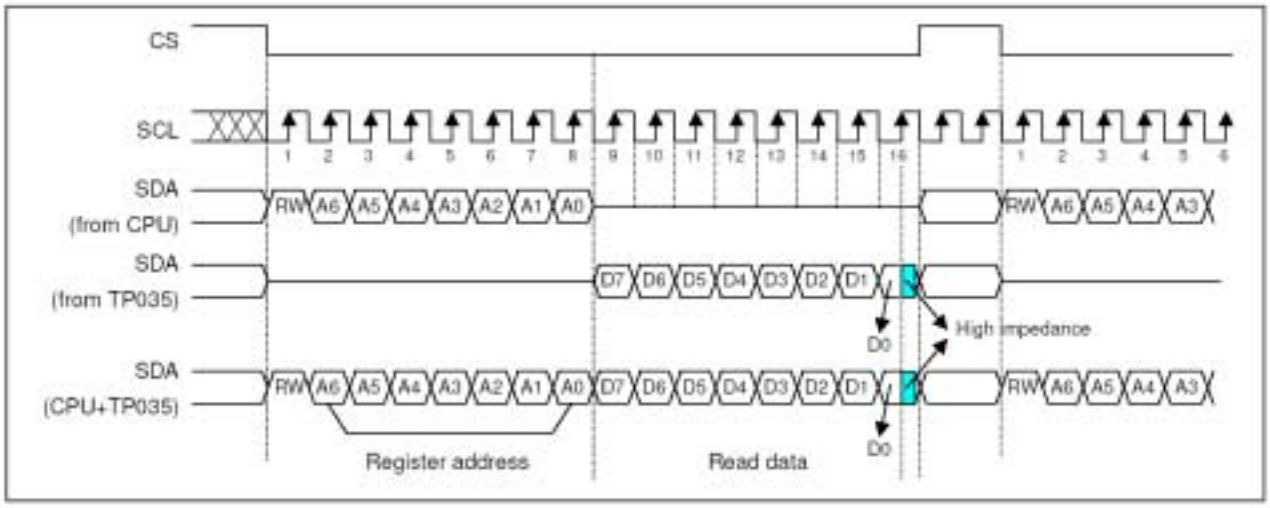
Read Mode (RW=H)



The read mode of the interface means that the micro controller reads data from the LCM.
To do so the micro controller first has to send a command: the read status command.
Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

The LCM samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges.
Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The LCM can read data of the Register0 to Register63

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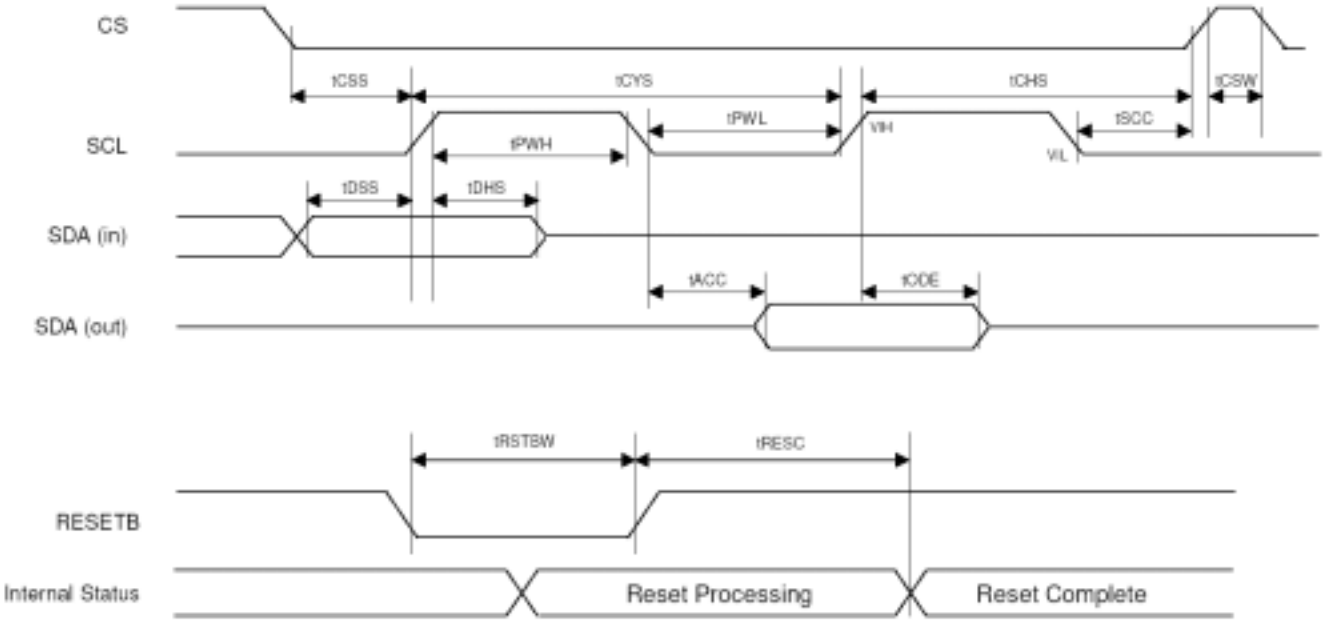
Serial interface and Reset waveform (VIH=0.8VDD1, VIL=0.2VDD1)



Serial interface and Reset						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock cycle	tCYS	-	150	-	-	ns
Clock High Period	tPWH	-	60	-	-	ns
Clock Low Period	tPWL	-	60	-	-	ns
Data Set-up Time	tDSS	-	60	-	-	ns
Data Hold Time	tDHS	-	60	-	-	ns
CS High width	tCSW	-	1	-	-	us
CS Set-up Time	tCSS	-	60	-	-	ns
CS Hold Time	tCHS	-	70	-	-	ns
SCL to CS	tSCC		40	-	-	ns
Output Access Time	tACC		10	-	50	ns
Output Disable Time	tODE		25	-	80	ns
RSTB low width	tRSTBW	-	1000	-	-	ns
RESET complete time	tRESC	-	-	-	1000	ns

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Command descriptions：

Reset the internal register by setting low level the RESETB pin or software reset command.

Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D	D4	D3	D2	D1	D0		
R0	00h	CHIPID[2:0]									Chip ID (Read only)	The Chip ID can be changed by MASK Option.
			1								D7=1 for SPFD5413	
					0	0	0				ID0	
					0	0	1				ID1	
					0	1	1				ID2	
					-	-	-					
					1	1	1				ID7	
		REVID[2:0]									Revision ID (Read only)	The Revision ID can be changed by MASK Option.
								0	0	0	REV 0	
								0	0	1	REV 1	
								0	1	0	REV2	
								0	1	1	REV3	
								-	-	-		
								1	1	1	REV 7	
R1	68h	VCM[7:5]									VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change
			0	0	0						-0.3V	
			0	0	1						-0.2V	
			0	1	0						-0.1V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	
		VCM[3:0]									VCOM voltage select	VCOM_DC value setting
							0	0	0	0	VCOMH=3.90V ; VCOML=0.20V	
							0	0	0	1	VCOMH=3.92V ; VCOML=0.22V	
							0	0	1	0	VCOMH=3.94V ; VCOML=0.24V	
							0	0	1	1	VCOMH=3.96V ; VCOML=0.26V	
							0	1	0	0	VCOMH=3.98V ; VCOML=0.28V	
							0	1	0	1	VCOMH=4.00V ; VCOML=0.30V	
							0	1	1	0	VCOMH=4.02V ; VCOML=0.32V	
							0	1	1	1	VCOMH=4.04V ; VCOML=0.34V	
							1	0	0	0	VCOMH=4.06V ; VCOML=0.36V	
							1	0	0	1	VCOMH=4.08V ; VCOML=0.38V	
							1	0	1	0	VCOMH=4.10V ; VCOML=0.40V	
							1	0	1	1	VCOMH=4.12V ; VCOML=0.42V	
							1	1	0	0	VCOMH=4.14V ; VCOML=0.44V	
							1	1	0	1	VCOMH=4.16V ; VCOML=0.46V	
							1	1	1	0	VCOMH=4.18V ; VCOML=0.48V	
							1	1	1	1	VCOMH=4.20V ; VCOML=0.50V	
R2	00h											Mode slection
		SYNCP									SYNC polarity select	
				0							Negative	
				1							Positive	
		DINT			0						Input data mapping select	
					1						18 bit interface (262k color)	
											16 bit interface (65k color, R:G:B=5:6:5)	
		DCKP									Input clock polarity change	
						0					No change	
						1					Change	
R3	04h	VSTS[3:0]									Vertical valid data start time select (VBP)	Default: QVGA = 4 HSYNC QCIF+ = 7 HSYNC 128x160 = 13 HSYNC 240x240 = 4 HSYNC
							0	0	0	0	2 HSYNC	
							0	0	0	1	2 HSYNC	
							0	0	1	0	2 HSYNC	
							0	0	1	1	3 HSYNC	
							0	1	0	0	4 HSYNC	
							0	1	0	1	5 HSYNC	
							-	-	-	-	-	
							1	1	1	1	15 HSYNC	

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Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R4	1Dh	HSTS[5:0]									Horizontal valid data start time select (HBP)	Default: QVGA = 30 DCK QCIF+ = 44 DCK 128x160 = 36 DCK 240x240 = 30 DCK
				0	0	0	0	0	0	0	10 DCK	
				0	0	0	0	0	1	0	10 DCK	
				0	0	0	0	1	0	0	10 DCK	
				0	0	0	0	1	1	0	10 DCK	
				0	0	0	1	0	0	0	10 DCK	
				0	0	0	1	0	1	0	10 DCK	
				0	0	0	1	1	0	0	10 DCK	
				0	0	0	1	1	1	0	10 DCK	
				0	0	1	0	0	0	0	10 DCK	
				0	0	1	0	0	1	0	10 DCK	
				0	0	1	0	1	0	0	10 DCK	
				0	0	1	0	1	1	0	11 DCK	
				0	0	1	1	0	0	0	12 DCK	
					-	-	-	-	-	-	-	
				0	1	1	1	1	0	0	30 DCK	
					-	-	-	-	-	-	-	
				1	1	1	1	1	1	1	63 DCK	
R5	01h	PARS[7:0]									Partial start line select	When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARS[8]=0, Gate256 is selected when PARS[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARS[8]=0, Gate257 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARS[8]=0, Gate258 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARS[8]=0, Gate259 is selected when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	1	1	1	1	1	1	Gate63 is selected when PARS[8]=0, Gate319 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	0	Gate64 is selected when PARS[8]=0, Gate320 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	1	Gate65 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	1	1	Gate127 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	0	0	Gate128 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	0	1	Gate129 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	1	0	Gate130 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
R6	00h	PARS[8]									Partial start line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	
R7	20h	PARE[7:0]									Partial end line select	When VSYNC+HSYNC+DE mode, DE=H: Normal display line DE=L: Non-display line (White) When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARE[8]=0, Gate256 is selected when PARE[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARE[8]=0, Gate257 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARE[8]=0, Gate258 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARE[8]=0, Gate259 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	0	1	1	1	1	1	Gate31 is selected when PARE[8]=0, Gate286 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	0	Gate32 is selected when PARE[8]=0, Gate287 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	1	Gate33 is selected when PARE[8]=0, Gate288 is selected when PARE[8]=1	
			0	0	1	0	0	0	1	0	Gate34 is selected when PARE[8]=0, Gate289 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	1	1	1	1	1	1	Gate63 is selected when PARE[8]=0, Gate319 is selected when PARE[8]=1	
			0	1	0	0	0	0	0	0	Gate64 is selected when PARE[8]=0, Gate320 is selected when PARE[8]=1	
			0	1	0	0	0	0	0	1	Gate65 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
R8	00h	PARE[8]									Partial end line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	

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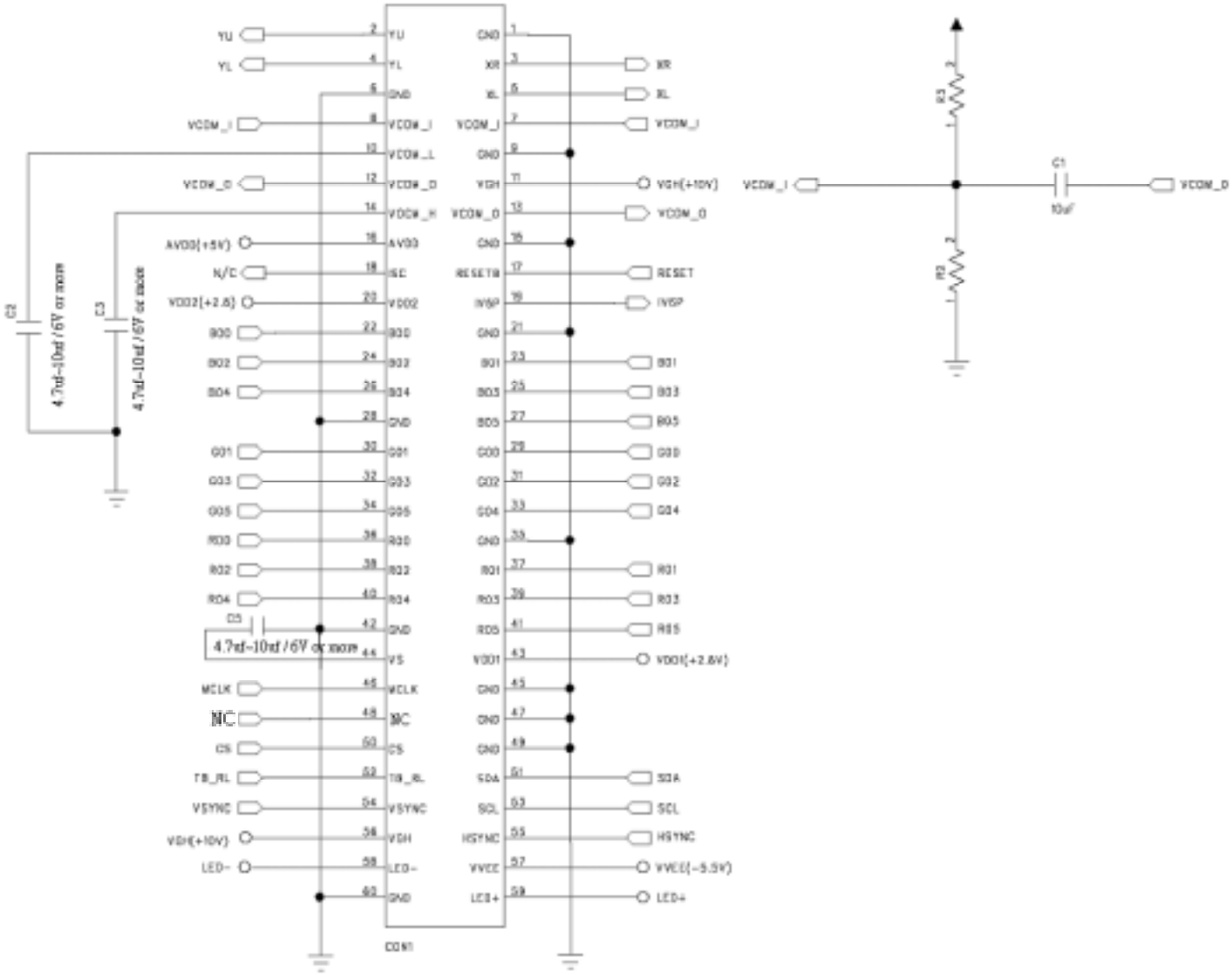
Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R10	00h	CMDR									Software reset	
										0	Normal	
										1	Software reset	
R11	68h	VCM8[7:5]									VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change (8 color partial mode)
			0	0	0						-0.3V	
			0	0	1						-0.2V	
			0	1	0						-0.1V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	

12.4 Notes for FPC circuit layout



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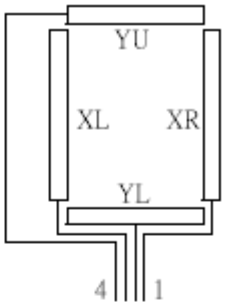
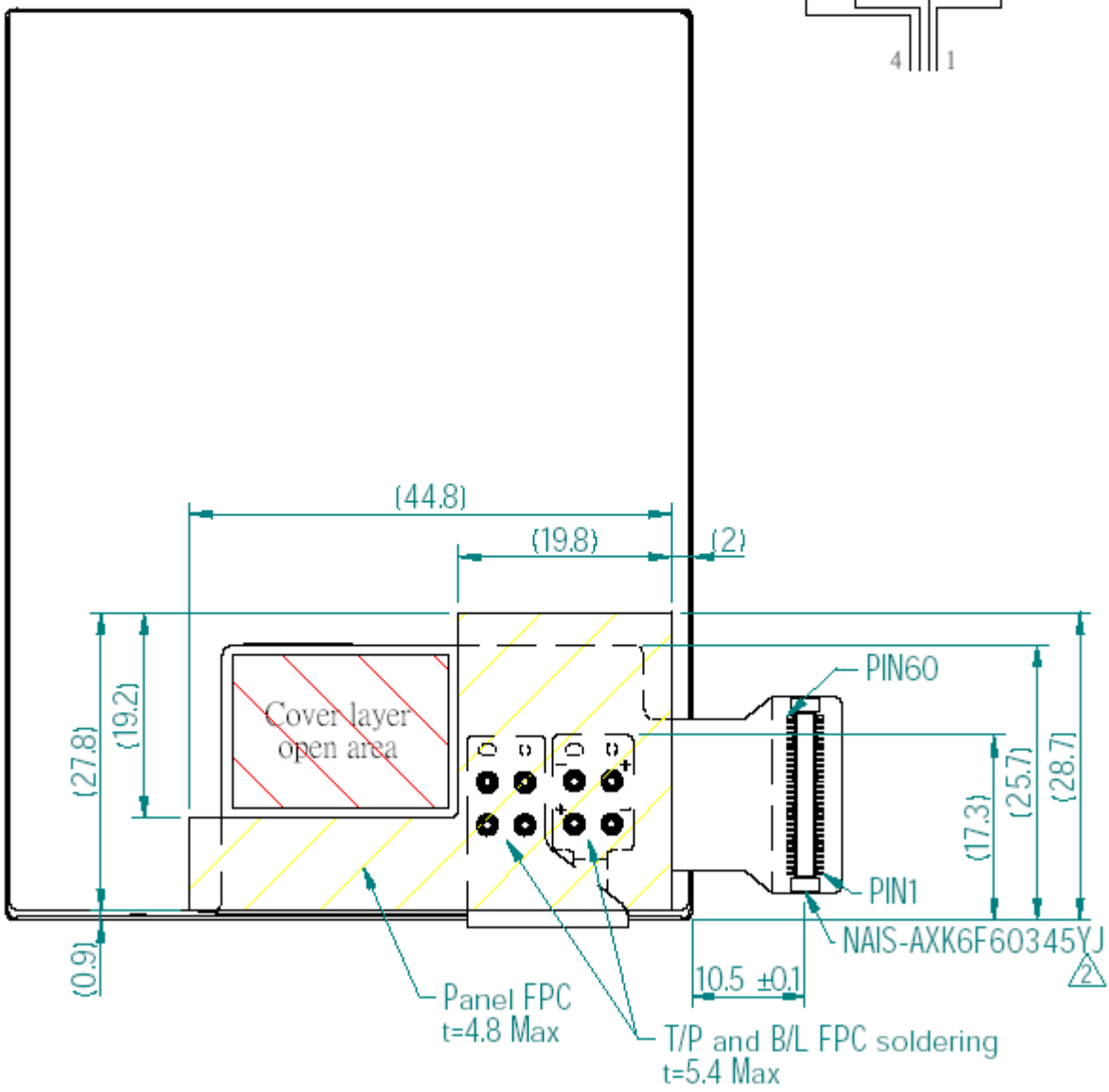
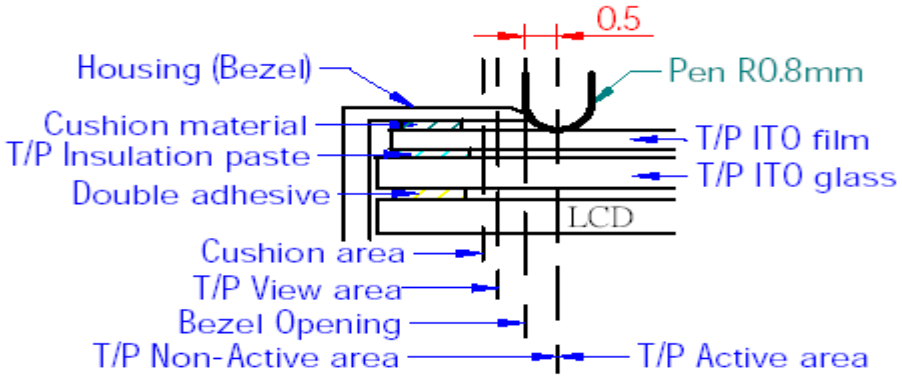
Pin Assignment for Touch panel







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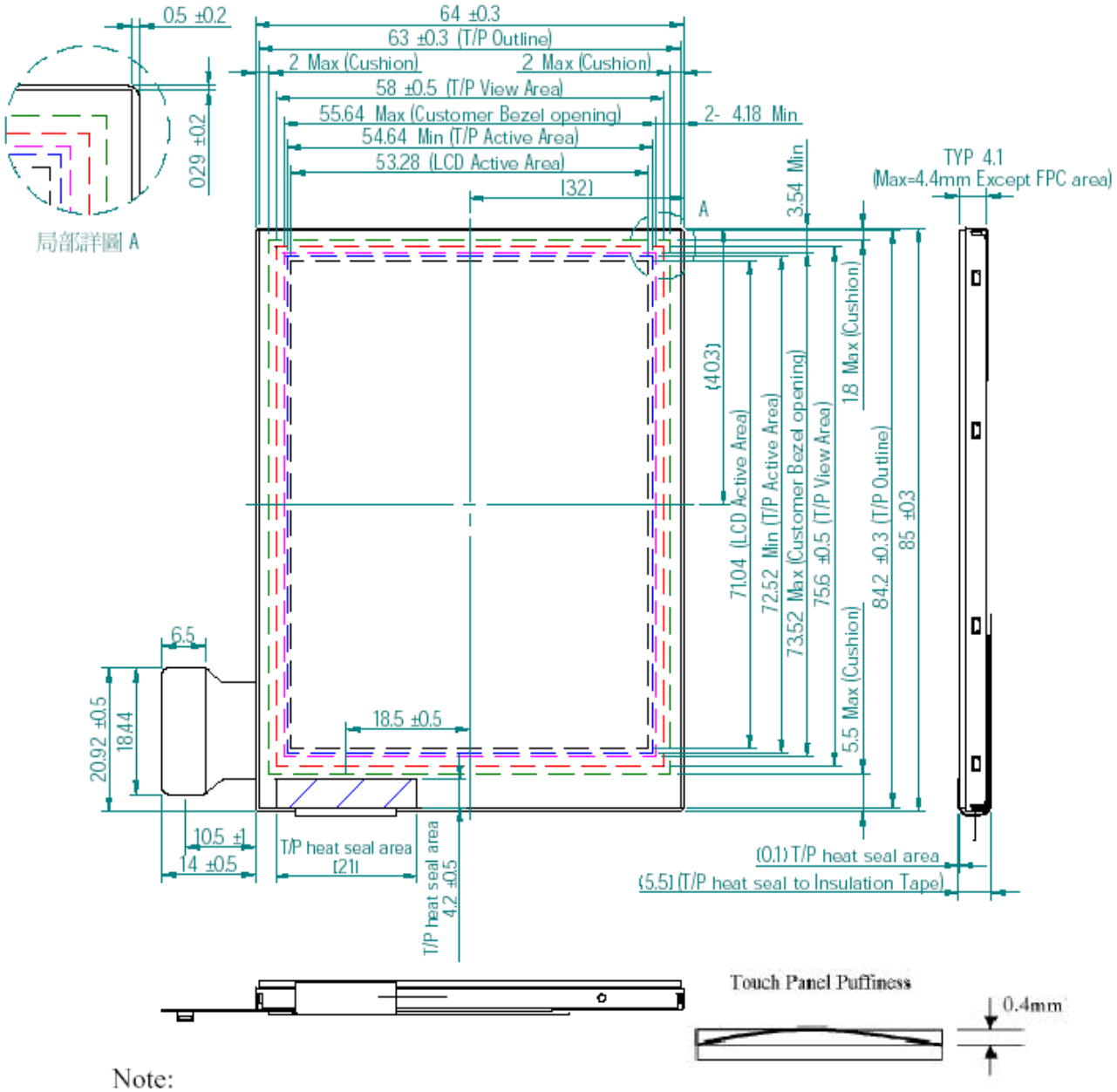

Note:

1. The dimension without tolerance is for reference only.
2. Touch Panel Puffiness Max=0.4mm

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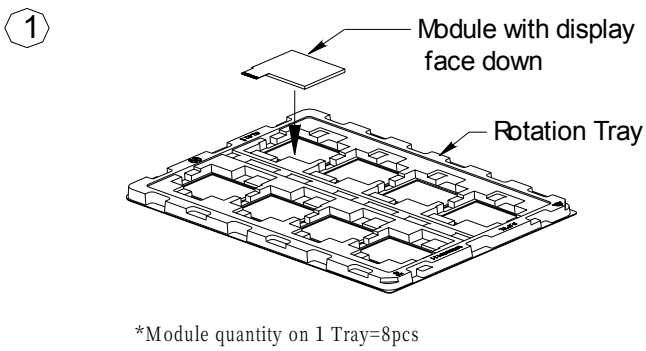
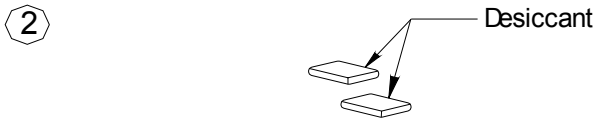
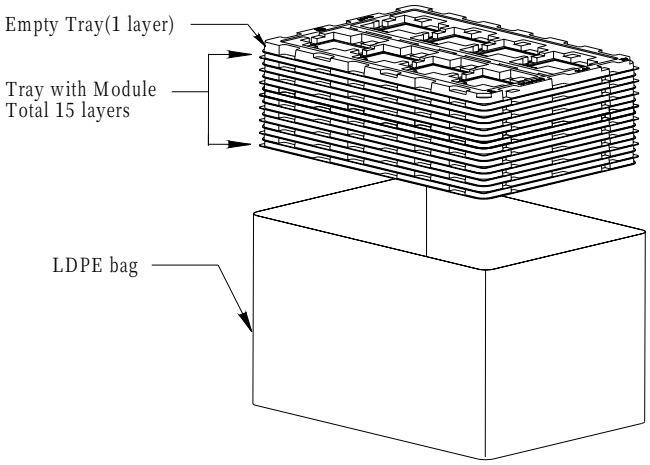
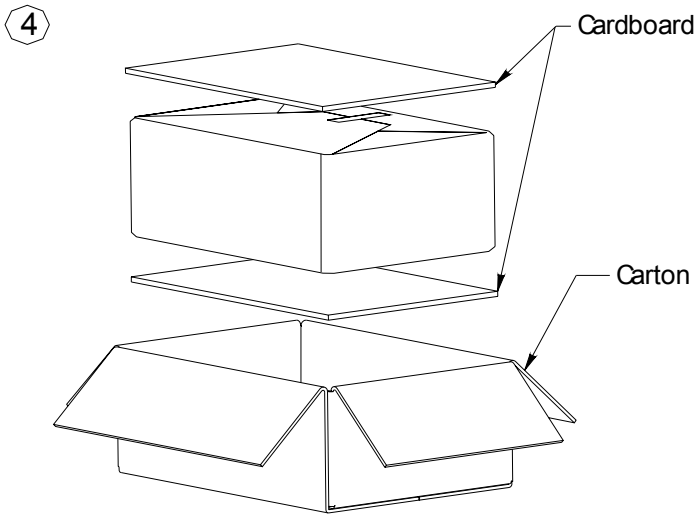
14. Packing Drawing

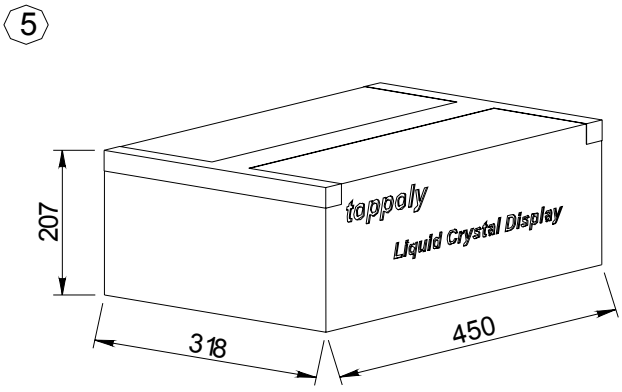


*Module quantity on 1 Tray=8pcs

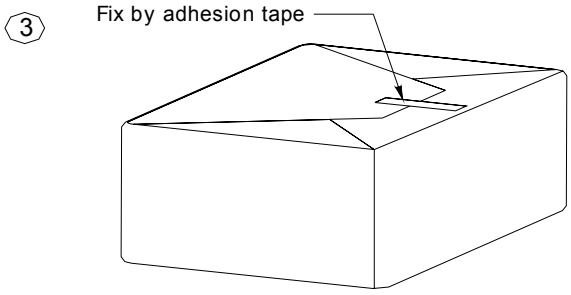








Module quantity in 1 carton=120pcs



TD035STED7 module delivery packing method

(1). Module packed into tray cavity with display face down.

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2 pcs desiccant put above the empty tray.

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4) Put 1pc cardboard inside the carton bottom, then pack the finished package into the carton.

(5). Carton sealing with adhesive tape.

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