Target

Ver.: 0.00

TFT LCD Specification

Model Name: TD080WGCA1

Customer Signature
Date

This technical specification is subjected to change without notice.

Table of Contents

NO.	Item	Page
	Cover Sheet	1
	Table of Contents	2
	Record of Revision	3
1	Features	4
2	General Specifications	4
3	Input / Output Terminals	5
4	Absolute Maximum Ratings	8
5	Electrical Characteristics	8
6	Timing Chart	10
7	Optical Characteristics	12
8	Reliability	14
9	Handling Cautions	15
10	Mechanical Drawing	16

Record of Revision

Rev	Issued Date	Description
0.00	Jul 10, 2006	New Create

1. FEATURES

The 8.0”(20.29 cm) LCD module is an active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used. Horizontal drivers are built on the panel. Horizontal scan can be from left to right or from right to left and Vertical scan can be from up to down or from down to up. The product is designed for the requirement of the green product, and the specification complies with Toppoly’s “Green Product Chemical Substance Specification Standard Hand Book”.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	8.0(20.29)	Inch (cm)
Display Type	Transmissive	
Active Area (HxV)	174 x 104.4	mm
Number of Dots (HxV)	800 X RGB X 480	dot
Dot Pitch (HxV)	0.0725x0.2175	mm
Color Arrangement	RGB Stripe	
Color Numbers	262K	
Outline Dimension (HxVxT) *	190 x 122 x 6.8	mm
Weight	TBD	g

* Exclude protrusions

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD Panel

Connector type: FH12-30S-0.5SH or Compatible

Pin	Symbol	I/O	Description	Remark
1	VCOM	--	Common voltage	
2	VEE	--	Power supply (-4V)	
3	VDD	--	Power supply (+13V)	
4	CSVO	I	CSV=H, CSVO=-6V CSV=L, CSVO=12V	
5	XCSVO	I	CSV=H, XCSVO=12V CSV=L, XCSVO=-6V	
6	GND	--	Ground for digital circuit	
7	AVSS	--	Ground for analog circuit	
8	POLC4	I	POL period control.	
9	POLC3	I	POL period control.	
10	POLC2	I	POL period control.	
11	POLC1	I	POL period control.	
12	VCC		Power supply (3.3V)	
13	CMOSB	I	CMOS & PMOS timing select CMOSB=H, CMOS timing CMOSB=L, PMOS timing	
14	OFPTON	I	Control Self-protection function OFPTRN=H, Control Self-protection function is on OFPTRN=L, Control Self-protection function is off	
15	OFPTRN	I	Self-protection function Intentionally writes black/White screen while getting abnormal signals. But if the signal returns normal, display normal screen. OFPTRN=H, The output data will produce full white pattern. OFPTRN=L, The output data will produce full black pattern.	
16	CKHP2	I	CKH plane timing adjust 2	
17	CKHP1	I	CKH plane timing adjust 1	
18	ENBP2	I	ENB period adjust 2	
19	ENBP1	I	ENB period adjust 1	

20	B5	I	Digital Input data blue5	
21	B4	I	Digital Input data blue4	
22	B3	I	Digital Input data blue3	
23	B2	I	Digital Input data blue2	
24	B1	I	Digital Input data blue1	
25	B0	I	Digital Input data blue0	
26	AVDD		Power supply for analog circuit	
27	V16	I	Gamma correction reference voltage	
28	V14	I	Gamma correction reference voltage	
29	V13	I	Gamma correction reference voltage	
30	V12	I	Gamma correction reference voltage	
31	V9	I	Gamma correction reference voltage	
32	V8	I	Gamma correction reference voltage	
33	V5	I	Gamma correction reference voltage	
34	V4	I	Gamma correction reference voltage	
35	V3	I	Gamma correction reference voltage	
36	V1	I	Gamma correction reference voltage	
37	G5	I	Digital Input data green5	
38	G4	I	Digital Input data green4	
39	G3	I	Digital Input data green3	
40	G2	I	Digital Input data green2	
41	G1	I	Digital Input data green1	
42	G0	I	Digital Input data green0	
43	R5	I	Digital Input data red5	
44	R4	I	Digital Input data red4	
45	R3	I	Digital Input data red3	
46	R2	I	Digital Input data red2	
47	R1	I	Digital Input data red1	
48	R0	I	Digital Input data red0	
49	DENB	I	Data enable	
50	NCLK	I	Clock input. Latching source data onto the line latches at the rising edge.	
51	VS	I	VSYNC	
52	HS	I	HSYNC	
53	RS3	I	Input resolution select pin	
54	RS2	I	Input resolution select pin	

55	RS1	I	Input resolution select pin	
56	REV	I	DATA polarity inverting pin REV=L normal white REV=H normal black	
57	CSV	I	Panel Vertical Line scan direction L => CSVO=H => From down to up H=> CVSO=L => From up to down	Note 3-1
58	LRC	I	Data scan direction H= from left to right L= from right to left	Note 3-2
59	DEHS	I	DEHS=L: The DENB MODE will be selected DEHS=H: The HS + VS MODE will be selected	
60	RSTB	I	Power on reset	

Note 3-1: CSV H: Normal scan, CSV L: Reverse scan

Note 3-2: LRC H: Normal scan, LRC L: Reverse scan

Light Source

Light Source Type: CCFL Backlight

Recommend Connector Type: JST BHSR-02VS-01

3.1.1 CCFL

Pin	Symbol	Description	Remark
1	V_H	High Voltage for Backlight	Color: Pink
2	V_L	Low Voltage for Backlight	Color: White

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	MAX	Unit
Power Supply for Driver	VCC	3.0	3.6	V
Back Light Lamp Current	I_L	--	TBD	mA
Operating Temperature	Topr	-30	+85	℃
Storage Temperature	Tstg	-40	+95	℃

5. ELECTRICAL CHARACTERISTICS

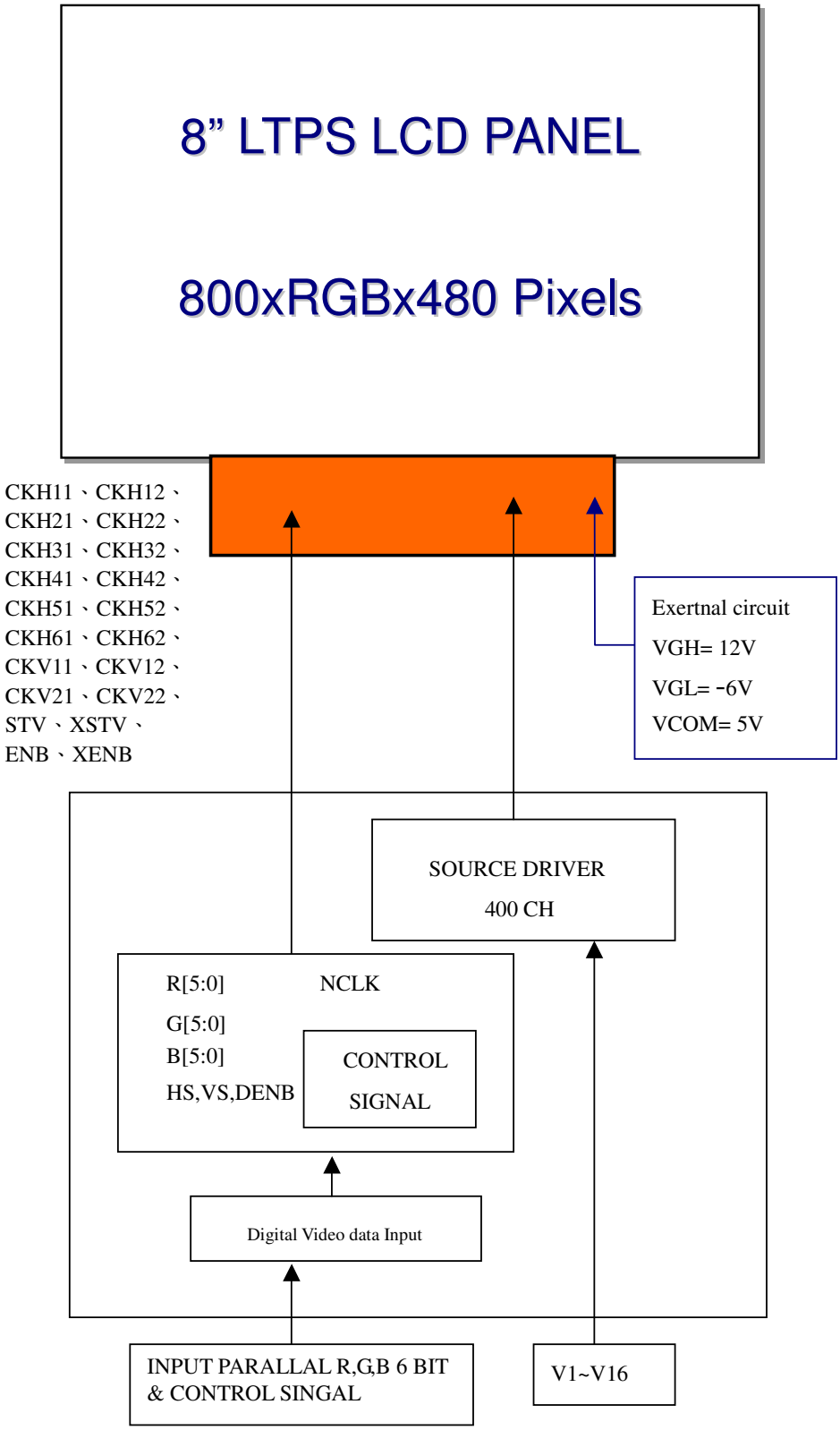
5.1 TFT LCD Module

VSS=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply for Driver	VDD	3.0	3.3	3.6	V	
Power Supply for Driver	AVDD		10	13	V	Max 13v
Power Supply for Panel	VEE	-5.4	-6	-6.6	V	
Power Supply for Panel	VVDD	11.7	12	15	V	Max 15v
Power Supply for Panel	VCOM	4.5	5.1	5.5	V	
Gamma reference voltage	V0	9.8	10	10.2	V	
Gamma reference voltage	V1	7.2	7.5	7.7	V	
Gamma reference voltage	V2	7.0	7.2	7.4	V	
Gamma reference voltage	V3	6.6	6.8	7.0	V	
Gamma reference voltage	V4	5.0	5.2	5.5	V	
Gamma reference voltage	V5	4.5	4.8	5	V	
Gamma reference voltage	V6	3	3.2	3.4	V	
Gamma reference voltage	V7	2.6	2.8	3	V	
Gamma reference voltage	V8	2.1	2.3	2.5	V	
Gamma reference voltage	V9	0.1	0.2	0.5	V	
Module Power Consumption	Wp	--	TBD		mA	Panel +ASIC IC
B/L Lamp Current	I_L	TBD	6	TBD	mA_{rms}	
B/L Lamp Voltage	V_L	--	TBD	--	V_{rms}	I_L=6mA
B/L Frequency	F_L	TBD	TBD	TBD	kHz	I_L=6mA
Kick –off Voltage	25℃ V_s	--	--	TBD	V_{rms}	at 25℃
	0℃ V_s	--	--	TBD	V_{rms}	at 0℃
	-30℃ V_s	--	--	TBD	V_{rms}	at -30℃
Backlight Power Consumption	W_{BL}	--	--	TBD	W	
Backlight Life Time	L_{BL}	--	TBD	--	hrs	Note 5-1

Note 5-1: Backlight luminance is not less than 50% of initial value at I_L=6mA.

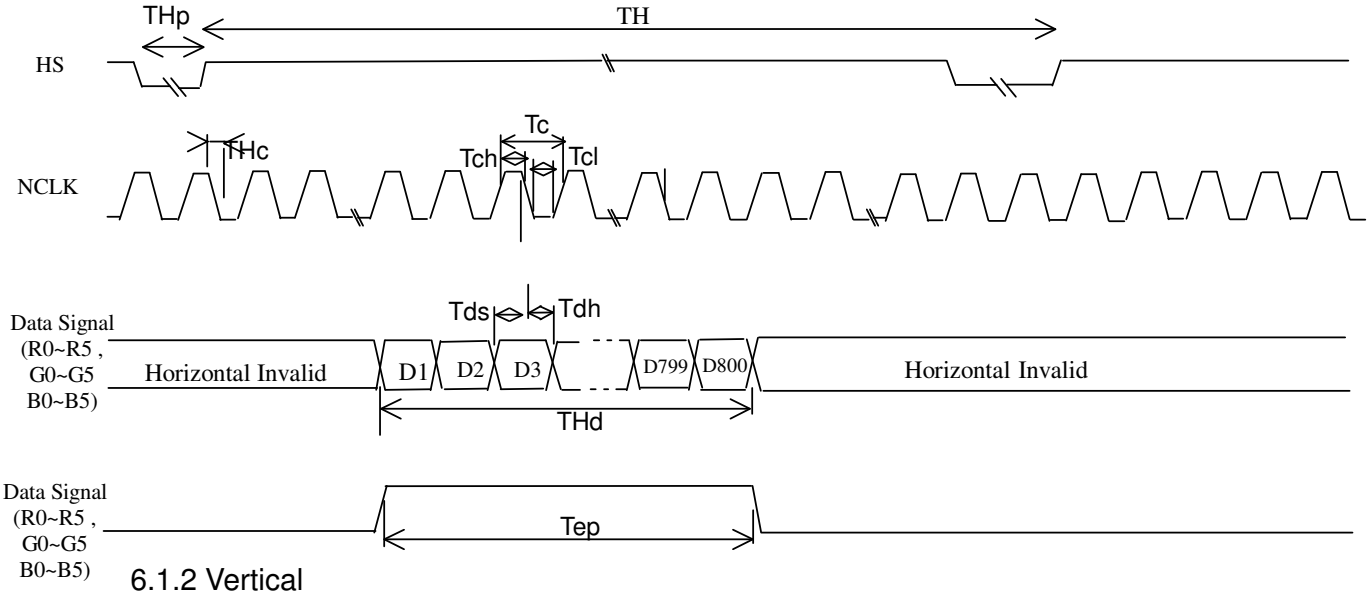
5.2 TFT LCD Module Block Diagram



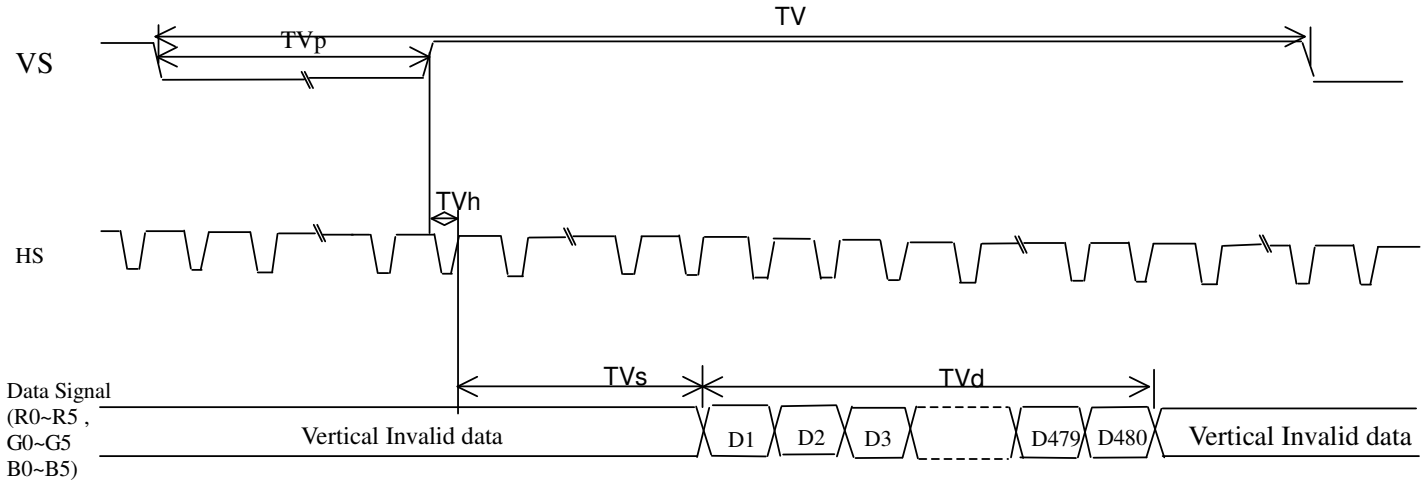
6. TIMING CHART

6.1 Timing Chart

6.1.1 Horizontal

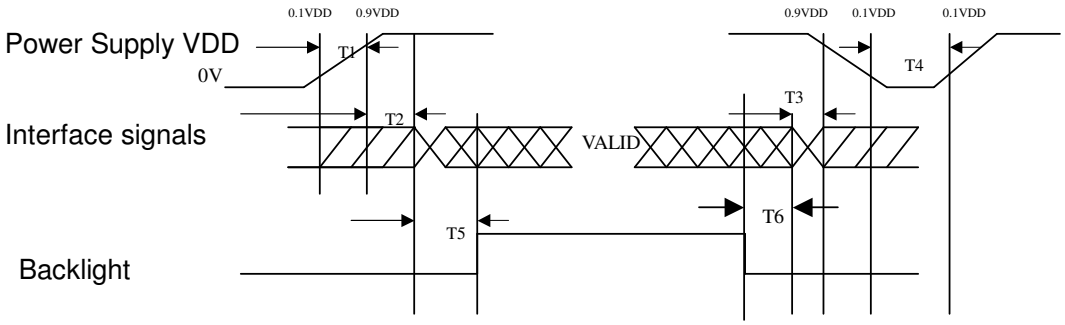


6.1.2 Vertical



6.2 Power ON/OFF Sequence

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



T1≦10ms 0≦T2≦50ms 0≦T3≦50ms 400ms≦T4 200ms≦T5 100ms≦T6

T1:VDD rising time from 0.1VDD to 0.9VDD.

T2:The time from 0.9VDD to valid data at power ON.

T3:The time from 0.9VDD to valid data at power OFF.

T4:VDD off time for window restarts.

T5:The time from valid data to B/L enable at POWER ON.

T6 The time from valid data to B/L enable at POWER OFF

6.3 Timing Characteristics

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
Clock(NCLK)	Frequency	1/Tc	--	33.2	36.2	MHz	Tc=tnclk
	High Time	Tch	5	--	--	ns	
	Low Time	Tcl	5	--	--	ns	
Data	Setup Time	Tds	3	--	--	ns	
	Hold Time	Tdh	10	--	--	ns	
Horizontal sync. Signal	Cycle	TH		31.8	--	us	
				1056		clock	
	Pulse Width	THp	1	128		clock	
Vertical sync. Signal	Cycle	TV		525		line	
	Pulse Width	TVp	1	4		line	
Horizontal display period		THd		800		clock	
Hsync-Clock phase difference		THc	10	--	Tc-10	ns	
Hsync-Vsync phase difference		TVh	0	--	TH-THp	ns	
Vertical display start position		TVs		33		line	
Vertical display period		TVd		480		line	
Enable signal	Setup time	Tes	5	--	Tc-10	ns	
	Pulse width	Tep	2	800	TH-10	clock	

7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

Ta=25℃

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angle		Θ11	CR ≥ 10	60	70	--	Degree	Note 7-1
		Θ12		60	70	--		
		Θ21		60	70	--		
		Θ22		40	50	--		
Contrast Ratio		CR	Θ=0°	400	500	--		Note 7-2
Response Time	Rising	Tr			4.5	TBD	ms	Note 7-3
	Falling	Tf			7.5	TBD		
Luminance (I_L=6mA)		L		400	500	--	cd//m^2	Note 7-4
Chromaticity	White	x_W		0.28	0.31	0.34		Note 7-5
		y_W		0.30	0.33	0.36		
NTSC Ratio		NTSC		--	50	--	%	Note 7-6

7.2 Basic Measure Conditions

7.2.1 Driving voltage

VDD= 3.3V

7.2.2 Ambient Temperature: Ta=25℃

7.2.3 Testing Point: Measure in the display center point and the test angle Θ=0°

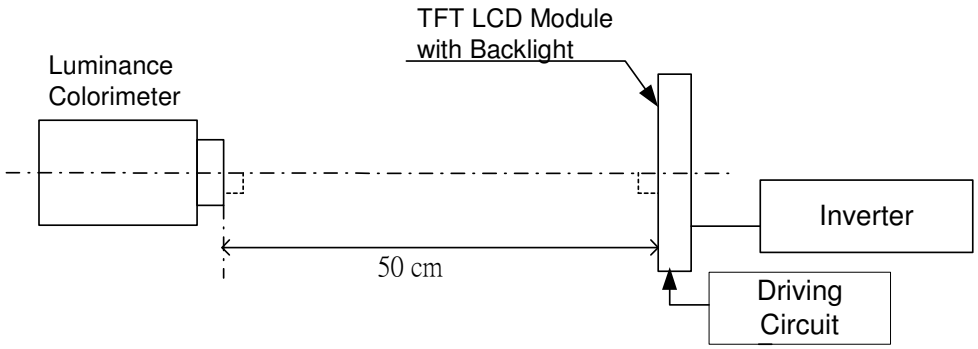
7.2.4 The Luminance measurement is based on using Harison HIU757 inverter

7.2.5 Measurement System

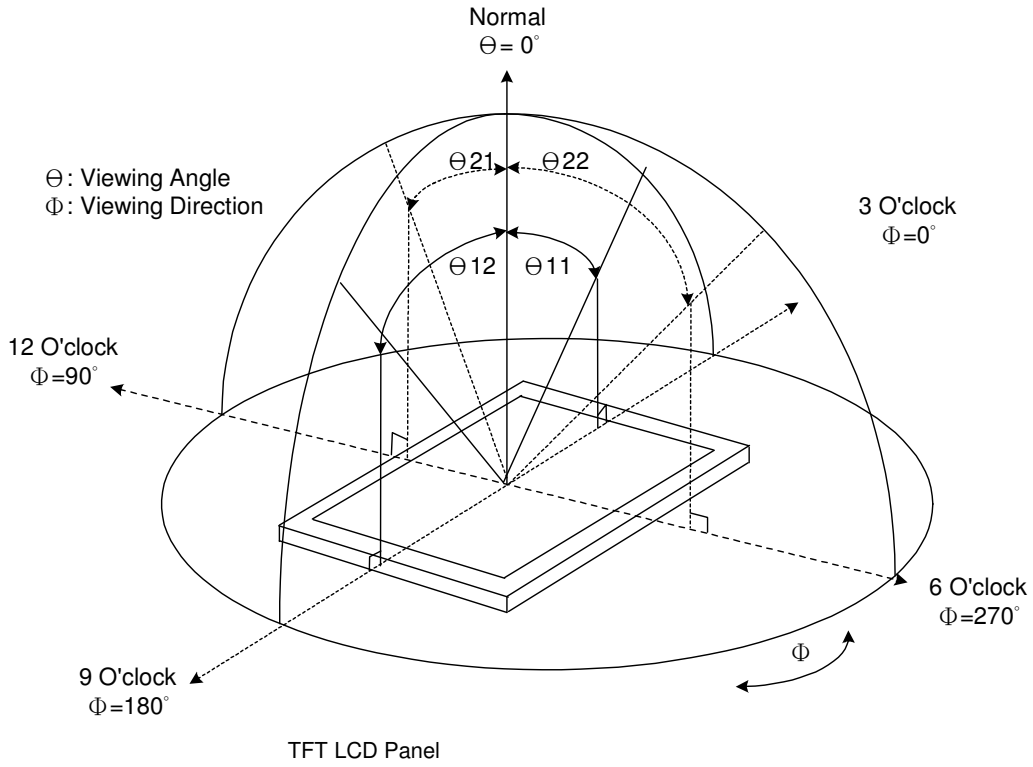
A. Environmental illumination: ≤ 1 Lux

B. Using the TOPCON BM-5A luminance meter

C. Using the Harison HIU 757 inverter



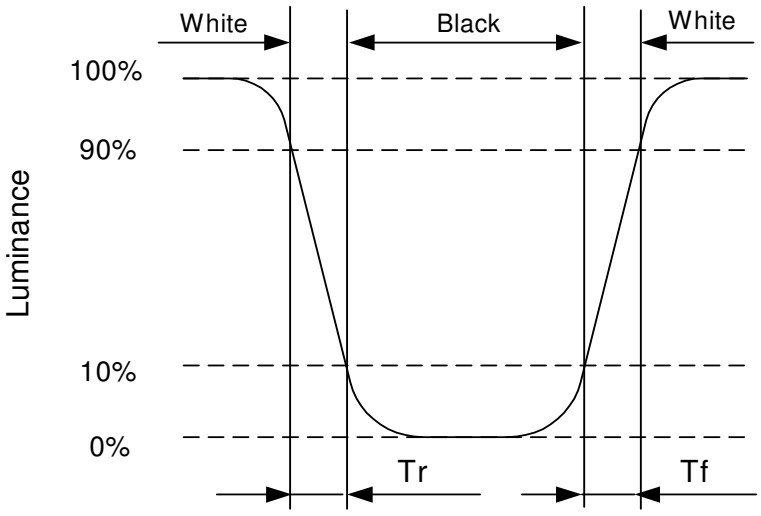
Note 7-1: Viewing angle diagrams:



Note 7-2: Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time:



Note 7-4: Luminance:

L = White luminance at the center of the panel

Note 7-5: Chromaticity: The same test condition as Note 7-4.

Note 7-6: Measure Chromaticity of full on color R,G,B at center of the panel.

8. REILIABILITY

No	Test Item	Condition
1	High Temperature Operation	Tp=+85℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+60℃, 90% RH, 240hrs
3	Low Temperature Operation	Ta=-30℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+95℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta=-40℃, 240hrs
6	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH, 240hrs
7	Thermal Shock (non-operation)	Test between -40℃(duration 30 min.) and 85℃(duration 30 min.), 168 cycles
8	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0Ω; Discharge: ±150V 3 times / Terminal
9	Surface Discharge (non-operation)	C=150pF, R=330Ω; Discharge: Air: ±15kV; Contact: ±15kV 5 times / Point; 5 Points / Panel
10	Vibration (non-operation)	Frequency range: 10-55 Hz±0.75mm Sinusoidal 55-2000 Hz Acceleration: 10G Sweep Time: 1 Oct./mim X/Y/Z 2 hrs for etch directions
11	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Twice Waveform: half-sine

Tp: Panel Temperature

Ta: Ambient Temperature

9. HANDLING CAUTIONS

9.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

9.1.1 In handling LCD panel, please wear non-charged material gloves. Connect the wrist conduction ring to the earth and the conducting shoes to the earth are necessary.

9.1.2 The machine and working table for the panel should have ESD protection strategy.

9.1.3 In handling the panel, using ionized air to decrease the charge in the environment is necessary.

9.1.4 In the process of assembly the module, shield case should connect to the ground.

9.2 Environment

9.2.1 Working environment of the panel should be in the clean room.

9.2.2 The front polarizer is easy to be damaged. Handle it carefully and do not scratch it by sharp material.

9.2.3 Panel has polarizer protective film in the surface. Please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

9.3.1 Turn off the power supply before connecting and disconnecting signal input cable.

9.3.2 The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

9.3.3 Water drop on the surface or condensation as panel power on will corrode panel electrode.

9.3.4 As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

9.3.5 When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

10. MECHANICAL DRAWING