High-Performance, Low-Current SIGFOX™ Gateway

GENERAL DESCRIPTION

Telecom Design's TD1207R/08R devices are high performance, low current SIGFOX™ gateways. The combination of a powerful radio transceiver and a state-of-the-art ARM Cortex M3 baseband processor achieves extremely high performance while maintaining ultra-low active and standby current consumption. The TD1207R/08R device offers an outstanding RF sensitivity of –126 dBm while providing an exceptional output power of up to +16 dBm with unmatched TX efficiency. The TD1207R/08R device versatility provides the gateway function from a local Narrow Band ISM network to the long-distance Ultra Narrow Band SIGFOX™ network at no additional cost. The broad range of analog and digital interfaces available in the TD1207R/08R module allows any application to interconnect easily to the SIGFOX™ network. The LVTTL low-energy UART, the I2C bus, the multiple timers with pulse count input / PWM output capabilities, the high-resolution / high-speed ADC and DAC, along with the numerous GPIOs can control any kind of external sensors or activators. Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way.

BOARD FEATURES

- 2.3V to 3.3V Power supply
- 1.8 µA sleep mode consumption
- LGA25 (25.4×12.7×3.81mm) Land Grid Array package with castellated pads
- High CAF Resistance

KEY FEATURES

- SIGFOX™ transceiver certified
- 145 dB maximum link budget
- (G)FSK, 4(G)FSK, GMSK, OOK modulation
- Receive sensitivity =-126 dBm
- +16 dBm maximum output power
- Frequency range = ISM 868 MHz
- Low active radio power consumption (3.3V)
  - 13/16 mA RX
  - 32mA Tx @ +10 dBm
  - 41mA Tx @ +14 dBm
  - 51mA Tx @ +16 dBm
-

APPLICATIONS

- SIGFOX™ transceiver (fully certified)
- Sensor network
- Health monitors
- Remote control
- Home security and alarm
- Telemetry
- Industrial control

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1.1 Simplified Block Diagram

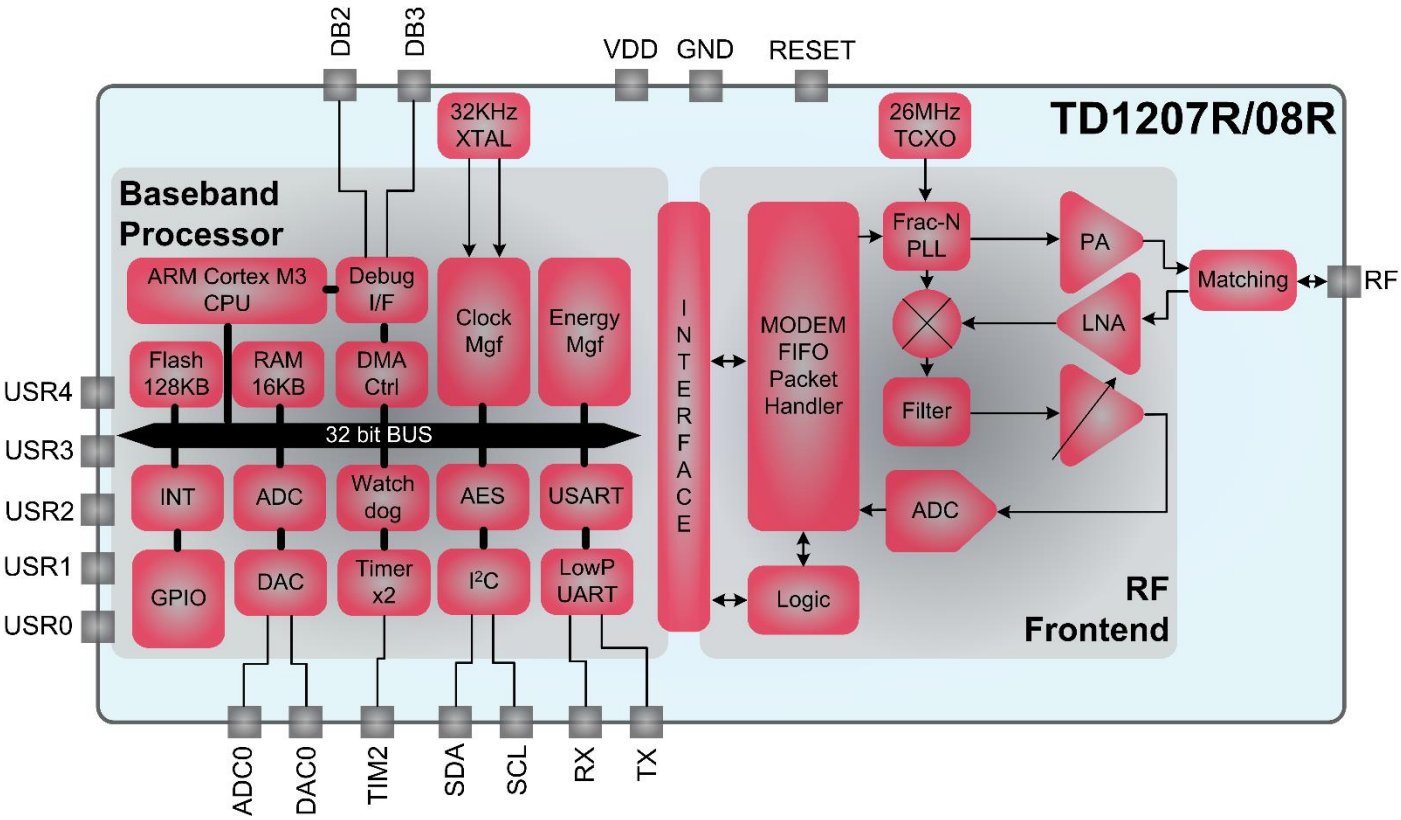


Figure 1. TD1207R/08R block diagram

1.2 Product Versions

The features of the two product variants TD1207R and TD1208R are detailed in the following table

Table 1. TD1207R/08R device variants

Part Number	Description	Package Type	Operating Temperature
TD1207R	ISM SIGFOX™ gateway 128K Flash/ 16K RAM / TCXO, with fixed AT command set	LGA25 Pb-free	-30° to +75°C
TD1208R	ISM SIGFOX™ gateway 128K Flash/ 16K RAM / TCXO, with fixed AT command set, user customizable firmware	LGA25 Pb-free	-30° to +75°C

1.3 Pin Diagram

The following diagram shows the pin arrangement of the LGA package.

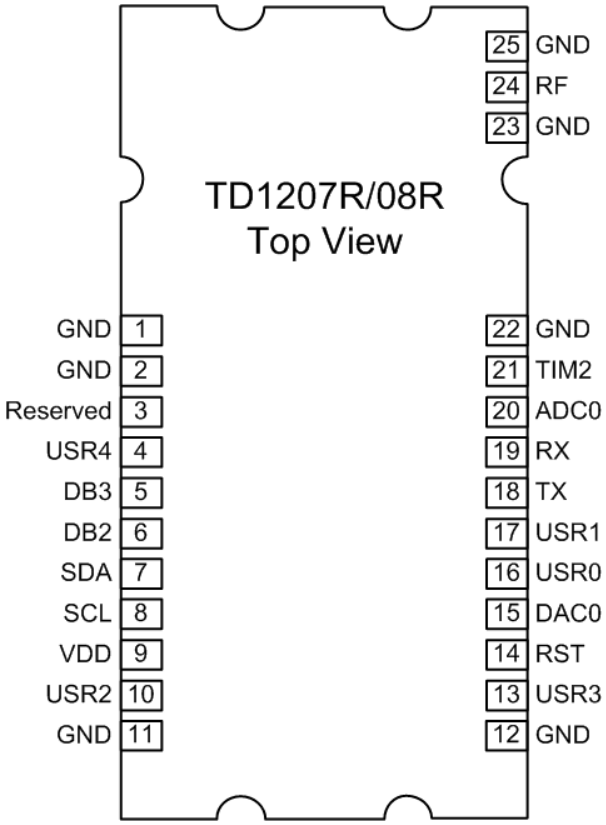


Figure 2. TD1207R/08R pin diagram

1.4 Pin Description

Table 2. Pin definition

Pin number	Signal Name	Pin Type	Principal function	Remarks	MCU pin name
1	GND	GND	Ground		-
2	GND	GND	Ground		-
3	Reserved	NC	Reserved	Do not connect	-
4	USR4	I/O	General Purpose I/O 4	See note 1	PC14
5	DB3	I	Serial Debug SWDCLK (SWD Clock) Signal	See note 1	PF0
6	DB2	I/O	Serial Debug SWDIO (SWD Data I/O) Signal	See note 1	PF1
7	SDA	I/O	Master Slave I^2C serial data	See note 1	PA0
8	SCL	I/O	Master Slave I^2C serial clock	See note 1	PA1
9	VDD	VDD	Power supply voltage	Connect a 10 µF capacitor as close as possible to this input	-
10	USR2	I/O	General Purpose I/O 2	See note 1	PC0
11	GND	GND	Ground		-
12	GND	GND	Ground		-
13	USR3	I/O	General Purpose I/O 3	See note 1	PC1
14	RST	I	Active Low RESET input signal	internally pulled up, can be left floating if not used	-
15	DAC0	I/O	DAC analog output #0	See note 1	PB11
16	USR0	I/O	General Purpose I/O 0	See note 1	PB13
17	USR1	I/O	General Purpose I/O 1	See note 1	PC15
18	TX	O	Low-Power UART Data Transmit data	internally pulled up, See note 1	PD4
19	RX	I	Low-Power UART Data Receive data	internally pulled up, See note 1	PD5
20	ADC0	I/O	ADC analog input #6	See note 1	PD6
21	TIM2	I/O	I/O Timer compare #2 function	See note 1	PD7
22	GND	GND	Ground		-
23	GND	GND	Ground		-
24	RF	I/O	Input / Output 50Ω RF signal		-
25	GND	GND	Ground		-

Notes:

1. *This pin may be configured to perform various functions. To obtain a list of the possible alternate functionalities, please refer to the EFM32G210 datasheet.*

1.5 Package Marking

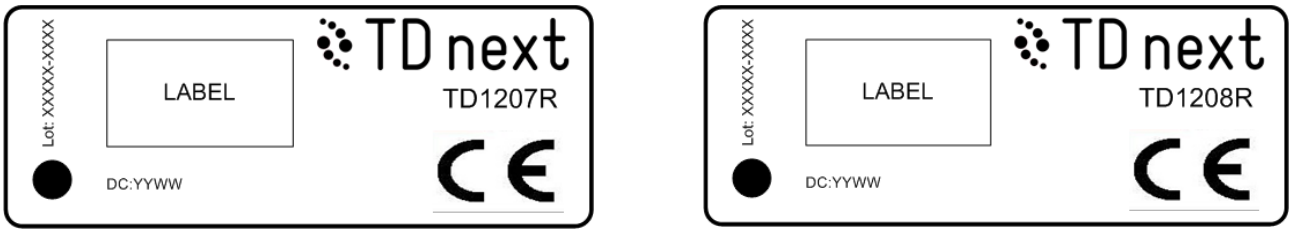


Figure 3. Package marking

Lot : XXXXX-XXXX : TD Next Lot No

DC : YYWW : Date code

Label : Label with QR code and SIGFOX™ ID

1.6 Definition of Test Conditions

1.6.1 Production Test Conditions:

- T_A = + 25°C
- V_{DD} = +3.3 VDC
- Production test schematics (unless noted otherwise)
- All RF input and output levels referred to the pins of the TD1207R/08R module

1.6.2 Qualification Test Conditions:

- T_A = -30 to +75°C (Typical T_A = 25°C)
- V_{DD} = +2.3 to 3.6 VDC (Typical V_{DD} = 3.3 VDC)
- Using TX/RX Split Antenna reference design or production test schematic
- All RF input and output levels referred to the pins of the TD1207R/08R module

2 Electrical Specifications

2.1 ESD Notice

TD1207R/08R modules are ESD sensitive devices, appropriate precautions should be taken during TD1207R/08R assembly in the final product. Mechanical impact and harsh tools must be avoided during TD1207R/08R assembly in the final product.

2.2 Absolute Maximum Rating

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX VRF-peak on RF pin. Caution: ESD sensitive device.

Table 3. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage	0	3.6	V
$V_{IRF\ peak}$	Instantaneous RF Peak	-0.3	8	V
$V_{SRF\ peak}$	Sustained RF Peak	-0.3	6.5	V
V_{DIN}	Voltage on Digital Inputs	0	V_{DD}	V
V_{AIN}	Voltage on Analog Inputs	0	V_{DD}	V
P_{IN_ISM}	RX Input Power	-	+10	dBm
T_A	Operating Ambient Temperature Range	-30	+75	°C
T_{STG}	Storage Temperature Range	-40	+125	°C
T_{SOL}	Maximum soldering Temperature	-	260	°C

2.3 DC Power characteristics

Table 4. DC Power Supply Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range[2]		2.3	3.3	3.6	V
I_{Sleep}	Power Saving Mode[2]	Sleep current using the 32 kHz crystal	1.5	1.8	3.5	µA
I_{Active}	Active CPU Mode	CPU performing active loop @ 14 MHz	2.55	3.0	3.45	mA
I_{RX}	Active CPU Mode + RX Mode Current[2]		-	13	16	mA
I_{TX_+16}	Active CPU Mode + TX Mode Current[2]	+16 dBm output power, 868 MHz	-	50	-	mA
I_{TX_+14}		+14 dBm output power, 868 MHz	-	41	-	mA
I_{TX_+10}		+10 dBm output power, 868 MHz	-	32	-	mA

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*

2.4 RF Power characteristics

2.4.1 Transmitter RF Characteristics

The table below give TX RF performance of TD1207R/08R. It is the responsibility of the user to respect ETSI standard requirement, especially about maximum authorized radiated output power.

Table 5. Transmitter RF Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TX}	TX Frequency Range[2]		868.0	-	869.7	MHz
Δf	Modulation Deviation Range[3]	868.0-869.7 MHz	-	1.5	-	MHz
F_{RES}	Modulation Deviation Resolution[3]	868.0-869.7 MHz	-	24.8	-	Hz
F_{ERR}	Frequency Error[2]	868.0-869.7 MHz, -20°C 868.0-869.7 MHz, 25°C 868.0-869.7 MHz, 55°C	-3 -2 -3	- - -	+3 +2 +3	kHz
P_{TX}	Maximum Conducted power	V_{DD} = 3.6 V, I = 52 mA V_{DD} = 3.3 V, I = 51 mA V_{DD} = 3 V, I = 50 mA V_{DD} = 2.8 V, I = 49 mA V_{DD} = 2.3 V, I = 45 mA	- - - - -	16.5 15.9 15.2 14.8 13.2	- - - - -	dBm
P_{TP}	Transient Power[2]	868.0-869.7 MHz, 25°C, BR=4.8kbps, FD=2.5kHz, cable loss 0.2 dB, antenna gain 2 dBi	-	-	3	dBm
P_{ACP}	Adjacent Channel Rejection[2]	BR=4.8kbps, FD=2.5kHz, 2dBi Offset=+/-25kHz	-	-57	-	dB
P_{OB_TX}	Spurious Emissions[2]	868.0-869.7 MHz, 25°C, BR 4.8kbps, dev 2.5kHz, 2dBi <30MHz <1GHz >1GHz	- - -	-80 -70 -42	- - -	dBm

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
3. *Guaranteed by component specification.*

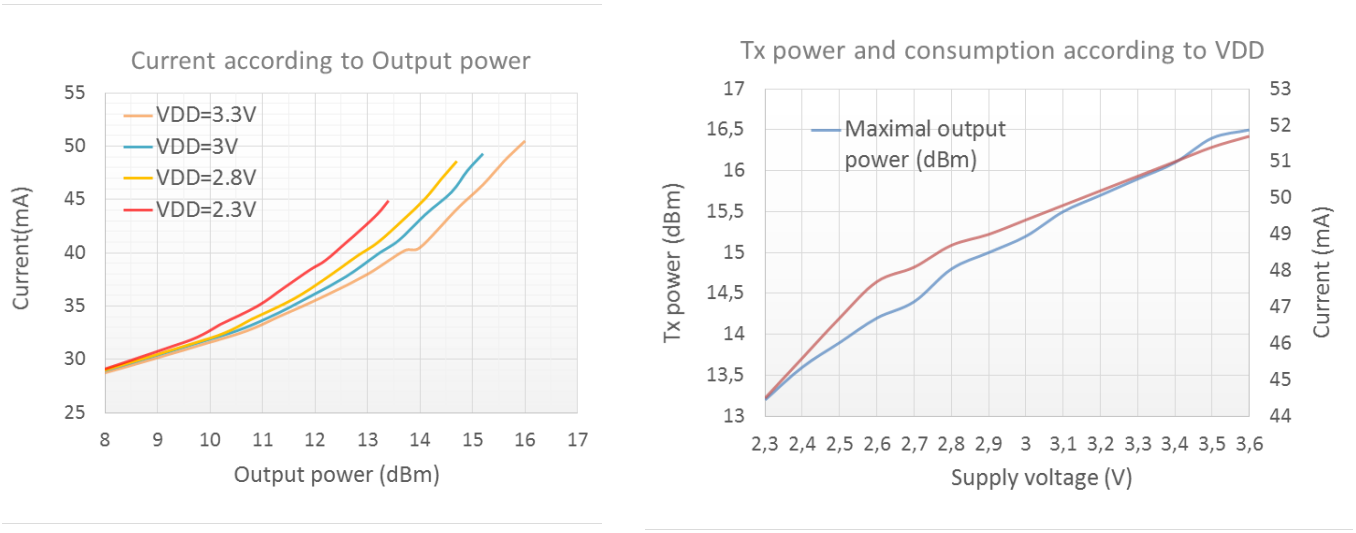


Figure 4. TD1207R/08R Tx performances

2.4.2 Receiver RF Characteristics

Table 6. Receiver RF Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{RX}	RX Frequency Range[2]		868.0	-	869.7	MHz
F_{RES}	Synthesizer Frequency Resolution[3]	868.0-869.7 MHz	-	24.8	-	Hz
BI	Blocking[2,4]	Offset=+/-2MHz Offset=+/-10MHz	-	67 79	-	dB
P_{OB_RX}	Spurious Emissions[2]	From 9 kHz to 1 GHz From 1 GHz to 6 GHz	-	-84 -70	-	dBm
P_{RX}	GFSK RX Sensitivity[3] BER<0.1%, BT=0.5	FDA=0.25 kHz, BR=0.5 kbps FDA=9.6 kHz, BR=2.4 kbps FDA=20 kHz, BR=40 kbps FDA=50 kHz, BR=100 kbps FDA=62.5 kHz, BR=125 kbps FDA=250 kHz, BR=500 kbps FDA=1.25 kHz, BR=1 Mbps	-	-126 -110 -110 -106 -105 -97 -88	-	dBm
P_{RX_OOK}	OOK RX Sensitivity[3] BER<0.1%, BT=0.5, PN15 data	BW=350kHz, BR=4.8kbps BW=350kHz, BR=40kbps BW=350kHz, BR=120kbps	-	-109 -104 -99	-	dBm
RES_{RSSI}	RSSI Resolution[3]		-0.5	-	+0.5	dB

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
3. *Guaranteed by component specification.*
4. *The typical blocking values were obtained while seeking for EN 300-220 Category 2 compliance only. The typical value specified in the component datasheet are -75 dB and -84 dB at 1 and 8 MHz respectively, with desired reference signal 3 dB above sensitivity, BER = 0.1%, interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz. The RF component manufacturer provides a reference design featuring a SAW filter which is EN 300-220 Category 1 compliant. Please contact Telecom Design for more information on EN 300-220 Category 1 compliance.*

2.5 Digital characteristics

Table 7. All Digital I/O DC & AC Characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IOIL}	Input Low Voltage[2]		-	-	$0.3V_{DD}$	V
V_{IOIH}	Input High Voltage[2]		$0.7V_{DD}$	-	-	V
V_{IOOH}	Output High Voltage[2] VDD=3.0V	6 mA, Std Drive Strength 20 mA, High Drive Strength	$0.95V_{DD}$ $0.9V_{DD}$	- -	- -	V
V_{IOOL}	Output Low Voltage[2] VDD=3.0V	6 mA, Std Drive Strength 20 mA, High Drive Strength	-	-	$0.05V_{DD}$ $0.1V_{DD}$	V
I_{IOLEAK}	Input Leakage Current[2]	High Impedance I/O connected to GND or V_{DD}	-25	-	+25	nA
R_{PU}	I/O Pin Pull-Up Resistor[2]		-	40	-	kΩ
R_{PD}	I/O Pin Pull-Down Resistor[2]		-	40	-	kΩ
R_{IOESD}	Internal ESD Series Resistor[2]		-	200	-	Ω
$t_{IOGLITCH}$	Pulse Width of Pulses to be Removed by the Glitch Suppression Filter[2]		10	-	50	ns
t_{IOOF}	Output Fall Time[2]	0.5 mA / C_L = 12.5 to 25 pF 2 mA / C_L = 350 to 600 pF	$20+0.1C_L$ $20+0.1C_L$	-	250 250	ns
V_{IOHYST}	I/O Pin Hysteresis (V_{IOTHR+} - V_{IOTHR-})[2]	V_{DD} = 2.3 to 3.3 V	$0.1V_{DD}$	-	-	V

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by component specification.*

2.6 ADC and DAC characteristics

2.6.1 ADC Characteristics

Table 8. ADC DC & AC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADCIN}	Input Voltage Range[2]	Single Ended mode Differential mode	0 -V_{REF}/2	- -	V_{REF} V_{REF}/2	V
$V_{ADCCMIN}$	Common Mode Input Range[2]		0	-	V_{DD}	V
I_{ADCIN}	Input Current[2]	2 pF Sampling Capacitors	-	100	-	nA
$CMRR_{ADC}$	Analog Input CMRR[2]		-	65	-	dB
I_{ADC}	Average Active Current[2]	10ksps/s, 12 bit, Internal 1.25V ref Warmup Mode = 0 Warmup Mode = 1 Warmup Mode = 2	 - - -	 67 63 64	 - - -	µA
I_{ADCREF}	Current Consumption of Internal Voltage Reference[2]		-	65	-	µA
C_{ADCIN}	Input Capacitance[2]		-	2	-	pF
R_{ADCIN}	Input ON Resistance[2]		1	-	-	MΩ
$R_{ADCFILT}$	Input RC Filter Resistance[2]		-	10	-	kΩ
$C_{ADCFILT}$	Input RC Filter/Decoupling Capacitance[2]		-	250	-	fF
f_{ADCCLK}	ADC Clock Frequency[2]		-	-	13	MHz
$t_{ADCCONV}$	Conversion Time[2]	6 bit 10 bit 12 bit	7 11 13	- - -	- - -	ADC CLK Cycles
t_{ADCACQ}	Acquisition Time[2]	Programmable	1	-	256	ADC CLK Cycles
$t_{ADCACQVDD3}$	Required Acquisition Time for V_{DD}/3 Reference[2]		2	-	-	µs
$t_{ADCSTART}$	Startup Time of Reference Generator and ADC Core	NORMAL Mode[2] KEEPADCWARM Mode[2]	- -	5 1	- -	µs
$V_{ADCOFFSET}$	Offset Voltage after calibration[2]	single ended mode differential mode	- -	0.3 0.3	- -	mV
$TGRAD_{ADCTH}$	Thermometer Output Gradient[2]	In mV/°C unit In ADC Codes/ °C unit	-	-1.92 -6.3	-	mV/°C C/°C
DNL_{ADC}	Differential Non-Linearity (DNL) [2]		-0.7		+0.7	LSB
INL_{ADC}	Integral Non-Linearity (INL)[2]	End Point Method	-1.2		+0.2	LSB
MC_{ADC}	No Missing Codes[2]		11.999[3]	12	-	bits
$GAIN_{ED}$	Gain Error Drift[2]	1.25V Reference 2.25V Reference	- -	0.01[4] 0.01[4]	0.033[5] 0.03[5]	%/°C
		1.25V Reference 2.25V Reference	0.07[5] -	0.2[4] 0.2[4]	- 0.62[5]	LSB/°C

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by component specification.*
3. *On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the*

missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbor codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

4. *Typical numbers given by abs(Mean) / (85 - 25).*
5. *Max number given by (abs(Mean) + 3x stddev) / (85 - 25).*

2.6.2 DAC Characteristics

Table 9. DAC DC & AC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DACOUT}	Output Voltage Range[2]	V_{DD} voltage reference, Single Ended	0	-	V_{DD}	V
V_{DACCM}	Output Common Mode Voltage Range[2]		0	-	V_{DD}	V
I_{DAC}	Active Current Including References for 2 Channels [2]	500 ksps/s 12 bit 500 ksps/s 12 bit 100 ksps/s 12 bit NORMAL	- - -	400 200 38	- - -	µA
SR_{DAC}	Sample Rate[2]		-	-	500	ksps
f_{DAC}	DAC Clock Frequency[2]	Continuous Mode Sample/Hold Mode Sample/Off Mode	- - -	- - -	1000 250 250	kHz
$CYC_{DACCONV}$	Clock Cycles per Conversion [2]		-	2	-	DAC CLK Cycles
$t_{DACCONV}$	Conversion Time[2]		2	-	-	µs
$t_{DACSETTLE}$	Settling Time[2]		-	5	-	µs
SNR_{DAC}	Signal to Noise Ratio (SNR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	 - -	 58 59	 - -	dB
$SNDR_{DAC}$	Signal to Noise-Pulse Distortion Ratio (SNDR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	 - -	 57 54	 - -	dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	 - -	 62 56	 - -	dB
$V_{DACOFFSET}$	Offset Voltage after calibration[2]	single ended mode	-	2	-	mV
DNL_{DAC}	Differential Non-Linearity[2]		-1	-	+1	LSB
INL_{DAC}	Integral Non-Linearity[2]		-5	-	5	LSB
MC_{DAC}	No Missing Codes[2]		-	12	-	bits

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.6 Definition of Test Conditions" on page 8.*
2. *Guaranteed by component specification.*

3 Functional Description

The TD1207R/08R devices are high-performance, low-current, wireless SIGFOX™ gateways. The wide operating voltage range of 2.3–3.3 V and low current consumption make the TD1207R/08R an ideal solution for battery powered applications. The TD1207R/08R operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2-level FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the baseband CPU by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 0.123 kbps to 1 Mbps. The TD1207R/08R operates in the frequency bands of 868.0–869.7 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The power amplifier (PA) supports output power up to +14 dBm with very high efficiency, consuming only 37 mA at +10 dBm. The integrated power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure.

As both the local Narrow Band ISM network and the long-distance Ultra Narrow Band SIGFOX™ network can be addressed seamlessly, the TD1207R/08R device provides a natural gateway function at no additional cost. Thus, the same TD1207R/08R module can be used both for local RF communication with peer modules, and also connect to the wide-area SIGFOX™ RF network.

The broad range of analog and digital interfaces available in the TD1207R/08R module allows any application to interconnect easily to the SIGFOX™ network. The LVTTL low-energy UART, the I^2C bus, the multiple timers with pulse count input / PWM output capabilities, the high-resolution/high-speed ADC and DAC, along with the numerous GPIOs can control any kind of external sensors or activators. Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. This unique combination of a powerful 32-bit ARM Cortex-M3 CPU including innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of intelligent peripherals allows any application to connect to the SIGFOX™ network.

The application shown in **Figure 5** shows the minimum interconnection required to operate the TD1207R/08R module.

Basically, only the 5 GND, 2 RF_GND, V_{DD}, TX, RX and RF antenna pin connections are necessary. The RST (reset) pin connection is not mandatory and this pin can be left floating if not used.

A 10 µF/6.3V decoupling capacitor must be added as close as possible to the V_{DD} pin.
The TX/RX pins are LVTTL-compatible and feature internal pull-up resistors.

A 50 Ω matched RF antenna must be connected to the RF pin, with a low-capacitance (< 0.5 pF) TVS diode to protect the RF input from ESD transients.

The connection of a super-blue LED with series current-limiting resistor of 220 Ω on pin TIM2 is recommended in order to display the bootloader status at boot time.

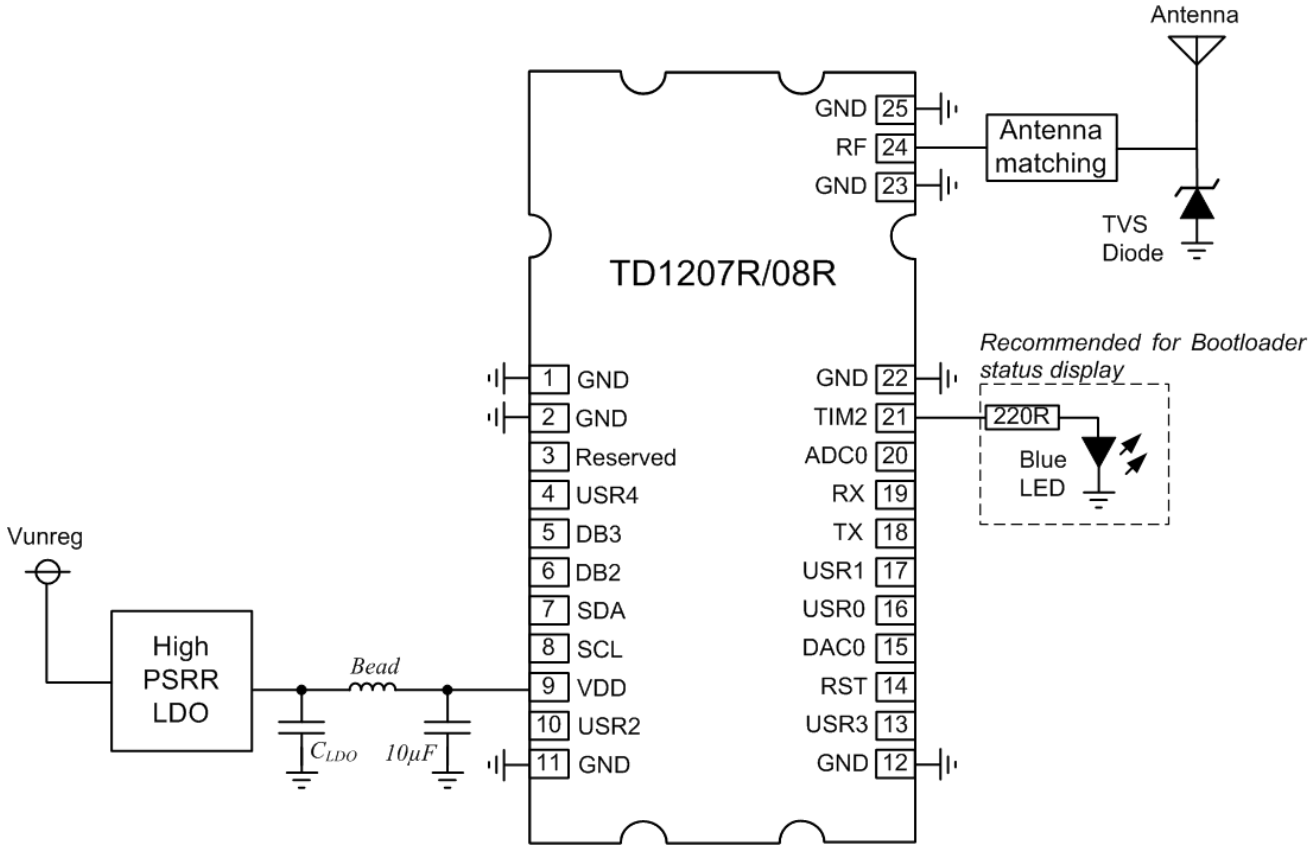


Figure 5. Typical Application

Note:

The TVS diode used for protecting the RF input against ESD must be of low-capacitance (0.5 pF typical) type, e.g. ESD9R3.3ST5G (On Semiconductor), for example.

4 Module Interface

4.1 Low-Power UART (Universal Asynchronous Receiver/Transmitter)

The TD1207R/08R communicates with the host MCU over a standard asynchronous serial interface consisting of only 2 pins: TX and RX. The TX pin is used to send data from the TD1207R/08R module to the host MCU, and the RX pin is used to receive data into the TD1207R/08R module coming from the host MCU.

This interface allows two-way UART communication to be performed in low energy modes, using only a few µA during active communication and only 150 nA when waiting for incoming data.

This serial interface is designed to operate using the following serial protocol parameters:

- LVTTL electrical level
- 9600 bps
- 8 data bits
- 1 stop bit
- No parity
- No hardware/software flow control
-

This interface operates using LVTTL signal levels to satisfy the common interface to a low power host MCU. If an EIA RS232-compliant interface voltage level is required, an RS232 level translator circuit must be used. It is also possible to use a common USB/UART interface chip to connect to an USB bus.

Over this serial interface, the TD1207R/08R device provides a standard Hayes "AT" command set used to control the module using ASCII readable commands and get answers, as well as to send or receive data.

The list of available commands with their corresponding arguments and return values, a description of their operation and some examples are detailed into the "*TD1207R/08R Reference Manual*".

4.2 I²C bus

As a convenience, the TD1207R/08R module is equipped with a popular I²C serial bus controller that enables communication with a number of external devices using only two I/O pins: SCL and SDA. The SCL pin is used to interface with the I²C clock signal, and the SDA pin to the I²C data signal, respectively. When not used for I2C bus, these 2 pins can be configured to perform other functions using "AT" configuration commands, please refer to the "*TD1207R/08R Reference Manual*" for details.
The TD1207R/08R module is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode (Sm), fast-mode (Fm) and fast-mode plus (Fm+) speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. Both 7-bit and 10-bit addresses are supported, along with extensive error handling capabilities (clock low/high timeouts, arbitration lost, bus error detection).
The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TD1207R/08R Reference Manual*".

4.3 Timer/Counter

The TD1207R/08R provides an interface to an integrated timer/counter using the TIM2 pin. This pin can be configured as either a capture input or a compare/PWM output to the 16-bit internal timer/counter. When not used for timer/counter operation, this pin can be configured to perform other functions using "AT" configuration commands, please refer to the "*TD1207R/08R Reference Manual*" for details.
The timer consists in a counter that can be configured to up-count, down-count, up/down-count (continuous or one-shot).

The timer also contains 2 output channels, that can be configured as either an output compare or single/double slope PWM (Pulse-Width Modulation) outputs routed to the TIM2 pin.
The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TD1207R/08R Reference Manual*".

4.4 ADC (Analog to Digital Converter)

The TD1207R/08R provides an interface to an integrated low-power SAR (Successive Approximation Register) ADC, capable of a resolution of up to 12 bits at up to 1 Msps or 6 bits at up to 1.86 Msps. The ADC0 pin provides the external interface to the ADC. When not used for ADC operation, this pin can be configured to perform other functions using "AT" configuration commands, please refer to the "*TD1207R/08R Reference Manual*" for details.
Along with the ADC0 analog input channel, the ADC also provides an internal temperature, VDD, and GND input channel that may be used to get a digital representation of analog temperature or voltage values. It is also possible to loopback the analog output of the integrated DAC (see section 4.5, "DAC (Digital to Analog Converter)").
The internal ADC provides an optional input filter consisting of an internal low-pass RC filter or simple internal decoupling capacitor. The resistance and capacitance values are given in the electrical characteristics for the device, named $R_{ADCFILT}$ and $C_{ADCFILT}$ respectively.
The reference voltage used by the ADC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, V_{DD}, a 5 V internal differential bandgap or unbuffered $2V_{DD}$.
Additionally, to achieve higher accuracy, hardware oversampling can be enabled. With oversampling, each selected input is sampled a number of times, and the results are filtered by a first order accumulate and dump filter to form the end result. Using 16x oversampling minimum, it is thus possible to achieve result resolution of upt to 16 bits.
The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "TD1207R/08R Reference Manual".

4.5 DAC (Digital to Analog Converter)

The TD1207R/08R provides an interface to an integrated DAC that can convert a digital value to a fully rail-to-rail analog output voltage with 12-bit resolution at up to 500 ksps. The DAC may be used for a number of different applications such as sensor interfaces or sound output. The analog DAC output is routed to the DAC0 pin. When not used for ADC operation, this pin can be configured to perform other functions using "AT" configuration commands, please refer to the "TD1207R/08R Reference Manual" for details.
The reference voltage used by the DAC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, or V_{DD}.
The internal DAC provides support for offset and gain calibration, and contains an automatic sine generation mode as well as a loopback output to the ADC (see section 4.4, "ADC (Analog to Digital Converter)").

4.6 GPIO (General Purpose Input/Output)

Apart from the TX and RX UART pins, and the RF pins, all signal pins are available as general-purpose inputs/outputs. This includes of course the generic USR0, USR1, USR2, US3 and USR4 pins, but also the ADC0, TIM2, DAC0, SCL, SDA, DB2, DB3 pins when not used for their main function. This configuration can be performed using "AT" commands, please refer to the "TD1207R/08R Reference Manual" for details.
All the USR0, USR1, USR2, USR3, USR4, ADC0, TIM2, DAC0, SCL, SDA, DB2, DB3 pins can be configured individually as tristate (default reset state), push-pull, open-drain, with/without pull-up or pull-down resistor, and with a programmable drive strength (0.5 mA/2 mA/6 mA/20 mA).
When configured as inputs, these pins feature an optional glitch suppression filter and full (rising, falling or both edges) interrupt with wake-up from low-power mode capabilities. Of course, the pin configuration is retained even when using these low-power modes.
The operation of the GPIOs is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "TD1207R/08R Reference Manual".

4.7 RST (Reset)

The TD1207R/08R module features an active-low RST pin. This pin is held high by an internal pull-up resistor, so when not used, this pin can be left floating.

4.8 Debug

The TD1207R/08R module devices include hardware debug support through a 2-pin serial-wire debug interface. The 2 pins DB2 and DB3 are used for this purpose. The DB2 pin is the ARM Cortex-M3's SWDIO Serial Wire data Input/Output. This pin is enabled after a reset and has a built in pull-up. The DB3 pin is the ARM Cortex-M3's SWCLK Serial Wire Clock input. This pin is enabled after reset and has a built-in pull down. When not used for debug operation, these 2 pins can be configured to perform other functions using "AT" configuration commands, please refer to the "TD1207R/08R Reference Manual" for details.
Although the ARM Cortex-M3 supports advanced debugging features, the TD1207R/08R devices only use two port pins for debugging or programming. The systems internal and external state can be examined with debug extensions supporting instruction or data access break- and watch points.
For more information on how to enable the debug pin outputs/inputs the reader is referred to Section 28.3.4.1 (p. 457), the ARM Cortex-M3 Technical Reference Manual and the ARM CoreSight™ Technical Reference Manual.

4.9 RF Antenna

The TD1207R/08R supports a single-ended RF pin with 50 Ω characteristic impedance for connecting a matched-impedance external antenna. This pin is physically surrounded by 2 RF GND pins for better noise immunity.

4.10 VDD & GND

The TD1207R/08R provides 5 GND pins and 2 RF_GND pins: all of them must be connected to a good ground plane.
A 10 µF/6.3 V decoupling capacitor should be placed as closed as possible to the single VDD pin.

5 Bootloader

The TD1207R/08R module contains an integrated bootloader which allows reflashing the module firmware either over the RX/TX UART connection, or over the air using the built-in RF transceiver.
The bootloader is automatically activated upon module reset. Once activated, the bootloader will monitor the UART/RF activity for a 200 ms period, and detect an incoming update condition.
If the update condition is met, the TD1207R/08R will automatically proceed to flash the new firmware with safe retry mechanisms, or falls back to normal operation.

6 Package outline

Figure 6 illustrates the package details for the TD1207R/08R. All dimensions are shown in millimeters (mm).

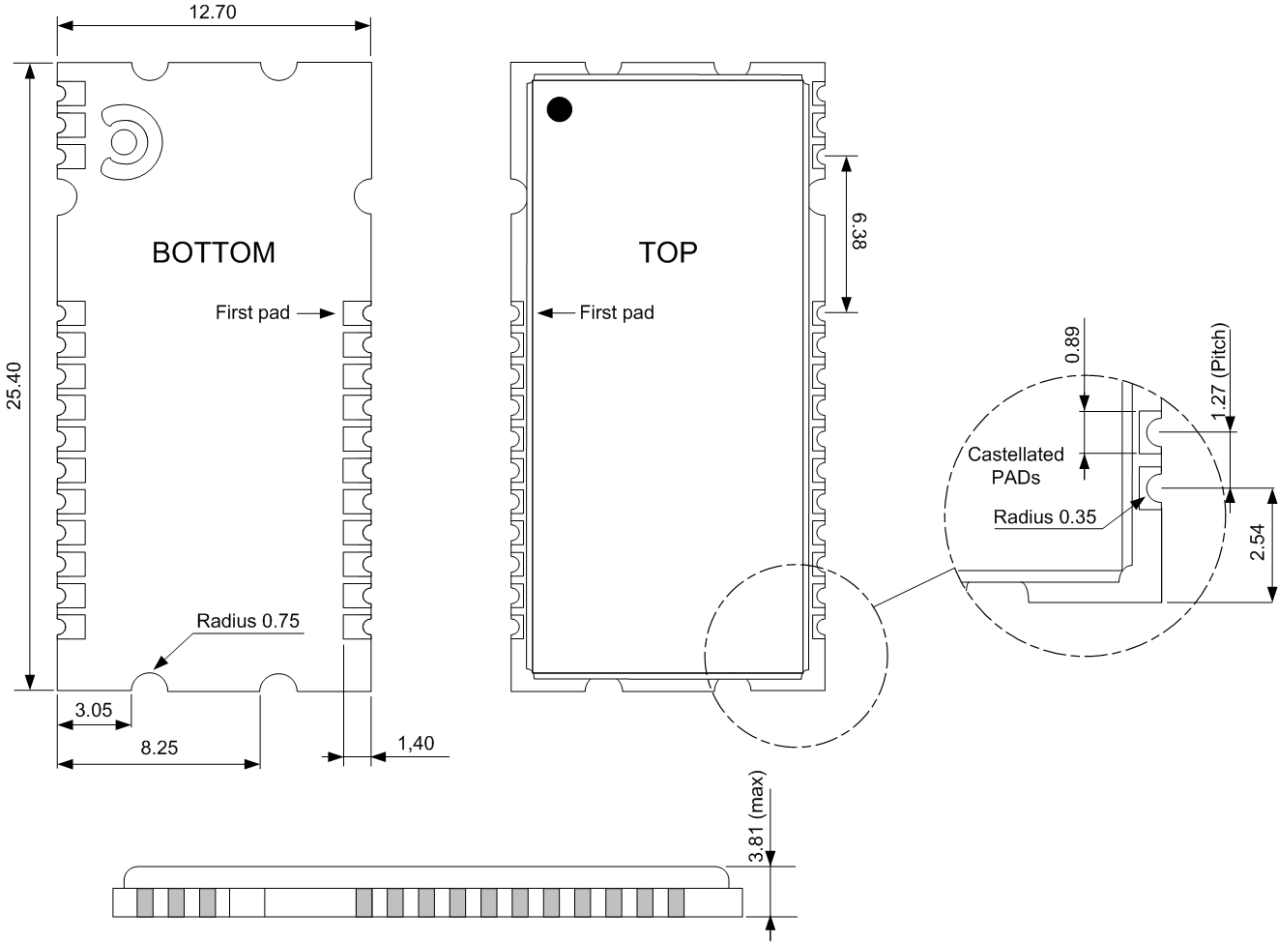


Figure 6. 25-Pin Land Grid Array (LGA)

7 Recommended PCB Land Pattern

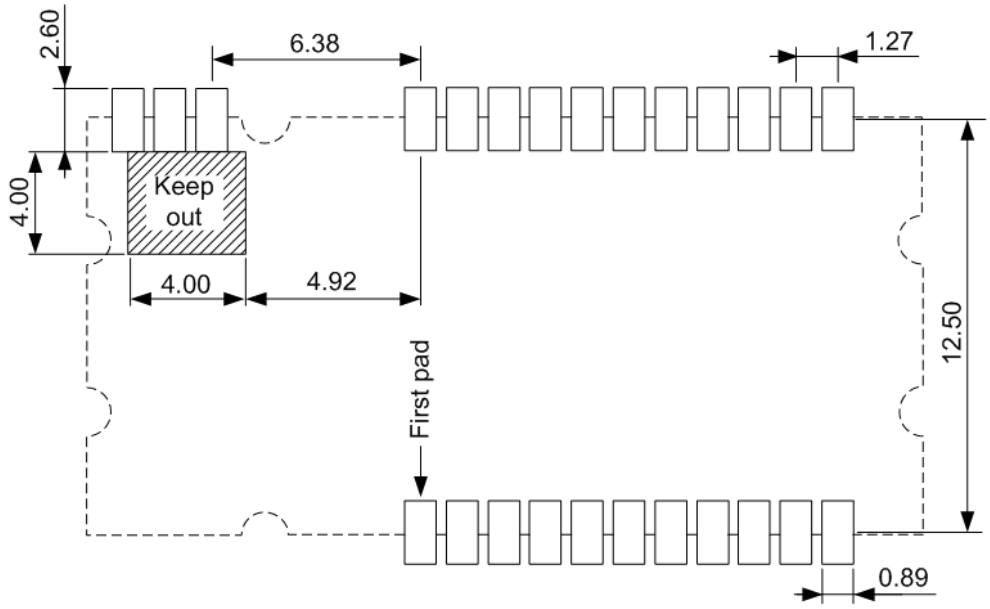


Figure 7. Recommended Land Pattern

Notes:

1. *All dimensions are shown in millimeters (mm) unless otherwise noted.*
2. *This land pattern is for reference purpose only. Consult your manufacturing group to ensure your company's manufacturing guidelines are met*

8 Ordering Information

Part number	Description	Package Type	Operating Temperature
TD1207R	ISM SIGFOX™ gateway 128K Flash / 16KRAM TCXO	LGA25 Pb-free	-30° to +75°C
TD1208R-C128	ISM SIGFOX™ gateway 128K Flash / 16KRAM TCXO	LGA25 Pb-free	-30° to +75°C

The TD1207R/08R ISM SIGFOX™ gateway module is available in several conditionings.
Please contact TDnext for more information.

9 Soldering information

9.1 Solder Stencil

The TD1207R/08R module is designed for RoHS reflow process surface mounting.

For proper module assembly, the solder paste must be applied on the receiving PCB using a metallic stencil with a recommended 0.150 µm thickness (1).

9.2 Reflow soldering profile

The recommendation for lead-free solder reflow from IPC/JEDEC J-STD-020D Standard should be followed.
For more information on reflow soldering process profiling, please visit the http://kicthermal.com/ website.

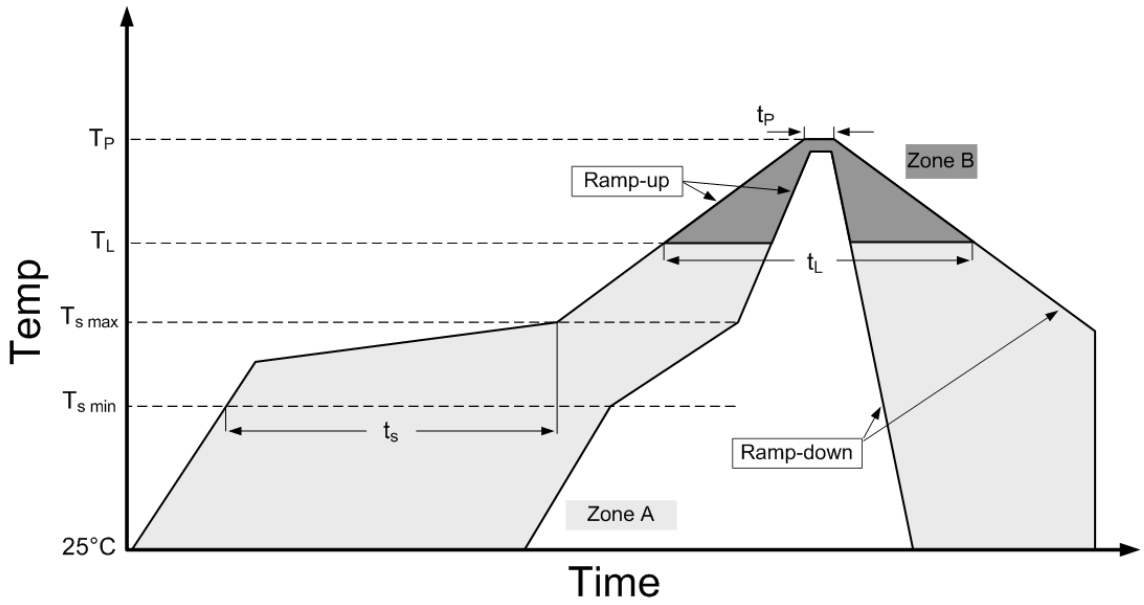


Figure 8. Recommended reflow soldering profile

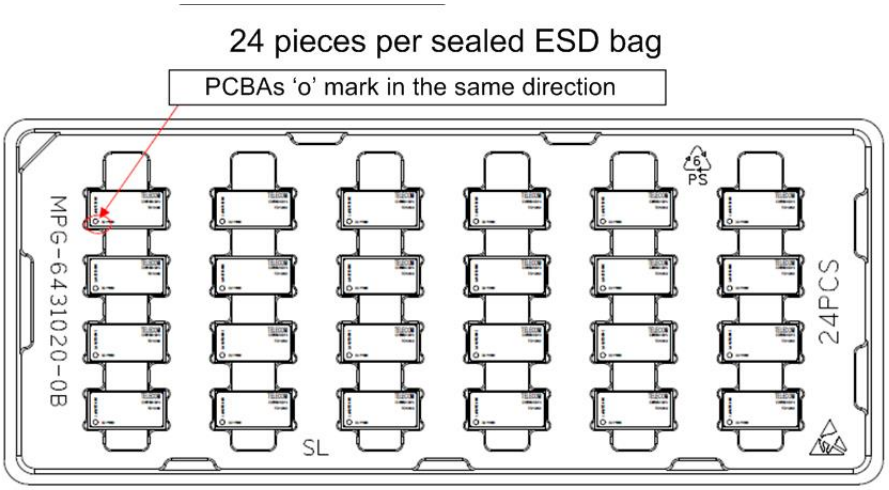
Table 10. Reflow soldering profile characteristics[1]

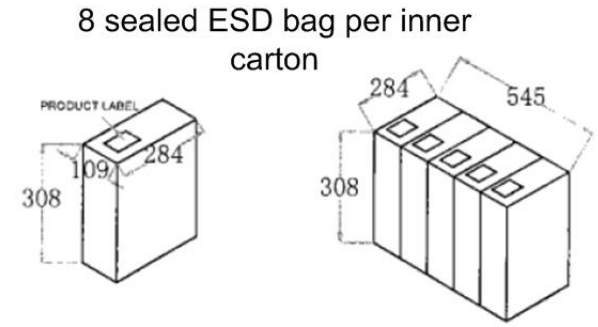
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Ramp-up	Reflow Ramp-up		-	-	3	°C/sec
Ramp-down	Reflow Ramp-down		-	-	6	°C/sec
T_S	Pre-Heating temperature	Solid phase of solder paste	125	-	200	°C
t_s	Pre-Heating time	Solid phase of solder paste	60	-	180	sec
T_L (2)	Phase temperature	Liquid phase temperature transition	-	217	-	°C
t_L	Reflow time	Liquid phase of solder paste	60	-	150	sec
T_p	Peak temperature		-	-	255	°C
t_p	Peak temperature time	Close to T_p Upper at 225°C	20 60	- -	40 90	°C

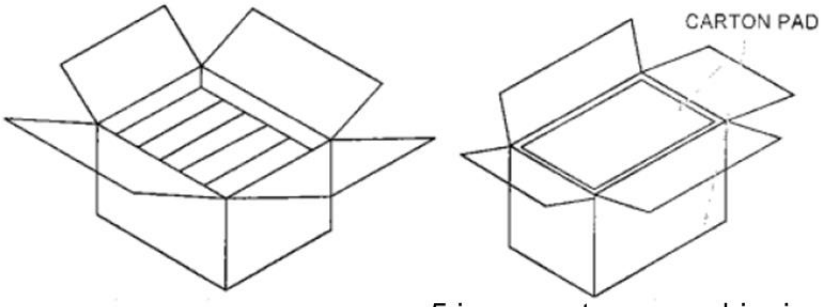
Notes:

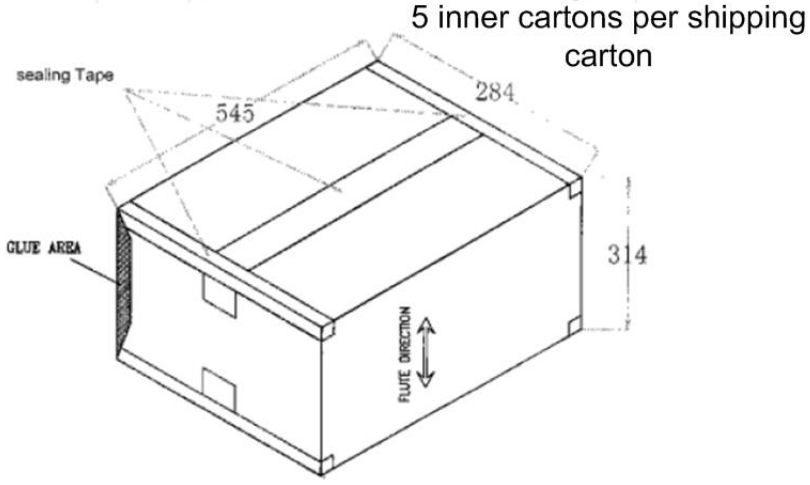
1. *This reflow soldering profile is for reference purpose only because it is strongly dependent of process used. Consult your manufacturing group to ensure your company's manufacturing guidelines are met*
2. *Liquid phase temperature of $S_nA_gC_u$ solder paste*

10 Shipping packaging









DOCUMENT CHANGE LIST

Revision 1.0

- TD1208R datasheet

Revision 1.1

- TD1207R reference added

Revision 1.2

- Figure 5 updated

CONTACT INFORMATION

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