TD1600ALF-4

Tuner module for digital terrestrial (OFDM) applications

Rev.c — 23-04-2007 **Preliminary data sheet**

1. General description

TD1600ALF-4 belong to the new generation of terrestrial tuners designed to cope with digital COFDM and analog transmission standards.

From function point-of-view these tuners can be divided into two high-frequency sections, a RF-loopthrough and a single conversion tuner part.

In the loopthrough section broadband low-noise amplifiers are used. The loopthrough frequency response covers the entire frequency range from VHF to UHF.

The RF-downstream section is equipped with a state-of-the-art single conversion tuner, which makes use of a highly integrated MOPLL IC that provides the required high level of performance necessary for COFDM signal processing.

The tuners are provided with a DC/DC converter to generate the tuning voltage internally.

The internal 4MHz PLL crystal reference frequency is fed through one of the pin-terminals and can be used as a clock for a 2nd device e.g. the channel decoder.

Two IF-outputs are provided, one is a wideband, non filtered IF-output, while the other, narrow-band IF-output is equipped with a SAW-filter and a gain controllable IF-amplifier. This narrow-IF-output matches the A-to-D converter input of currently available channel decoders.

All tuners out of this family can be equipped with two standard IEC-connectors, RF-in is IEC-female, RF-out is IEC-male. The tuner housing is available in a vertical or horizontal mountable execution; the pinning pitch corresponds to the World Standard Pinning convention.

Apart from the RF-connectors, all other terminals are made with wire pins at the bottom side of the tuner.

Table 1. Frequency allocation table

Parameter	TD1611ALF-4/ TD1311ALF-4	TD1344ALF-4
RF frequency range	174 MHz – 230 MHz	474 MHz – 858 MHz (*)
	474 MHz – 858 MHz (*)	
Channel bandwidth	7/8MHz	8 MHz
RF-loopthrough range	ch E2 - ch E69	ch E2 - ch E69
IF-center frequency	36.16 MHz	36.16 MHz
RF input connector	IEC female	IEC female
RF output connector	IEC male	IEC male

(*) data refer to RF-channel center frequency.

2. Features

- Highly integrated RF-module, 3-band tuner plus active loopthrough
- +5V supply voltage only; no external tuning voltage required
- Tuners for horizontal and vertical mounting available
- Option with DC – power output through input connector (e.g. indoor antenna supply)
- Tuners comply with relevant CENELEC standards with regard to requirements concerning signal handling capability and immunity
- Superior low noise and high sensitivity performance
- RF-in to RF-out loopthrough amplifiers
- Low noise and excellent linearity
- Full VHF to UHF frequency range coverage
- Standard connectors for in- and output e.g. IEC, F-connector, RCA
- High performance and cost effective single conversion tuner
- I2C programmable
- 400kHz Bus compliant
- Fast PLL tuning speed (programmable step size e.g. 62.5kHz and 166.67kHz)
- Tuner internal gain control loop with selectable TakeOverPoint settings via I2C Bus
- External gain control possible with internal loop disabled
- 4.0V (max. gain) to 0V (min. gain) gain control voltage
- Flat overall frequency response
- High PLL loop bandwidth which ensures very low oscillator phase noise
- 4 MHz crystal reference frequency output
- SAW-filter and IF-amplifier included
- Switchable 7/8 MHz SAW filter
- Fixed 8 MHZ SAW filter
- IF-amplification controllable over a wide range

- Differential, filtered (SAW) ‘digital’ IF-output to directly drive the channel decoder

3. Ordering information

Table 2. Ordering information

Table description (optional)

Type number	Package		
	Name	Description	Version
TD1611ALF/IVP-4	3112 297 15531	VHF 3 – UHF PLL tuner, Loopthrough, antenna power, Screw hole, DC/DC converter, IEC connector, vertical mount	-
TD1611ALF/IHP-4	3112 297 15521	VHF 3 – UHF PLL tuner, Loopthrough, antenna power, Screw hole, DC/DC converter, IEC connector, horizontal mount	-
TD1311ALF/IVP-4	3112 297 15491	VHF 3 – UHF PLL tuner, Loopthrough, antenna power, DC/DC converter, IEC connector, vertical mount	-
TD1311ALF/IHP-4	3112 297 15481	VHF 3 – UHF PLL tuner, Loopthrough, antenna power, DC/DC converter, IEC connector, horizontal mount	-
TD1644ALF/IVP-4	3112 297 15631	UHF only PLL tuner, loopthrough, antenna power, Screw hole, DC/DC converter, IEC connector, vertical mount	-
TD1644ALF/IHP-4	3112 297 15621	UHF only PLL tuner, Loopthrough, antenna power, Screw hole, DC/DC converter, IEC connector, horizontal mount	-
TD1344ALF/IVP-4	3112 297 15511	UHF only PLL tuner, Loopthrough, antenna power, DC/DC converter, IEC connector, vertical mount	-
TD1344ALF/IHP-4	3112 297 15501	UHF only PLL tuner, Loopthrough, antenna power, DC/DC converter, IEC connector, horizontal mount	-
TD1311AF/PHP-4	3112 297 15691	VHF 3 – UHF PLL tuner, antenna power, DC/DC converter, phono connector, horizontal mount	-

4. Block diagram

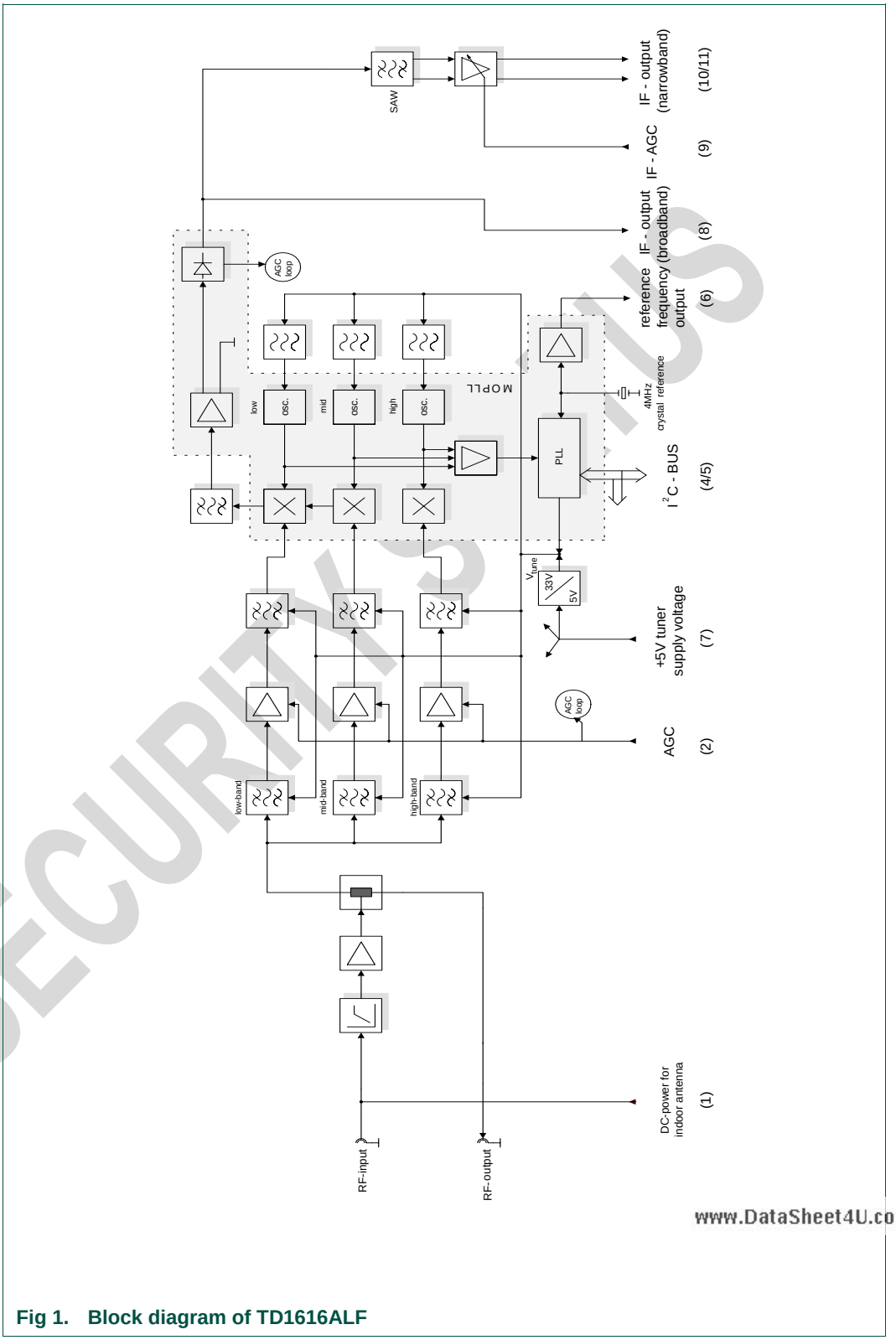


Fig 1. Block diagram of TD1616ALF

5. Pinning information

5.1 Pinning

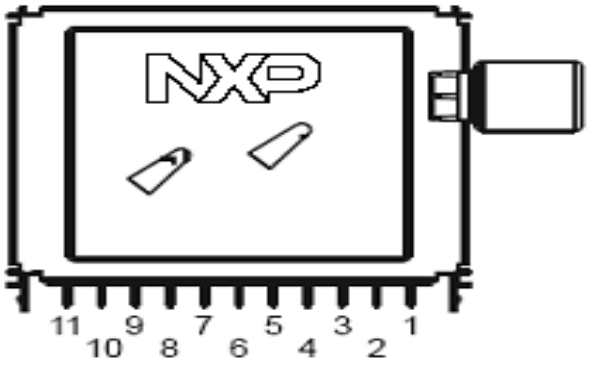


Fig 2. Pinning diagram

5.2 Pin description

Table 3. Pin description

Table description (optional)

Pin	Description
1	DC-power option for tuners with P-extension [1]
2	External RF-gain control voltage (0.5V - 4.0V)[2]
3	PLL chip address select (I^2C / tuner) [3]
4	SCL (I^2C / tuner)
5	SDA (I^2C / tuner)
6	4MHz reference frequency output [4]
7	+5V ± 5% supply tuner (V_{TU})
8	'broadband' IF – output[4]
9	IF-gain control voltage [5]
10	'narrowband' IF – output 1[4]
11	'narrowband' IF – output 2[4]

[1] Max. permissible current: 35mA

[2] Max. permissible control voltage source impedance limited to 200ohms (see application notes)

[3] see application notes

[4] AC coupled

[5] max. gain at 3V,min. gain at 0V (see application notes)

6. Limiting values

Table 4. Limiting values under non-operational conditions

Table description (optional)

Symbol	Parameter	Conditions	Min	Max	Unit
T_{AMB}	Ambient temperature		-25	+85	°C
RH	Relative humidity		-	95	%
g_B	Bump acceleration	25g	-	245	m/s^2
g_S	Shock acceleration	50g	-	490	m/s^2
A_{vib}	Vibration amplitude	10Hz to-55 Hz	-	0.35	mm

7. Static Characteristics

Table 5. Static characteristics

T_{AMB} = -10 °C to +60 °C, RH=95

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_L	DC-loopthrough to input connector	Optional	-	-	20	V
I_L	Max. permissible current		-	-	35	mA
V_{TU}	Tuner supply voltage		4.75	5.00	5.25	V
I_{TU}	Relevant supply current		180	200	210	mA
V_{AGC}	Tuner AGC input voltage		-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range		0.3	-	4.0	V
I_{AGC}	AGC control current	at 0V AGC voltage	-2	-	-	mA
$V_{IF\text{-}AGC}$	IF- AGC input voltage		-	3.0	4.0	V
$\Delta_{VIF\text{-}AGC}$	IF- AGC input voltage range		0	-	3.5	V
$I_{IF\text{-}AGC}$	IF- AGC input current		-	-	10	µA
V_{AS}	Address select input voltage		-	-	5.25	V
V_{SCL}	Serial clock input voltage		-0.3	-	5.25	V
V_{SDA}	Serial data input voltage		-0.3	-	5.25	V
I_{SDA}	Serial data input current		-1	-	5	mA

8. Dynamic Characteristics

Next specification data refer to the overall performance from RF-input to IF-output.

If not otherwise stated, all data are assigned to broadband IF-output.

The tuner has to be tuned as such that coincidence between RF-channel center and IF-center frequency of 36.16 MHz is given.

Table 6. Dynamic characteristics

T_{amb} = 22 °C ±2 °C; RH =60%±10%; V_{TU}=5V±0.1V; V_{RF_AGC}=4.0V±0.1V(internal AGC detector disabled):V_{IF_AGC} =1V(maximum); $Z_{i(RF)}$ = 75Ω; $Z_{o(RF)}$=75Ω; unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Unit
Frequency ranges [1]	TD1611 (VHF high)	174		230	MHz
	TD1611 (UHF)	470		862	MHz
	TD1644 (UHF)	470		862	MHz
RF power gain [2]		47	50		dB
Overall gain taper			6		dB
RF AGC range	Low band	40			dB
	Mid band	40			dB
	High band	35			dB
Image rejection (Referred to IF-center frequency)	VHF high (mid band)	66	70		dB
	UHF (high band)	55	60		dB
Osc. voltage at aerial input	(f < 1000MHz)		<20		dBµV
In-channel return loss [3]		5	7		dB
Overloading causing 1dB gain compression			76		dBµV
Noise figure	at nom. gain		5	6	dB
ESD protection of terminals		2			kV
Surge protection at RF-input		5			kV
Osc. phase noise [4]	At 1 kHz		-88	-78	dBc/Hz
	At 10 kHz		-90	-82	dBc/Hz
Overall voltage gain [5]			70		

[1] channel center including tuning margin

[2] to be measured at 'broadband' IF-output with 75ohms load

[3] to be measured at RF-input in the range channel-center ± 3MHz

[4] PLL step size 166.667kHz / 148.86kHz; CP as recommended (see application notes)

[5] measured at terminals 10/11; IF-AGC voltage (terminal 9) set to 3V

Cross-modulation:

Definition: The cross-modulation is defined as the transfer of the adjacent channels' modulation depth to the wanted carrier.

Measurement:

Unwanted carriers (f_{unw}) = wanted carrier (f_w) ± 8MHz

Level of all carriers = 70dBµV

Modulation = AM, 50%, 15kHz

IF-output loaded with 1kΩ // 15pF // 1.2uH (load compensation)

IF-output level limited to 104dBµV

Spec. limit: max. cross-modulation is less or equal 1% (typ. 0.3%)

Flatness (tilt) of overall responds curve (to be measured at broad-band IF-output):

Definition: tilt of curve is defined in the specified IF-range from highest to lowest gain point at nom. gain

Measured at broadband IF-output:

- in the range IF-center ± 3MHz : 3dB max.
- in the range IF-center ± 4MHz : 4dB max.

Deterioration of flatness during AGC (0dB to 30dB): 1.0dB max.

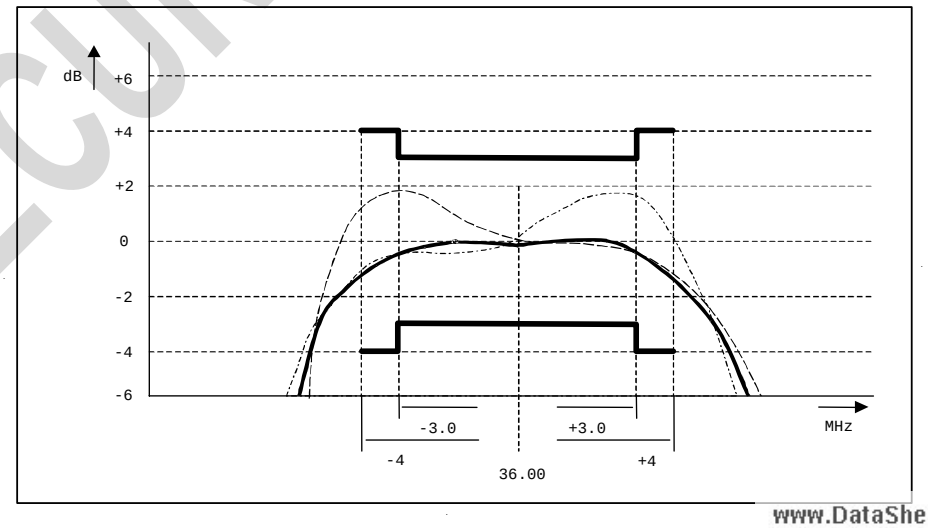
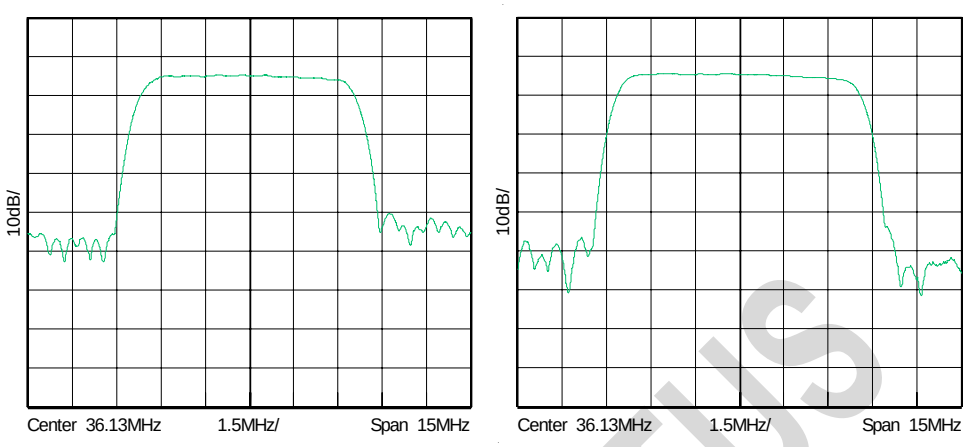


Fig 3. Flatness (tilt) of overall responds curve



a. 7MHz wide SAW-filter selected b. 8MHz wide SAW-filter selected

Fig 4. Typical response curves at narrowband IF-output

8.1 Input sensitivity:

The typical input sensitivity, when measured in an adequate application (i.e. Philips Semiconductors COFDM reference board OM5754) is: - 82dBm , BER $2x10^{-4}$ post Viterbi

Conditions: Gaussian channel w/o added noise, 8k OFDM, 64QAM, code rate 2/3, guard interval 1/8

8.2 4MHz reference output (terminal 6):

Frequency accuracy : 80ppm max.

Max. permissible load : t.b.f.

Output level : 440mVpp typ.

[0°C - 60°C ;

supply voltage (terminal 7) +5V±5% ;

loaded with min. t.b.d.]

Phase Noise @ 1kHz : -104dBc/Hz typ.

8.3 Overall performance from RF input to RF output

Table 7. Overall performance from RF input to RF output

Specification data refer to the overall performance from RF-input to RF-output. (valid for all tuners out of this family)

Parameter	Min	Typ	Max	Unit
Frequency range (referred to channel center)	51		858	MHz
Power gain	0		3	dB
Overall gain taper		2.5		dB
Noise figure (tuners w/o remod)		5		dB
CSO / CTB (acc. EN50083)	-57			dBc
RF-output return loss (referred to 75Ω)		10		dB

9. Application information

9.1 Programming of tuner PLL

The tuner control (frequency selection and band switching) is done via the I^2C bus.

One address byte and four data bytes are needed to fully program the tuner.

A PLL lock flag can be read from the tuner during 'READ' - mode.

Four independent PLL addresses are available; which one is actually valid depends on the address select voltage that is connected to terminal 3.

TD1300ALF tuners comply to the 5V I^2C – Bus specification.

Table 8. -bus data format ' WRITE ' - mode:

Name	Description	7	6	5	4	3	2	1	0	ACK
ADB	Address byte	1	1	0	0	0	CA1	CA0	R/W=0	A
DIV1	Divider byte1	0	N14	N13	N12	N11	N10	N9	N8	A
DIV2	Divider byte2	N7	N6	N5	N4	N3	N2	N1	N0	A
CB1	Control Data Byte1	1	D/A=1	0	0	1	R2	R1	R0	A
		1	D/A=0	0	0	ATC	AL2	AL1	AL0	A
CB2	Control data byte2	CP2	CP1	CP0	SP5	SP4	SP3	SP2	SP1	A

Table 9. Description of used symbols

Symbol	Description	Conditions
CA1, CA0	Chip address selection bits[1]	
R/W	Read/write bit	Bit = 0 (write mode), bit = 1 (read mode)
N14 to N0	LO frequency divider bits	-
D/A	D/A = 1 ⇒ following 6 bits contain test and reference divider ratio data	
	D/A = 0 ⇒ following 6 bits contain AGC setting data	
R2, R1, R0	Reference divider bits [2]	
SP5 ..... SP1	Band selection and SAW filter switch ports	
ATC	AGC time constant data bit; only valid with int. AGC loop active	ATC = 1 ⇒ enables fast tuning speed during channel search mode
		ATC = 0 ⇒ recommended after channel acquisition; normal mode
AL2, AL1, AL0	AGC Take-Over-Point bits [3]	
CP2, CP1, CP0	PLL charge pump current selection bits [4]	
SP5 - SP1	Switch ports [5]	bit = 1 ⇒ port V_{out} is 'ON'
		bit = 0 ⇒ port V_{out} is 'OFF
CA1, CA0	Programmable address selection bits [6]	

[1] See table: Programmable address selection

[2] See table: Reference Divider Settings

[3] see table: Internal AGC loop TOP

[4] see table: Charge Pump Settings

[5] see table: Band and SAW-filter selection table

Table 10. Programmable address selection bits (CA1, CA0)

CA1	CA0	Voltage applied to terminal 3
0	0	0V to 0.1x VTU
0	1	Terminal open
1	0	0.4xVTU to 0.6xVTU
1	1	0.9xVTU to 1.0xVTU

N14 to N0: programmable divider bits

divider ratio: $N = N14x2^{14} + N13x2^{13} + ... + N1x2^{1} + N0$

How to calculate the divider ratio N :

$$N = \frac{\left(f_{input} + f_{IF}\right)}{f_{ref}}\left[\frac{Hz}{Hz}\right] \quad \text{whereby} \quad f_{ref} = \frac{4 \cdot 10^6}{64^{(1)}}[Hz] = 62.5kHz$$

$$f_{ref} = \frac{4 \cdot 10^6}{24^{(1)}}[Hz] = 166.67kHz$$

$$f_{ref} = \frac{4 \cdot 10^6}{28^{(1)}}[Hz] = 142.86kHz$$

Note (1) : divider ratio to be set with Bits ' R2 ..... R0 ' (see table below)

Do not set the divider ratio as such that the tuner is tuned into extreme conditions i.e. far below or far above the specified ranges.

R2, R1, R1: PLL reference divider settings (Control Data Byte 1):

Important note: in order to avoid instabilities of the reference divider it is advisable to set the reference divider in combination with the IF-frequency and channel spacing as per below table

Table 11. PLL reference divider settings (Control Data Byte)

PLL step size (kHz)	PLL ref. divider ratio	R2	R1	R0	IF frequency (MHz)	Channel spacing (MHz)
142.86	28	0	0	1	36.16	8
166.67	24	0	1	0	36.16	6 and 7

AL2, AL1, AL0: AGC Take-Over-Point bits (Control Data Byte 1):

External AGC mode: The tuner can be controlled by an external gain control voltage applied to terminal 2 of the tuner.

In that case the ALx - bits need to be set as shown in table below.

The impedance of the control voltage source should not exceed 200ohms.

Table 12. External AGC mode setting

AL2	AL1	AL0	Typical TOP level	Remarks
0	0	0	124dBuV	
0	0	1	121dBuV	-
0	1	0	118dBuV	-
0	1	1	115dBuV	-
1	0	0	112dBuV	-
1	0	1	109dBuV	-
1	1	0	I_{AGC} = 0	External AGC [1]
1	1	1	V_{AGC} = 3.5V	Loop disabled [2]

[1] The tuner internal AGC current sources are disabled (default mode after power on reset).

[2] The tuner internal AGC detector is disabled. With no external AGC voltage applied to the tuner, the RF-gain is always set to maximum.

CP2, CP1, CP0: PLL charge pump current settings

Note: during search tuning it is recommended to set the PLL to a moderate charge pump.

To enable best oscillator phase noise performance during digital signal processing, the PLL charge pump current should be set to conditions as given with following table.

Table 13. PLL charge pump current settings

CP2	CP1	CP0	Typical CP current (uA)	Recommendations
0	0	0	40	-
0	0	1	60	-
0	1	0	90	To be used during search tuning and for 50kHz, 62.5kHz PLL step sizes
0	1	1	130	Low band: 87MHz to 130MHz
				Mid band: 200MHz to 290MHz
				High band: 480MHz to 620MHz
1	0	0	190	-
1	0	1	280	Low band: 130MHz to 160MHz
				Mid band: 290MHz to 420MHz
				High band: 620MHz to 830MHz
1	0	1	280	Low band: 130MHz to 160MHz
				Mid band: 290MHz to 420MHz

1	1	0	410	Low band: >160MHz(*)
				Mid band: >420MHz(*)
1	1	1	600	High band: >830MHz (*)

(*) oscillator frequencies

Table 14. SP5 ……SP1 Band and SAW-filter selection table

Band	SP5	SP4	SP3	SP2	SP1
Low – band	0	X	0	0	0
Mid – band	0	X	0	1	0
High – band	0	X	1	0	0
7 MHz SAW filter	0	0	X	X	X
8 MHz SAW filter	0	1	X	X	X

Table 15. I ^{2}C-bus data format, ' READ ' - mode

Description	7	6	5	4	3	2	1	0	ACK
Address byte	1	1	0	0	0	CA1	CA0	R/W=1	A
Status byte	POR	FL	0	1	AGC	1	0	0	A

A : Acknowledge

CA1 / CA0 = chip address (see address selection table)

POR= power-on-reset-flag ; POR = 1 after power-on

FL= in-lock-flag ; FL = 1 when PLL is phase locked

AGC= internal AGC flag ; AGC = 1 when internal AGC is active

Timing of program sequences:

Because of the Tuner – PLL frequency divider settling time of min. 60usec. , the occurrence of any other I2C traffic start condition present within that periode on the Bus will disturb the divider and result in a not properly tuned tuner VCO.

Each time the Tuner-PLL frequency divider has been programmed, a 60usec wait becomes necessary before continuing the I2C bus traffic.

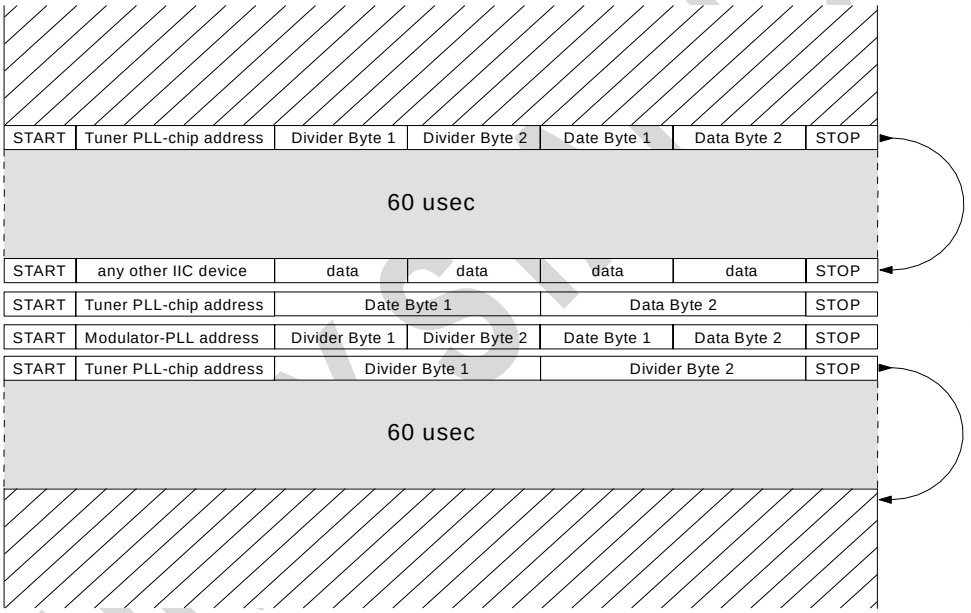


Fig 5. Program sequence

9.2 Max. Permissible IF-load impedance:

The max. load applied to the ' broadband ' IF-output of the tuner should not exceed:

2kΩ min.//15pF max.

The reactive load has to be compensated (tuned-out to the IF-center frequency) by an inductance connected in parallel to the load.

The max. load applied to the ' narrowband ' balanced IF-output of the tuner is limited to 1kΩ min.

9.3 Gain control characteristics of IF amplifier

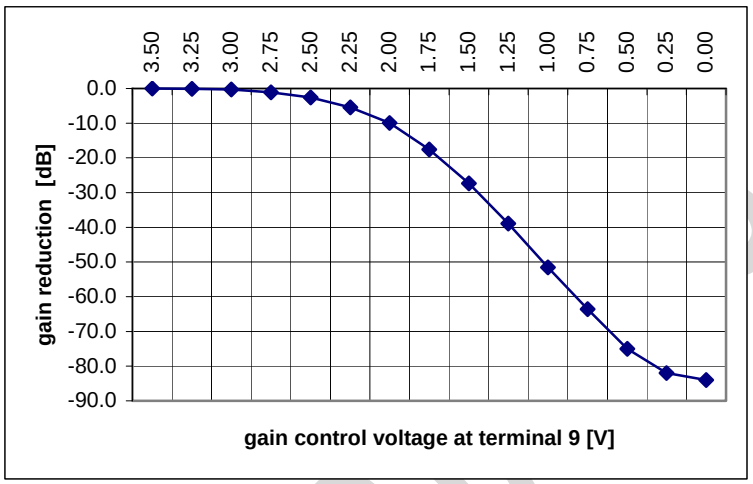
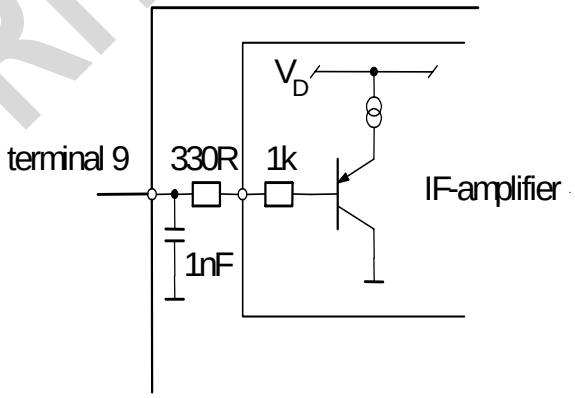
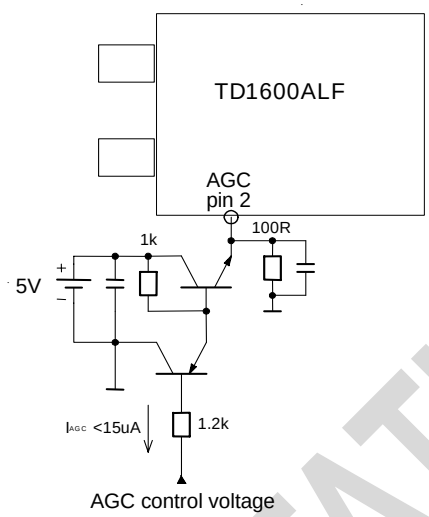


Fig 6. Gain control characteristic of IF-amplifier (terminal 9)



(1) With an IF-gain control voltage of about 1.3V applied to terminal 9 of tuner, the narrowband IF-output level is about the same of the broadband IF-output.

Fig 7. Internal AGC circuit



Note: In case the above recommended AGC control voltage source is not used, alternatively a control voltage source with a max. 200ohms impedance can be used

Fig 8. External RF-Gain Control Voltage; recommended schematic

9.4 Phase noise, I²C bus traffic and crosstalk

The low noise PLL used in these tuners will clean up the noise spectrum of the VCOs close to the carrier to reach noise levels @ 1 kHz offset from the carrier compatible with e.g. OFDM reception.

Linked to this noise improvement, some disturbances may become visible while they were not visible because they were hidden into the noise in analog dedicated applications and circuits.

This is especially true for disturbances coming from the I²C bus traffic, whatever this traffic is intended for the MOPLL or for another slave on the bus.

To avoid this I²C bus crosstalk and be able to have a clean noise spectrum, it is necessary to use a bus gate that enables the signal on the bus to drive the MOPLL. This is used only when the communication is intended for the tuner part (such a kind of I²C bus gate is included into the Philips terrestrial channel decoders), and to avoid unnecessary repeated sending of the same information.

9.5 Main board recommendations:

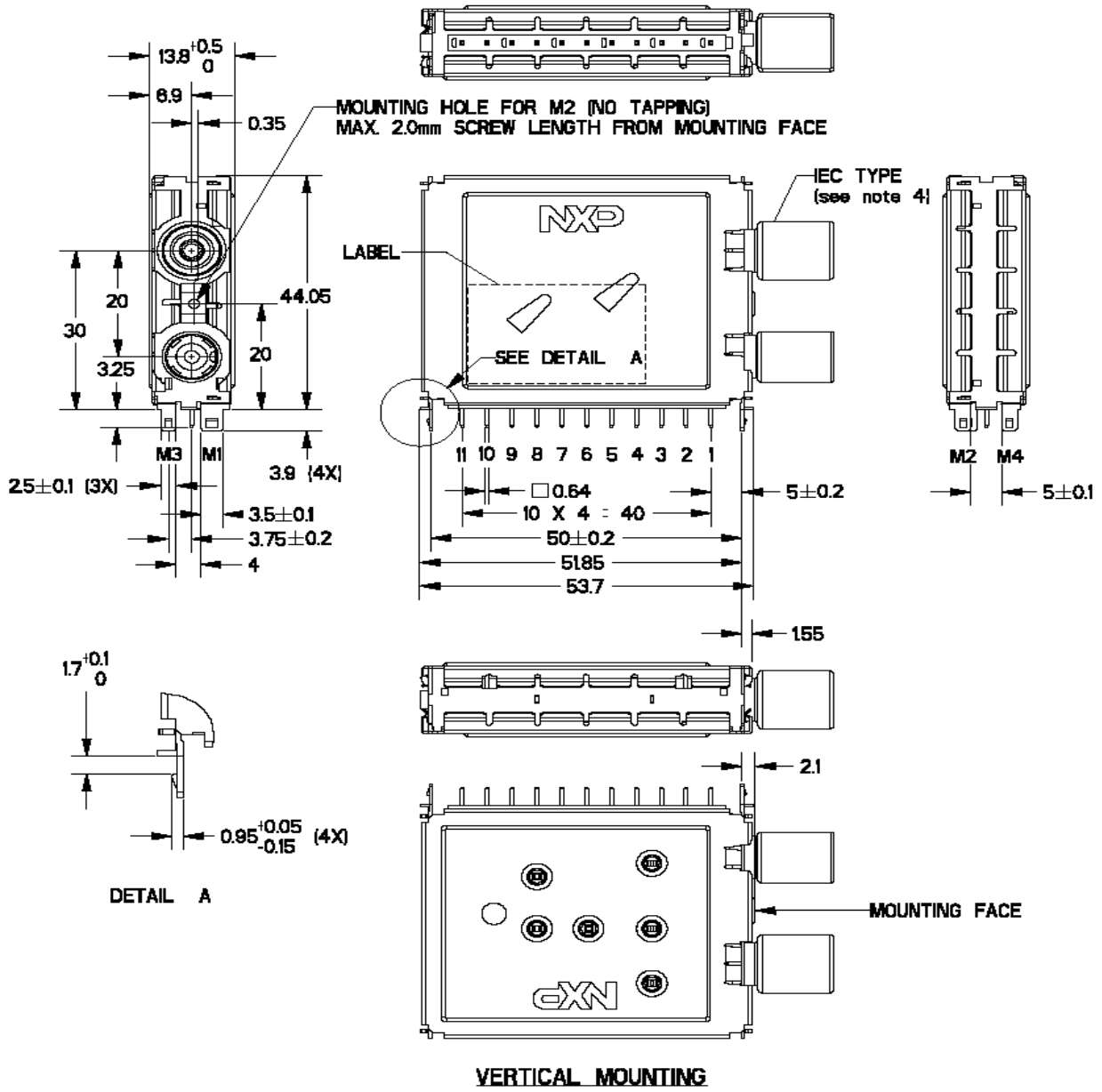
The tracks on the main board connected to the tuners' terminals should be kept as short as possible in order to avoid interferences because of immunity problems and/or to avoid problems with regard to radiation of the local oscillator.

9.6 For tuners with antenna-power function (tuners with type name extension “P”)

Attention:

Modules with type name extension 'P' do have the DC-supply option through out the RF-input connector on board. The max. permissible current drive has to be limited to 35mA . Should this option be used in the end application, it is recommended that an electronic switch with some current protection circuitry be employed, to avoid damage to the tuner itself.

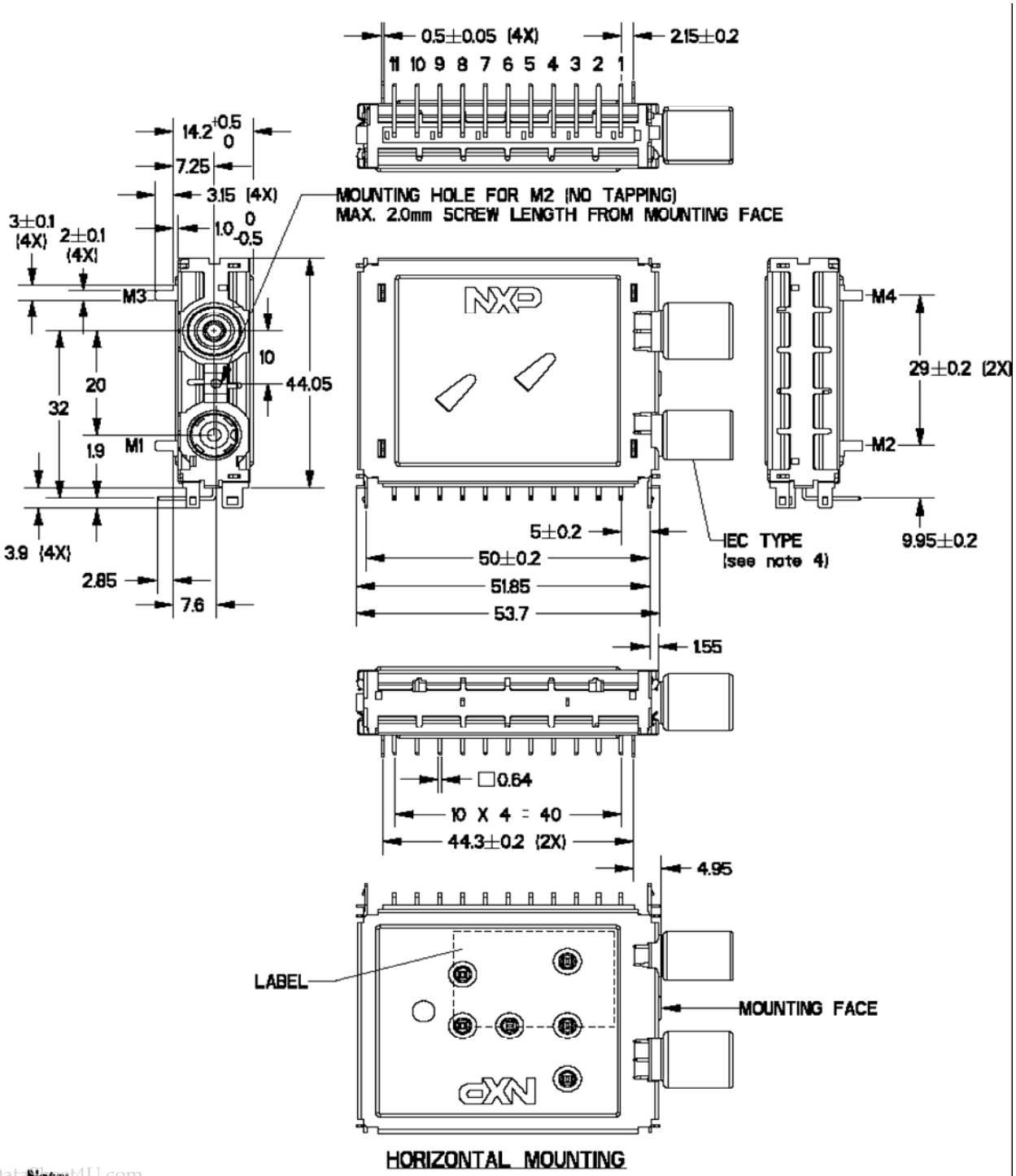
10. Package outline



Note:
1) General tolerance ±0.5 mm unless otherwise stated.
2) All dimensions are in millimeter.
3) Drawing not to scale.
4) For details on connector types and dimensions, refer to sheet 110-03.

(1)

Fig 9. Package outline of TD1600ALF-4



Note:
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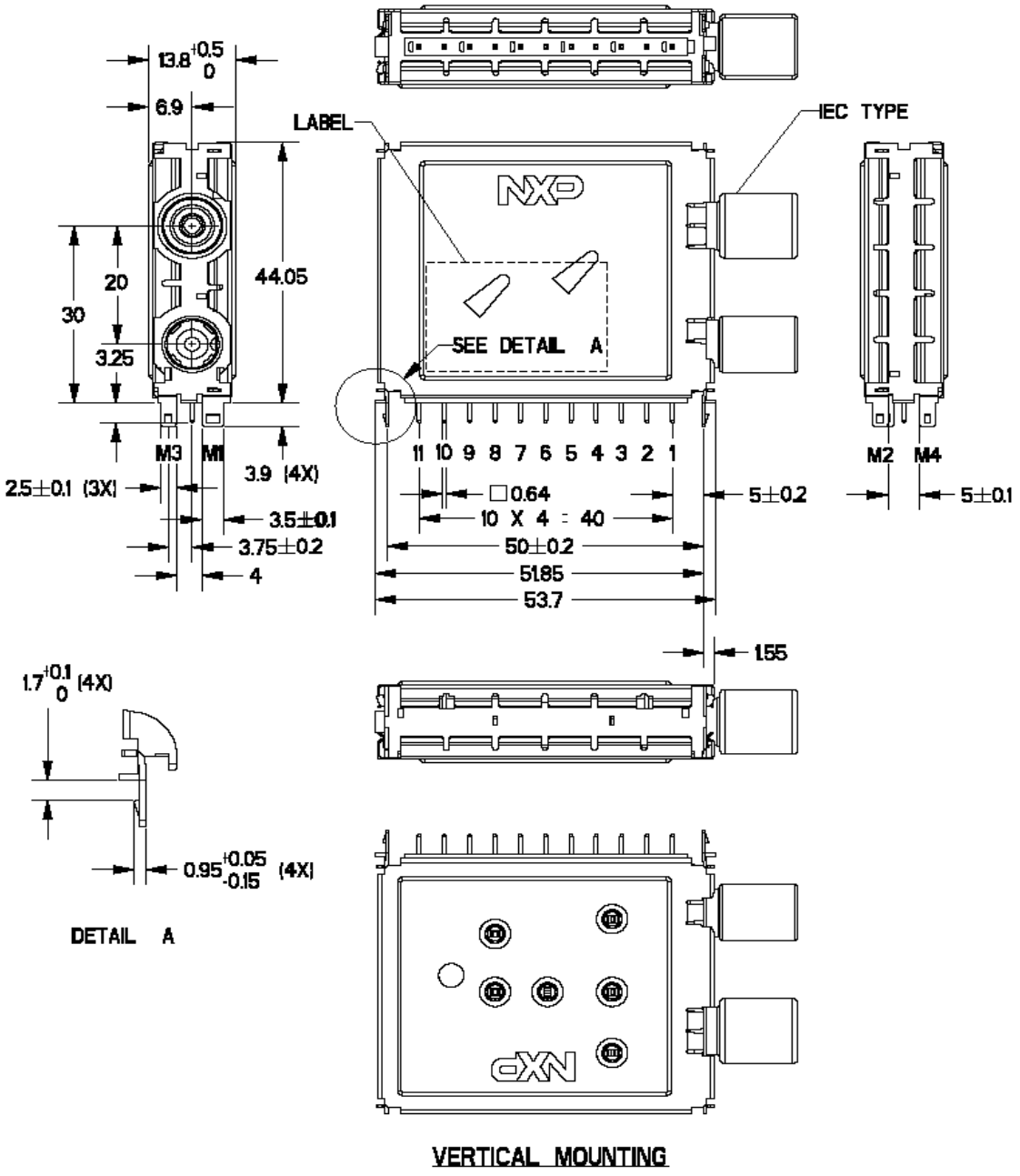
Fig 10. Package outline of TD1600ALF-4



Note:
- General tolerance ±0.5 mm unless otherwise stated.
- All dimensions are in milimeter.
- Drawing not to scale.

Fig 11. Package outline of TD1300ALF-4

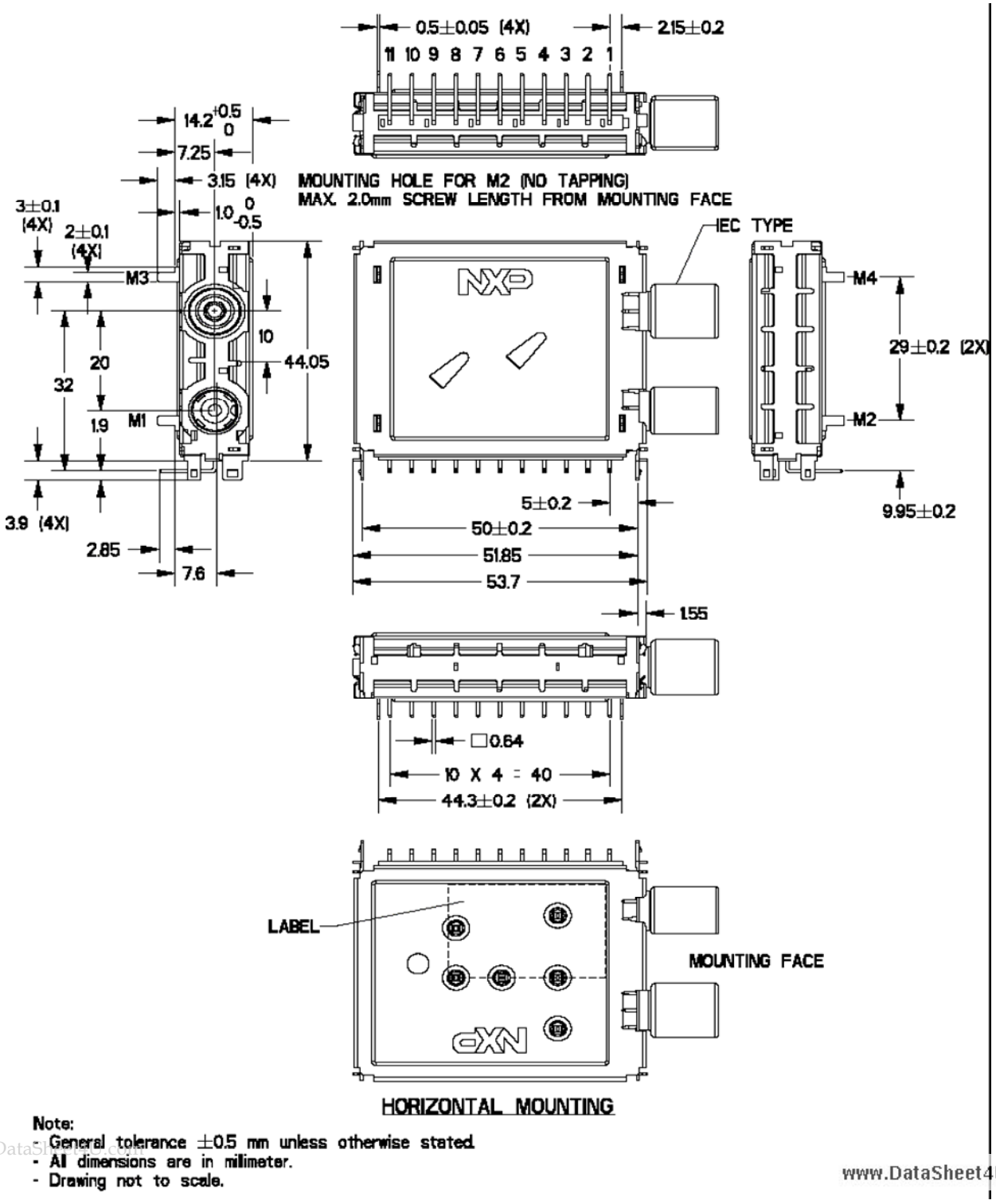
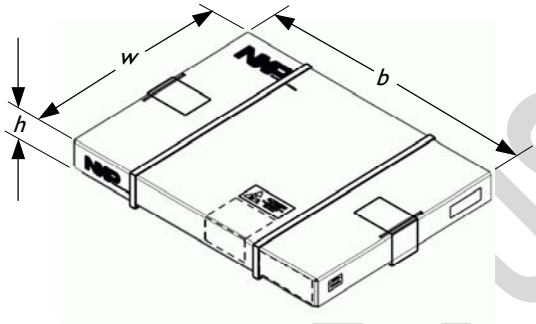


Fig 12. Package outline of TD1300ALF-4

11. Packing information

The products are packed in the carton box and transferred to customers by Pallet Transport.



Carton Boxes are made of Corrugated Fibreboard which are free of environmentally banned substances.

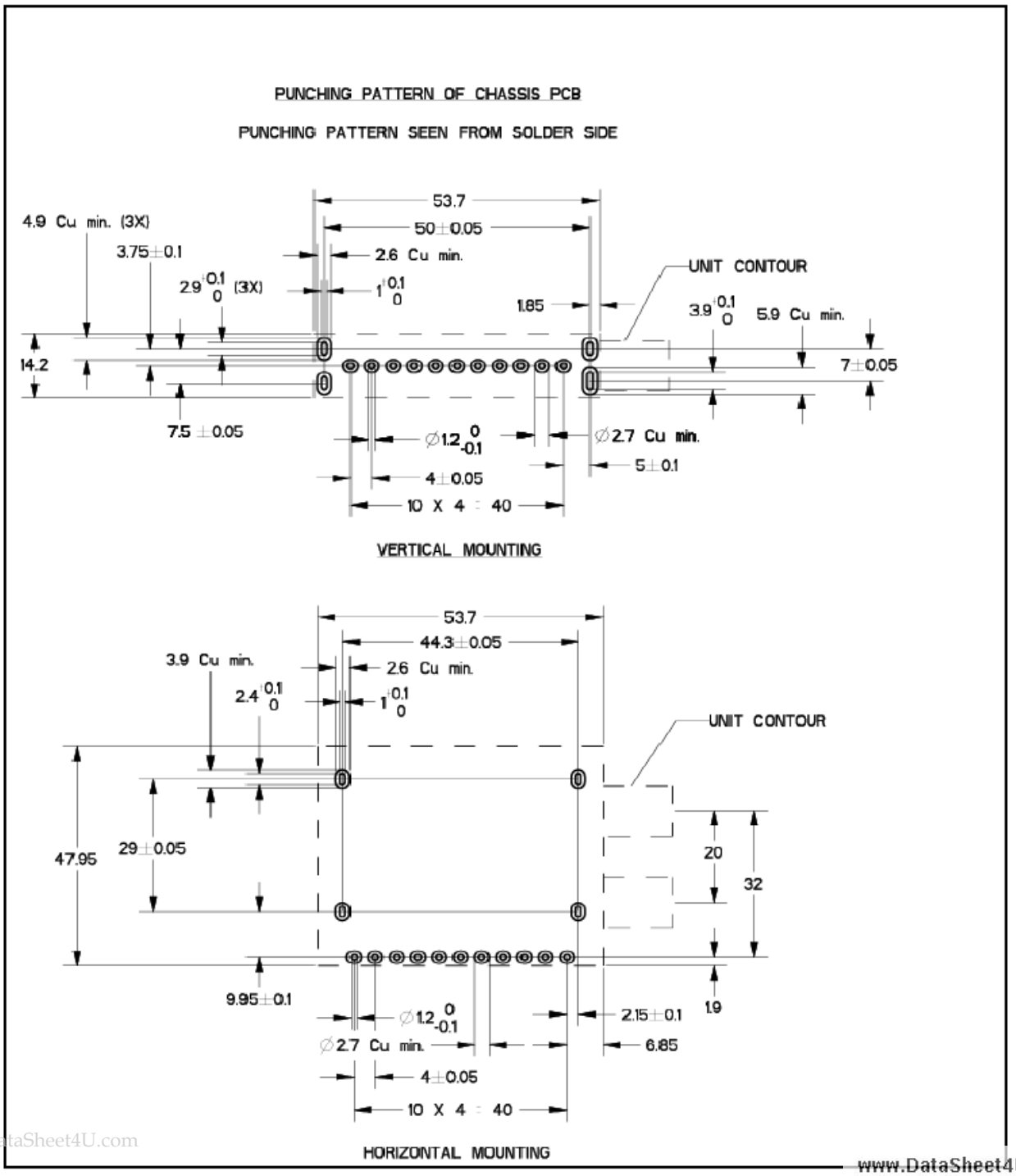
Fig 13. Example of carton box

Table 16. Package information

Table description (optional)

Package	Dimension L x W x H (cm)	Number of sets	Gross weight (kg)
Carton vertical	46 x 34 x 7.5	98	4.09
Pallet vertical	120 x 105 x 105	7742	345.1
Carton horizontal	46 x 34 x 9.4	60	3.16
Pallet horizontal	120 x 105 x 105	3900	227.4

12. Mounting



(1)

Fig 14. Punching pattern of chassis PCB

13. Revision history

Table 17. Revision history

Table description (optional)

Document ID	Release date	Data sheet status	Change notice	Supersedes
TD1600ALF-4	2007-01-19	Objective data sheet	Rev a-	-
Modifications	-			
TD1600ALF-4	2007-03-23	Preliminary data sheet	Rev b	Rev a
Modifications	• Mechanical drawings updated to NXP cover • Packaging information updated • Supply voltage and performance data updated • Change status to Preliminary • TD1644ALF/IVP-4 and TD1644ALF/IHP-4 added Pg 2 - Add product 12nc			
TD1600ALF-4	2007-04-23	Preliminary data sheet	Rev c	Rev b
Modifications	• New type TD1311AF/PHP-4 added in page 3			

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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