

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

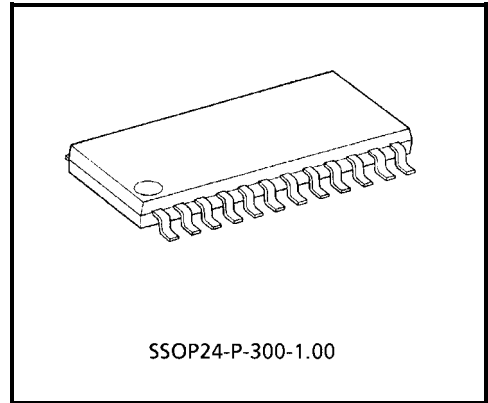
TD62C853F,TD62C854F

8BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH DRIVERS

The TD62C853F and TD62C854F are monolithic circuits designed to be used together with Bi-CMOS integrated circuits. The devices consist of a 8 bit shift register, 8 bit latches, and 8 output circuits.

FEATURES

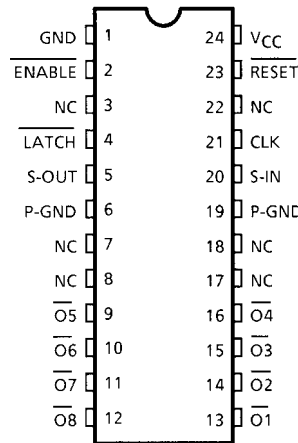
- 8 bit serial-in parallel-out shift register / latch driver (Bi-CMOS process)
- Maximum output sustaining voltage ; 50 V
- Maximum output current ;
TD62C853F 200 mA / ch (Low saturation type)
TD62C854F 500 mA / ch (darlington type)
- CMOS compatible inputs
- Package ; SSOP24-P-300-1.00



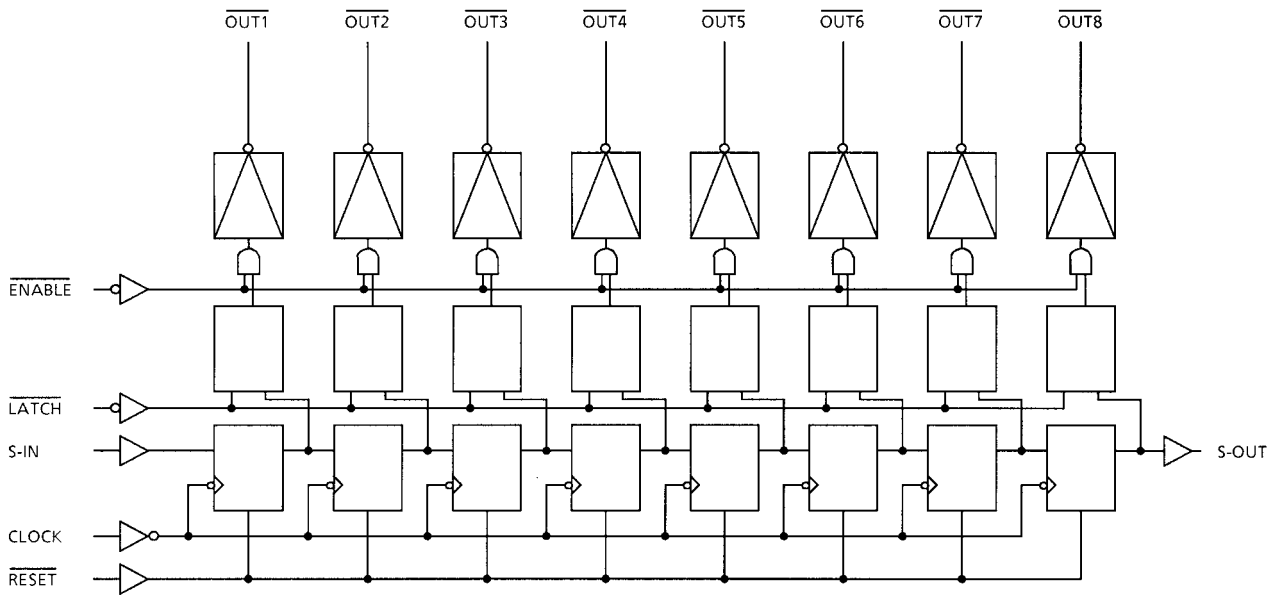
Weight: 0.32 g (Typ.)

Note: S-OUT pin is sensitive against Latch-up. (Latch-up performance is under 30 mA)
Please connect an external resistor to S-OUT pin in series due to protect this device from Latch-up. (Recommended resistance: R = 100 [Ω])

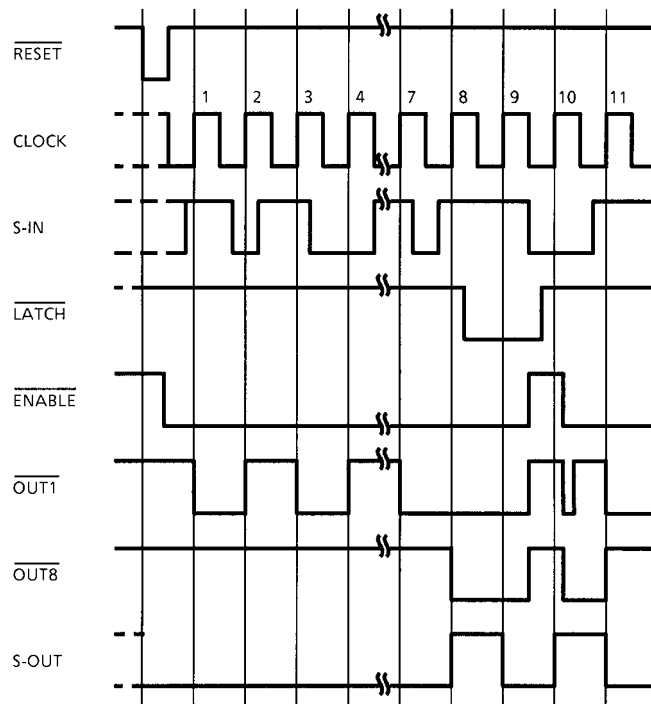
PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

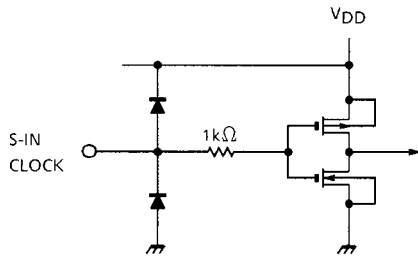


TIMING DIAGRAM

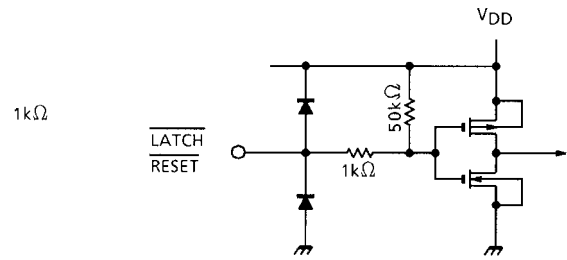


EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS

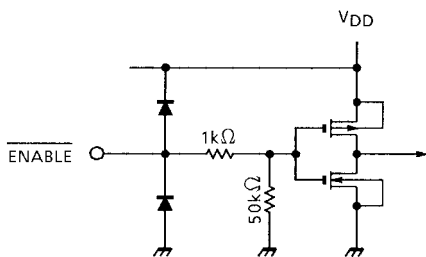
S-IN, CLOCK terminal equivalent circuits



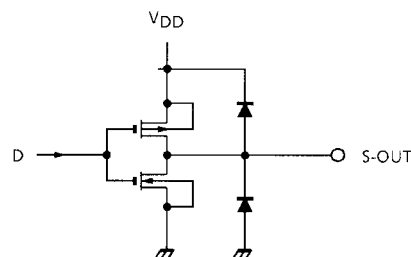
LATCH, RESET terminal equivalent circuits



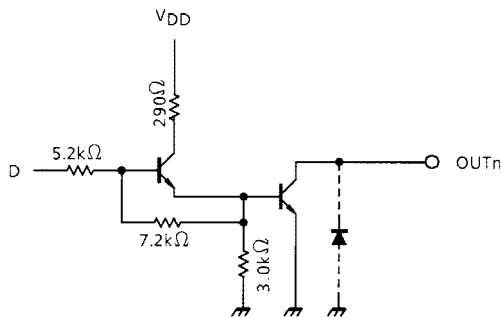
ENABLE terminal equivalent circuits



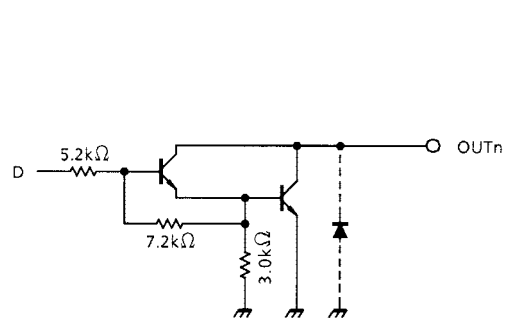
S-OUT terminal equivalent circuits



Output terminal equivalent circuits (TD62C853F)



Output terminal equivalent circuits (TD62C854F)



Note: The output parasitic diode cannot be used as clamp diode.

TRUTH TABLE

CK	\bar{E}	\bar{R}	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT
					$\bar{O}1$	$\bar{O}n$	
	L	H	H	L	OFF	$\overline{O}n-1$	Q ₇
	L	H	H	H	ON	$\overline{O}n-1$	Q ₇
	L	H	L	(*)	NC	NC	Q ₇
	H	H	(*)	(*)	OFF	NC	Q ₇
	(*)	(*)	(*)	(*)	NC	NC	Q ₇
(*)	(*)	L	H	(*)	OFF	OFF	L
(*)	H		L	(*)	NC	NC	L

<p>CK = CLOCK E = ENABLE R = RESET LATCH = LATCH S-IN = SERIAL IN OUT = PARALLEL OUT S-OUT = SERIAL OUT</p>	<p>(*) = DON'T CARE NC = NO CHANGE L = LOW LEVEL H = HIGH LEVEL</p>
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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Output Sustaining Voltage	V _{CE (SUS)}	-0.5~50	V
Output Current	TD62C853P	200	mA / ch
	TD62C854P	500	
Input Voltage	V _{IN}	~0.4~V _{DD} + 0.3	V
Power Dissipation	P _D	830 (Note)	mW
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

Note: On PCB (50 × 50 × 1.6 mm Cu 30% Glass Epoxy PCB)
The derating factor above Ta = 25°C: 6.6 mW / °C

PRECAUTIONS for USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.

Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.

Utmost care is necessary in the design of the output line, V_{DD} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT	
Supply Voltage		V _{DD}	—	4.5	5.0	5.5	V	
Input Voltage		V _{IN}	—	0	—	V _{DD}	V	
Output Current ("H" Level)	S-OUT	I _{OH}	Ta = 25°C	—	—	-0.4	mA	
Output Voltage ("L" Level)	$\overline{O}n$	V _{OH}	—	0	—	50	V	
Output Current ("L" Level)	S-OUT	I _{OL}	—	—	—	0.4	mA / ch	
			DC 1 circuit, Ta = 25°C	0	—	160		
	8 circuits on T _{pw} = 25 ms Ta = 85°C V _{DD} = 5.5 V		Duty = 10%	0	—	160		
			Duty = 40%	0	—	55		
	TD62C853F		$\overline{O}n$	DC 1 circuit, Ta = 25°C	0	—		360
				8 circuits on T _{pw} = 25 ms Ta = 85°C V _{DD} = 5.5 V	Duty = 10%	0		—
Duty = 50%	0	—	170					
Clock Frequency		f _{CLOCK}	—	1.5	—	—	MHz	
Clock Pulse Width		f _w CLOCK	—	0.33	—	—	μs	
Data Set Up Time		t _{setup}	—	100	—	—	ns	
Data Hold Time		t _{hold}	—	100	—	—	ns	

ELECTRICAL CHARACTERISTICS (Ta = -40~85°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT			
Input Voltage	"H" Level	V_{IH}	—	—	0.7 V_{DD}	—	—	V			
	"L" Level	V_{IL}	—	—	—	—	0.3 V_{DD}				
Input Current	"H" Level	I_{IH}	—	ENABLE, $V_{DD} = 5.5\text{ V}$ $V_{IH} = V_{DD}$	28	55	110	μA			
	"L" Level	I_{IL}	—	LATCH, RESET $V_{DD} = 5.5\text{ V}$, $V_{IL} = \text{GND}$	-55	-110	-275				
		I_{IN}	—	CLOCK, S-IN $V_{IN} = V_{CC}$ or GND	—	—	± 1.0				
Output Voltage	"H" Level	S-OUT	V_{OH}	—	$V_{DD} = 4.5\text{ V}$ $I_{OH} = -10\ \mu\text{A}$	3.9	4.1	—	V		
	"L" Level	S-OUT	V_{OL}	—	$V_{DD} = 4.5\text{ V}$	$I_{OL} = 0.8\text{ mA}$	—	0.2	0.4	V	
		$\overline{\text{On}}$				TD62C853F	$I_{OL} = 100\text{ mA}$	—	0.29		0.50
						TD62C854F	$I_{OL} = 160\text{ mA}$	—	0.39		0.65
		$I_{OL} = 250\text{ mA}$				—	1.24	1.90			
$I_{OL} = 400\text{ mA}$	—	1.54	2.30								
Output Current	"H" Level	$\overline{\text{On}}$	I_{OH}	—	$V_{DD} = 5.5\text{ V}$, $V_{OH} = 50.0\text{ V}$	—	—	100	μA		
Operating Supply Current			I_{DD1}	—	$V_{DD} = 5.5\text{ V}$ $T_a = 25^\circ\text{C}$	ENABLE = "H" $f_{CLK} = 1\text{ MHz}$ Output open DATA = 1 / 2 f_{CLK}	—	130	200	mA	
			I_{DD2}				—	2.0	5.0		
		TD62C853F	I_{DD3}				—	35	40		
		TD62C854F					—	1.0	1.4		

SWITCHING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time	Low-to-High	CK-S-OUT	t_{pLH}	—	$V_{DD} = 5.0\text{ V}, V_{IH} = 5.0\text{ V}$ $V_{IL} = 0\text{ V}, \text{Duty} = 50\%$ $R_L = \begin{cases} 300\Omega \text{ (TD62C853F)} \\ 120\Omega \text{ (TD62C854F)} \end{cases}$	—	0.40	0.65	μs
		$\overline{\text{CK}}-\overline{\text{On}}$				—	1.80	3.00	
		$\overline{\text{L}}-\overline{\text{On}}$				—	2.10	3.50	
		$\overline{\text{R}}-\overline{\text{On}}$				—	1.50	2.50	
		$\overline{\text{E}}-\overline{\text{On}}$				—	1.50	2.50	
	High-to-Low	CK-S-OUT	t_{pHL}	—		—	0.33	0.55	
		$\overline{\text{CK}}-\overline{\text{On}}$				—	0.41	0.70	
		$\overline{\text{L}}-\overline{\text{On}}$				—	0.30	0.50	
		R-S-OUT				—	0.25	0.42	
		$\overline{\text{E}}-\overline{\text{On}}$				—	0.21	0.35	
Maximum Clock Frequency			f_{MAX}	—	1.5	2.0	—	MHz	
Minimum Pulse Width	CLOCK		t_{wCK}	—	—	250	330	ns	
	$\overline{\text{LATCH}}$		t_{wL}		—	116	160		
	$\overline{\text{RESET}}$		t_{wR}		—	107	140		
Data Set Up Time			t_{setup}	—	—	30	60	ns	
Data Hold Time			t_{hold}	—	—	14	40		
Maximum Clock Rise Time			t_r	—	—	70	—	ns	
Maximum Clock Fall Time			t_f	—	—	70	—		

Fig.1 I_{OUT} - V_{CE(sat)}

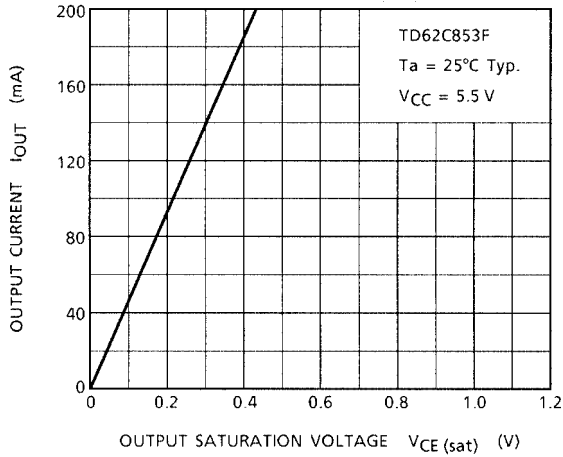
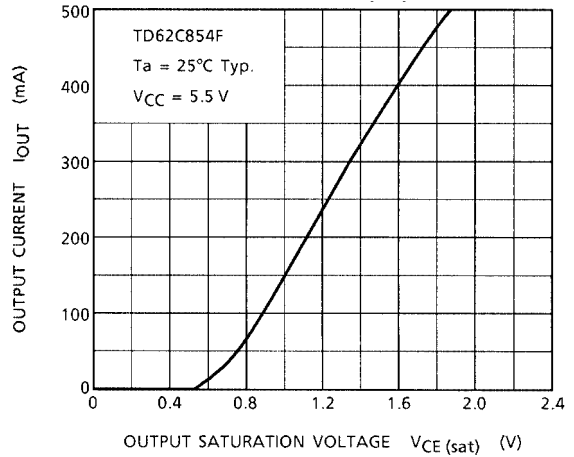


Fig.2 I_{OUT} - V_{CE(sat)}



TD62C853F each characteristic data and reference graph

Output current I_{OUT} vs lighting rate DUTY,
Condition : 1~8 circuit operation, V_{DD} = 5.5 V

Fig.3 DUTY - I_{OUT}
(Topr = 85°C)

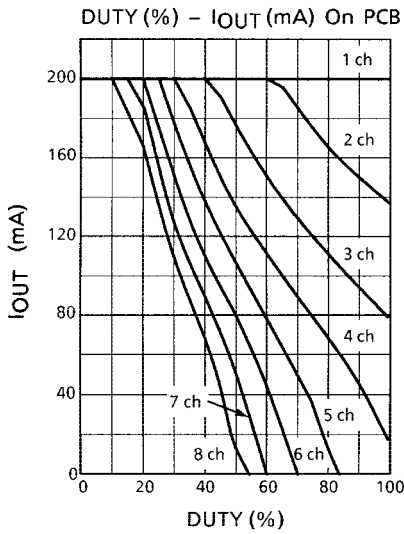


Fig.4 DUTY - I_{OUT}
(Topr = 55°C)

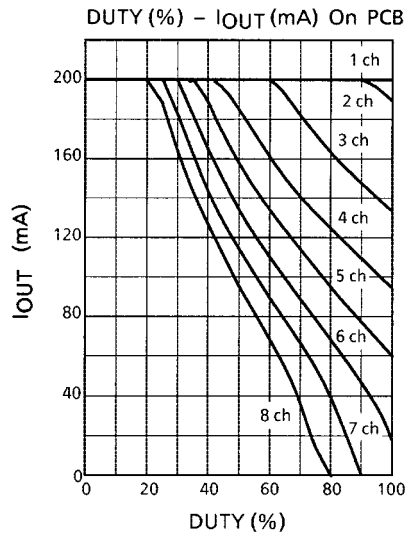
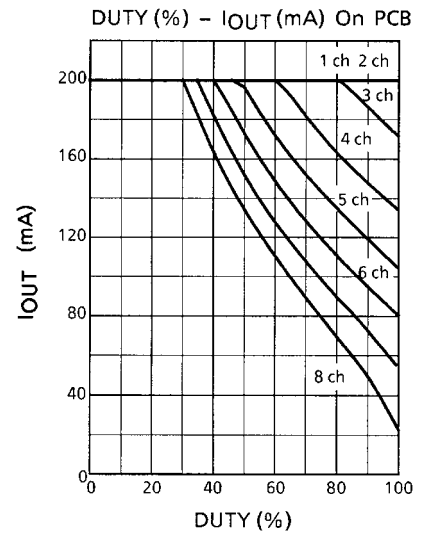


Fig.5 DUTY - I_{OUT}
(Topr = 25°C)



TD62C854F each characteristic data and reference graph

Output current I_{OUT} vs lighting rate DUTY,
 Condition: 1~8 circuit operation, $V_{DD} = 5.5\text{ V}$

Fig.6 DUTY - I_{OUT}
 ($T_{opr} = 85^\circ\text{C}$)

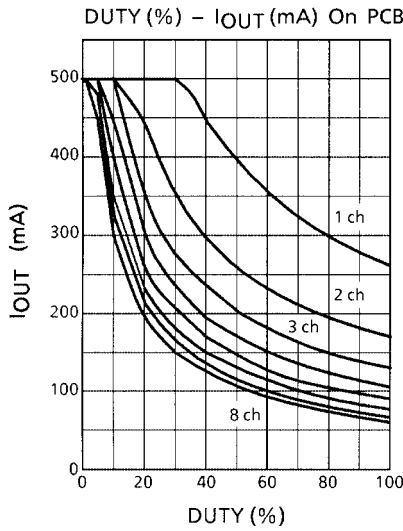


Fig.7 DUTY - I_{OUT}
 ($T_{opr} = 55^\circ\text{C}$)

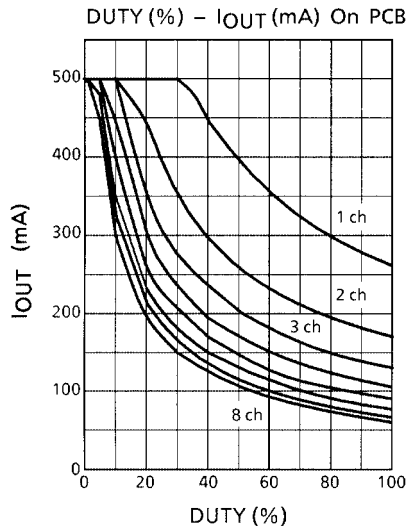
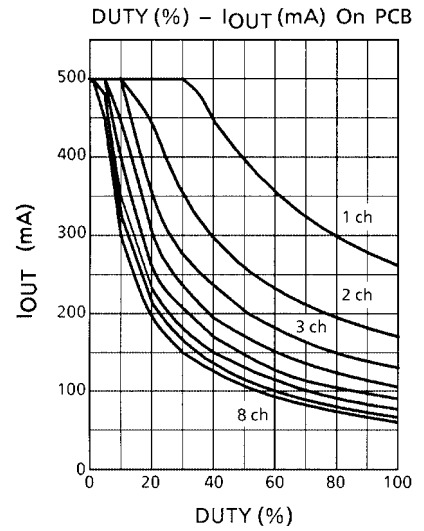
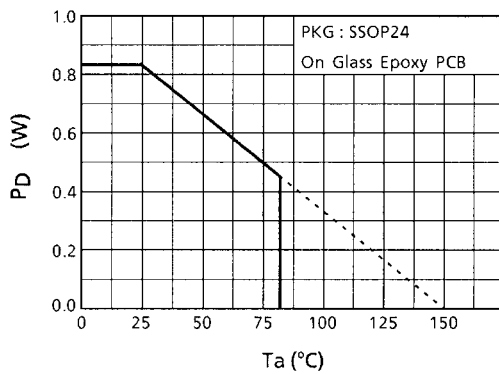


Fig.8 DUTY - I_{OUT}
 ($T_{opr} = 25^\circ\text{C}$)



SSOP24 Power dissipation

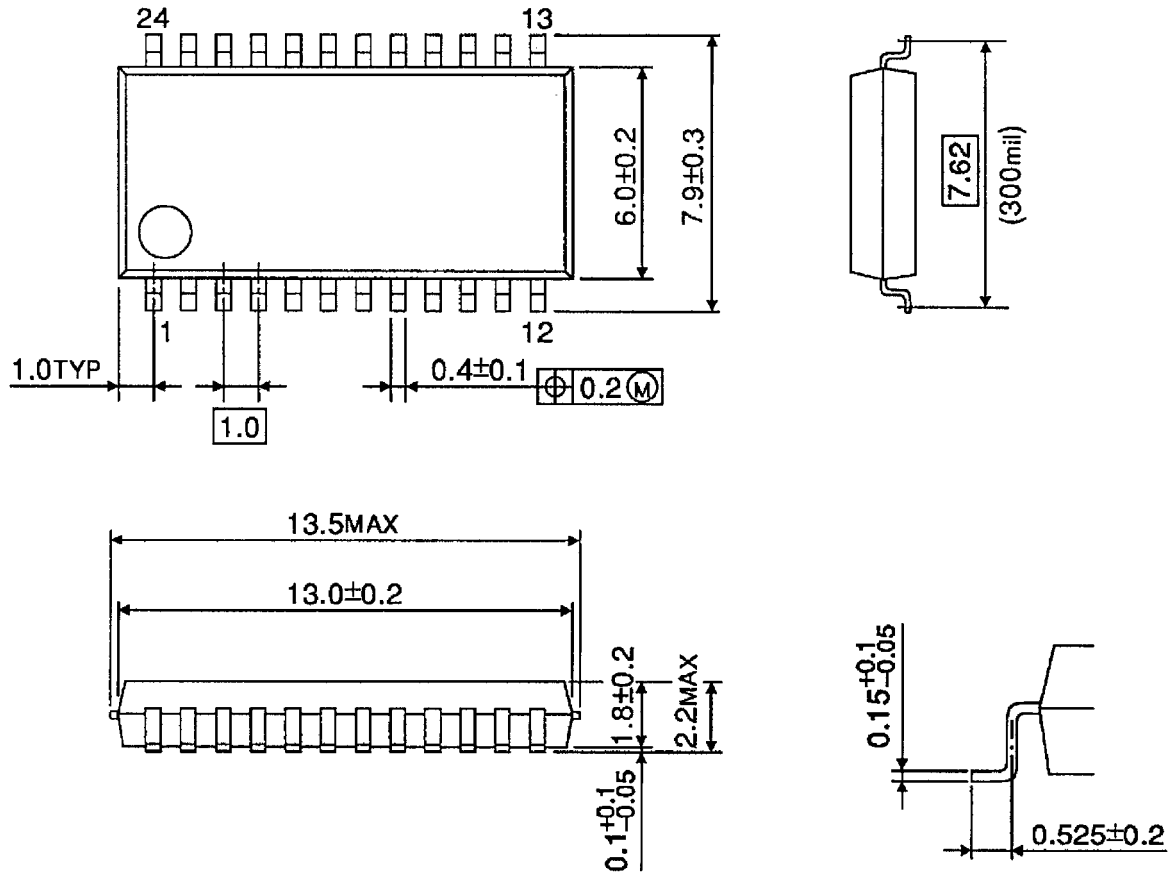
Fig.9 $P_D - T_a$



PACKAGE DIMENSIONS

SSOP24-P-300-1.00

Unit: mm



Weight: 0.32 g (Typ.)

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000707EBA

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