TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TD6336F

#### 8-BIT SERIAL-IN PARALLEL-OUT DRIVER

The TD6336F is an automotive 8-bit SI/PO driver IC using a Bi-CMOS process characterized by high output withstand voltage.

The shift registers share a common clock and a common reset signal. Data is shifted on the leading edge of the clock. The IC also has LATCH and ENABLE inputs. Its output is an N-channel open-drain output, and Isink is up to 100mA. When the supply voltage becomes low, the output turns off.



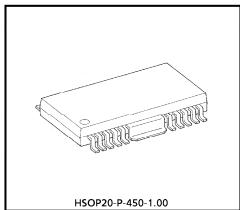
Serial input and 8-stage parallel/serial output

Serial output allows cascade expansion.

**ENABLE** input for output control

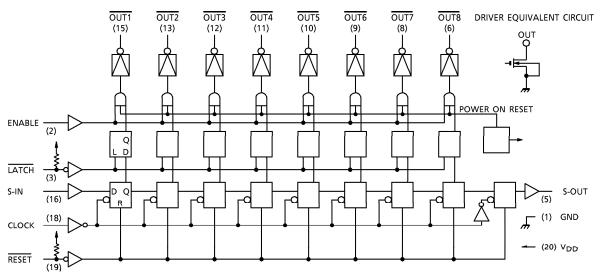
Large output current : 100mA (Max.) : 80V (Max.) High output withstand voltage

Power detection circuit incorporated: The output is disabled when  $V_{DD}$ <3V (Typ).



Weight: 0.79g (Typ.)

#### **BLOCK DIAGRAM AND PIN LAYOUT**



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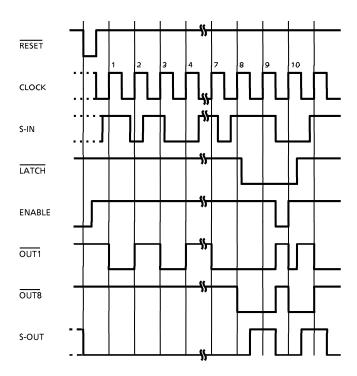
#### **PIN DESCRIPTION**

PIN No.	SYMBOL	DESCRIPTION
1	GND	Grounded. Must be connected to the FIN pin.
2	ENABLE	Data is output when this signal is high; all output buffers turn off when the signal goes low.
3	LATCH	Data is held when this signal is low; data is rewritten when the signal goes high. When the pin is open, the signal is high.
5	s-out	Serial output pin allowing easy bit addition. To prevent malfunction, this pin has a function for a half-bit delay output.
6	OUT8	Supplies shift register data or latch data. The signal is an N-channel MOS
~15	~OUT1	open-drain output.
16	S-IN	Serial data input pin.
18	CLOCK	Clock input pin for shift registers. The register acts at the leading edge of the clock.
19	RESET	Clears data in the shift registers. The shift registers do not change when this signal is high; they are reset when the signal goes low. When the pin is open, the signal is high.
20	$V_{DD}$	Power supply pin.
4, 7, 14, 17	NC	Not connected.
FIN	GND	Ground pin serving also as a heat sink. This pin must be connected to pin 1.

#### TRUTH TABLE

СК	E	R	LATCH	S-IN	Ol	OUT		
CK	<u> </u>	, n	LATCH	3-114	Q1	Qn	S-OUT	
4	Η	Н	Н	L	OFF	Qn-1	Q7	CK = CLOCK NC = NO CHANGE
4	Н	Н	Н	Н	ON	Qn-1	Q7	E = ENABLE L = LOW LEVEL
4	Н	Н	L	*	NC	NC	Q7	R = RESET H = HIGH LEVEL - S-IN = SERIAL IN
4	L	Н	*	*	NC	NC	Q7	OUT-PARALLEL OUT
ارا	*	*	*	*	NC	NC	Q7	S-OUT = SERIAL OUT
*	*	L	Н	*	OFF	OFF	L	* = DON'T CARE
*	Н		L	*	NC	NC	L	

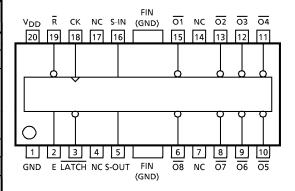
#### **TIMING CHART**



#### MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	
Supply Voltage	$V_{DD}$	-0.3~7	V	
Input Voltage	V <sub>IN</sub>	$-0.3 \sim V_{DD} + 0.3$	٧	
Output Voltage	VOUT1 (Note 1)	-0.3~V <sub>DD</sub> +0.3	٧	
Output Voltage	V <sub>OUT2</sub> (Note 2)	-0.3~80		
Output Current	lout	100	mA	
Power Dissipation	PD	1.0	W	
Storage Temperature	T <sub>stg</sub>	<b>- 55∼150</b>	°C	
Lead Temperature-time	T <sub>sol</sub>	260 (10s)	°C	

#### **PIN CONFIGURATION**



(Note 1) S-OUT (Note 2) OUT1∼OUT8

### **RECOMMENDED OPERATING CONDITIONS** (Ta = $-40 \sim 105$ °C)

CHARACT	ERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage			$V_{ m DD}$	_	_	4	5.0	6	٧	
Input Voltage			VIN	_	_	0	_	$V_{DD}$	V	
Output Current	High	S-OUT	<sup>I</sup> ОН	_	_	0	_	- 1.0	mA	
Output Voltage	High	Qn	Voн	_	_	0	_	60	٧	
Output Current	Low	Lovar	S-OUT	loL		_	0	_	1.0	mA
Output Current		Qn	loL	_	_	0	_	70	mΑ	
Clock Frequency			f clock	_	_	0	_	1.0	MHz	
Clock Pulse Wid	th		tw clock		_	500	_	_	ns	
Data Setup Time	Data Setup Time			_		500		_	ns	
Data Hold Time			<sup>t</sup> hold	_	_	500	_	_	ns	
Maximum Clock	Clock Rise Time		t <sub>r</sub>			_	_	70	μs	
Time	Fall	Time	t <sub>f</sub>			_	_	70	μs	

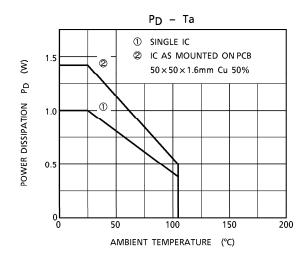
## **ELECTRICAL CHARACTERISTICS** (Ta = $-40 \sim 105$ °C, $V_{DD} = 4 \sim 6V$ )

CHARACTERISTIC			SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT										
		High	V <sub>IH</sub>	_	_	0.8 × V <sub>DD</sub>	1	ı	<b>&gt;</b>										
Input Voltage		Low	V <sub>IL</sub>			0.2 × V <sub>DD</sub>													
Input Current	R, LATCH		IN	_	$V_{IN} = 0 \sim V_{DD}$	_	_	± 100											
Input Current	CK, S-IN, E		lιΝ	_	V <sub>IN</sub> = 0~V <sub>DD</sub>	_	_	± 1	$\mu$ A										
Output Voltage	High			_	I <sub>OH</sub> = -1mA	V <sub>DD</sub> - 0.4	_	_	٧										
Output Current	High	Qn	Іон	<b>—</b>	V <sub>OH</sub> = 80V	_	_	100	μA										
Output Valtaga	Laver	Low	Lovar	Lovar	Lovar	Lovar	LOW	LOW	LOW	Low	LOW	S-OUT	$v_{OL}$	_	I <sub>OL</sub> = 1mA	_	_	0.4	V
Output Voltage	LOW	Qn	VOL	_	$Ta = 25$ °C, $I_{OL} = 100$ mA	_	_	1.2	٧										
Static Current Consumption			I <sub>DD</sub> (1)	_	$V_{DD} = 5V$ , $f = 0Hz$	_	_	1	mA										
Dynamic Current Consumption			I <sub>DD</sub> (2)	_	V <sub>DD</sub> = 5V, f = 1MHz	_	_	5	mA										

**SWITCHING CHARACTERISTICS** (Ta =  $-40 \sim 105$ °C,  $V_{DD} = 4 \sim 6V$ )

CHAR.	ISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	МАХ.	UNIT	
	High	CK-S-OUT	t <sub>pLH</sub>			_	0.1	0.5	
Dolay Timo	iligii	CK-Qn	t <sub>pLH</sub>		$R_L$ S-OUT = $2k\Omega$	_	0.5	2.5	
Delay Time	Low	CK-S-OUT	t <sub>pHL</sub>			_	0.1	0.5	$\mu$ s
		CK-Qn	t <sub>pHL</sub>		$R_L \overline{Qn} = 150\Omega$	_	0.3	1.5	
Maximum Cl	Maximum Clock Frequency				$C_L = 15pF$ $V_{IH} = 3.0V, V_{IL} = 0V$		10	_	MHz
Maximum D	Maximum Data Setup Time					_	5	25	ns
Minimum Data Hold Time			thold		Duty = 50%	_	5	25	ns
Maximum Cl	aximum Clock Rise Time		t <sub>r</sub>				70	_	,,,
Time		Fall Time	tf			_	70	_	$\mu$ \$

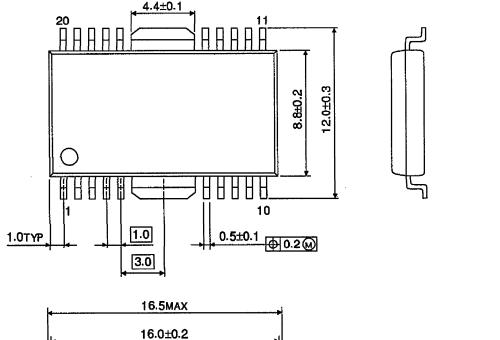
 $\mathsf{C}_{\mathsf{L}}$  : Includes the capacitances of the measuring instrument and probe.

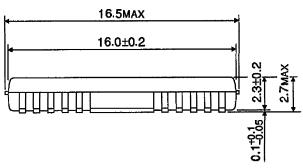


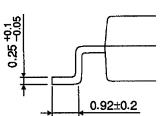
#### **OUTLINE DRAWING**

HSOP20-P-450-1.00

Unit: mm







Weight: 0.79g (Typ.)