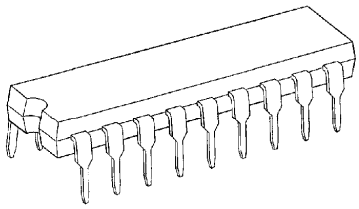
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD6338P

Bi-CMOS 10 BIT SERIAL-INPUT / PARALLEL OUTPUT DRIVER

The TD6338P is an IC built using a Bi – CMOS process characterized by high output withstand voltage. It contains a serial-input, 10-stage parallel-output shift register and latches as well as a bipolar 10-stage parallel output driver.
It also has a serial output which facilitates output expansion.



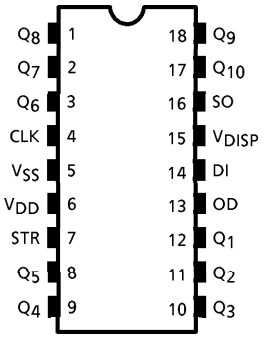
DIP18-P-300-2.54D

Weight : 1.4g (Typ.)

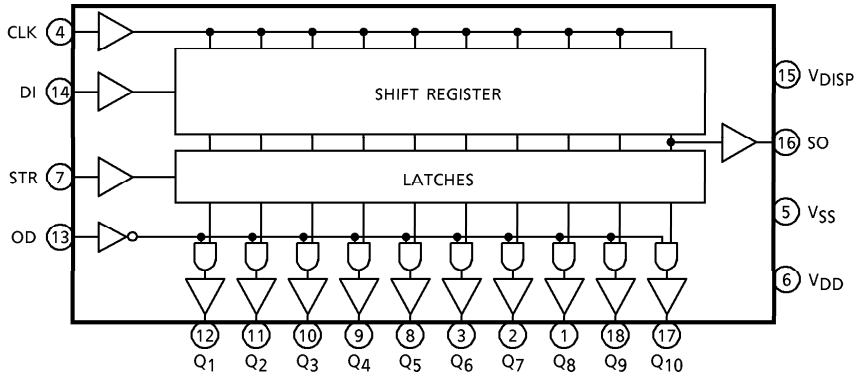
FEATURES

- Serial input and 10-stage parallel / serial output
- Serial output allows cascade expansion.
- DISABLE input for output control
- High output withstand voltage : ≧60V
- Wide operating temperature range : Ta = – 40 to 85°C

PIN LAYOUT



BLOCK DIAGRAM AND PIN LAYOUT



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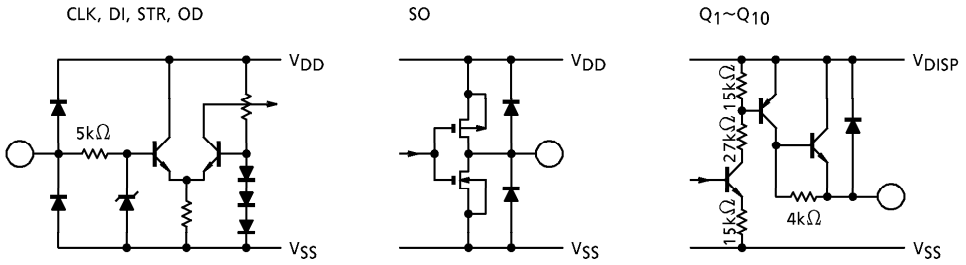
PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
12 to 8 3 to 1 18 to 17	Q_1~Q_{10}	Parallel output pins which supply shift register output when the strobe input (STR) is high and the output disable input (OD) is low.
4	CLK	Clock input pin for shift register. The shift register becomes active on the leading edge of the clock.
5	V_{SS}	Grounded.
6	V_{DD}	Power supply pin
7	STR	When this signal is low, data is held ; when it is high, data is rewritten.
13	OD	Output disable input pin. When this signal is low, data is output ; when it is high, all outputs are set low.
14	DI	Serial data input pin
15	V_{DISP}	Power supply pin for parallel output

I / O CIRCUIT DIAGRAM



OUTLINE OF FUNCTIONS

The circuit consists of a 10-stage D-type flip-flop and ten latches and buffers connected to the outputs of the flip-flop.

Suppose that data is fed to the serial data input (DI) pin and clock pulses are supplied to the clock input (CLK) pin. When the clock changes from low to high, the data enters the shift register, and the data in the shift register shifts at the same time.

Shift register data is output at the parallel output pins when the strobe input (STR) is high and the output disable input (OD) is low.

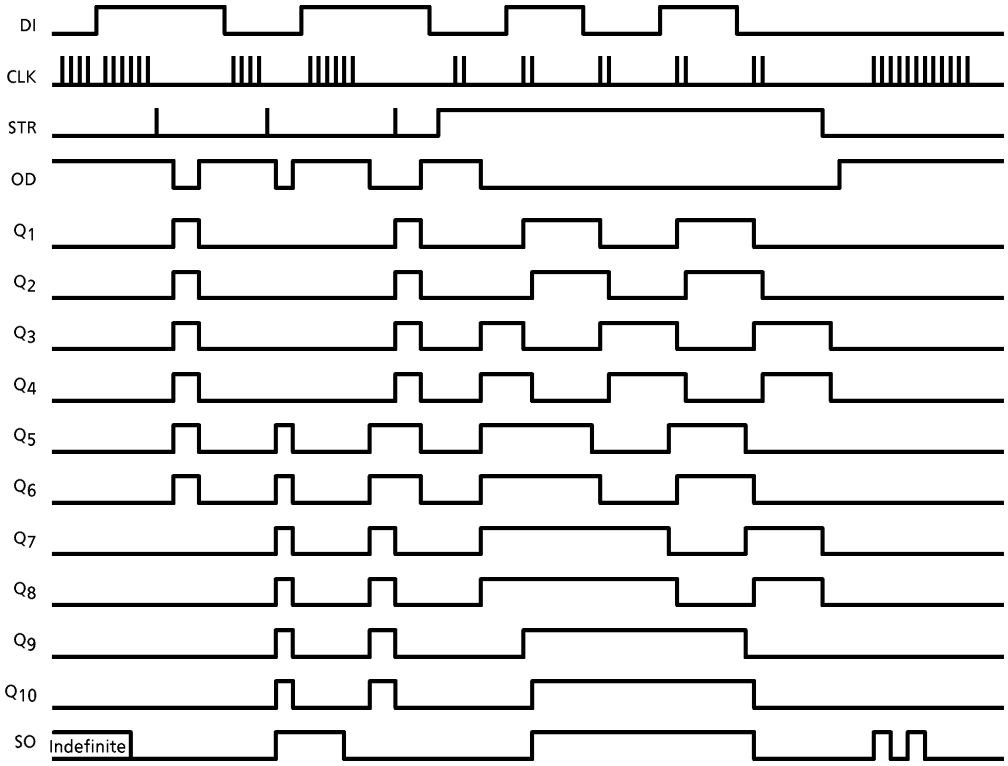
When the strobe input is set low, the contents of the latches are held regardless of the contents of the shift register.

The serial data output (SO) pin supplies a signal with the same polarity as the parallel outputs.

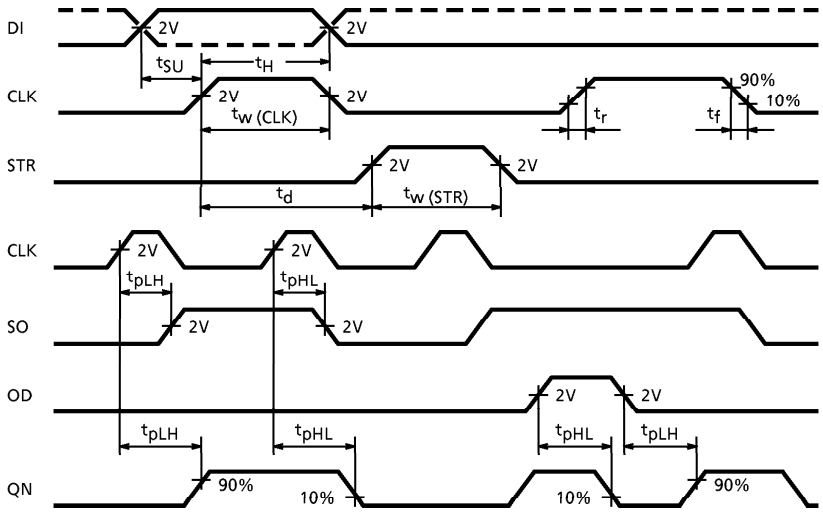
When multiple TD6338Ps are used for output expansion, the serial data output (SO) of one TD6338P is connected to the serial data input (DI) of the next-stage TD6338P.

When the output disable input (OD) is set high, the outputs Q_1 to Q_{10} become low. At the time of power-on, set the OD input high so that the outputs Q_1 to Q_{10} will be kept low until input data is set to determine the internal logic state.

TIMING CHART



VOLTAGE WAVEFORM



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING	UNIT
Display Voltage	V_{DISP}	—	65	V
Supply Voltage	V_{DD}	—	−0.3 to 15	V
Output Voltage	V_{OUT}	SO Output	−0.3 to V_{DD} + 0.3	V
		Q_1 to Q_{10} : Output off	−0.3 to V_{DISP} + 0.3	
Output Current	I_{OUT}	Q_1 to Q_{10} : Output on	−40	mA
Input Voltage	V_{IN}	—	−0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	—	1.25	W
Operating Temperature	T_{opr}	—	−40 to 85	°C
Storage Temperature	T_{stg}	—	−55 to 150	°C

RECOMMENDED CONDITIONS

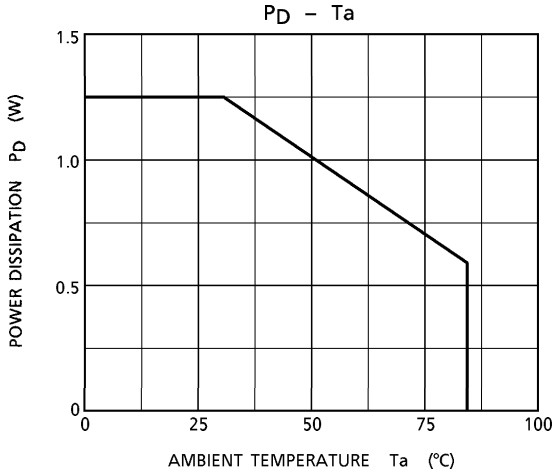
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	4	5	6	V
Output Voltage	V_O	Q_1 to Q_{10} : Output off	—	—	55	V
Output Current	I_{OUT}	Current per circuit Q_1 to Q_{10} : Output on at the same time	—	15	—	mA

DC ELECTRICAL CHARACTERISTICS (Ta = −40 to 85°C, V_{DD} = 5V, V_{DISP} = 55V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IH}	—	—	3.4	—	—	V
	V_{IL}	—	—	—	—	1.1	
Input Current	I_{IH}	—	V_{IH} = 3.4V	—	—	20	μA
	I_{IL}	—	V_{IL} = 1.1V	—	—	5	
Output Voltage	V_{OH}	—	I_{OH} = 20μA, SO	4.3	—	—	V
	V_{OL}	—	I_{OL} = 20μA, SO	—	—	0.7	
Output Current	I_{OH}	—	V_{OH} = 4.5V, SO	−100	—	—	μA
	I_{OL}	—	V_{OL} = 0.5V, SO	300	—	—	
Output Voltage	V_{OH}	—	I_{OH} = −15mA, QN	52.5	—	—	V
	V_{OL}	—	R_{OUT} = 15kΩ, QN	—	—	1.5	
Current Consumption	I_{DISP}	—	All output circuits off	—	—	6.0	mA
	I_{DD}	—	All output circuits off	—	—	10.0	

AC ELECTRICAL CHARACTERISTICS (Ta = −40 to 85°C, V_{DD} = 4 to 6V, V_{DISP} = 55V)

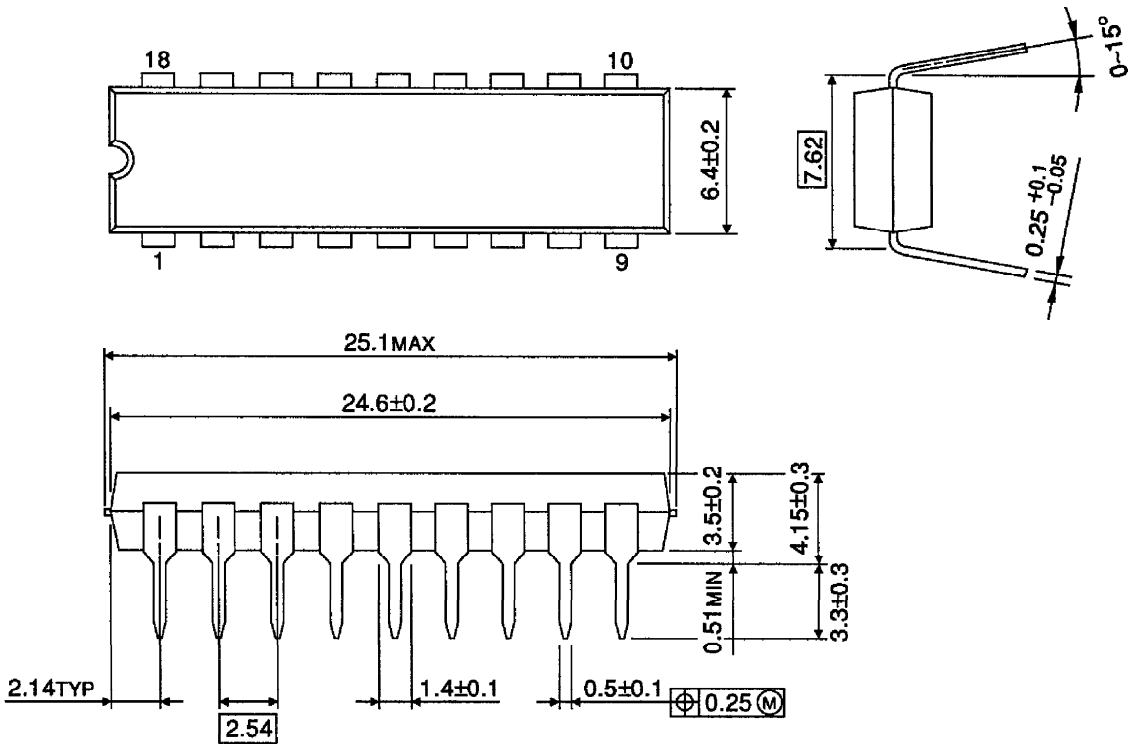
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	$f_{(CLK)}$	—	Input duty : 40 to 60%	—	—	800	kHz
Clock Pulse Width	$t_{w(CLK)}$	—	—	500	—	—	ns
Strobe Pulse Width	$t_{w(STR)}$	—	—	600	—	—	ns
Data Setup Time	t_{SU}	—	—	150	—	—	ns
Data Hold Time	t_H	—	—	400	—	—	ns
Clock Latch Time	$t_{d(CLK-STR)}$	—	—	1.5	—	—	μs
Clock Pulse Rise Time	$t_{r(CLK)}$	—	—	—	—	500	ns
Clock Pulse Fall Time	$t_{f(CLK)}$	—	—	—	—	500	ns
Transfer Delay Time	t_{pLH}	—	From input CLK to output SO	—	—	2.0	μs
	t_{pHL}		$R_{L(SO)} = \infty$, C_L = 15pF	—	—	2.0	
	t_{pLH}	—	From input CLK to output QN	—	—	3.0	
	t_{pHL}		$R_{L(QN)}$ = 2kΩ, C_L = 15pF	—	—	7.0	
	t_{pLH}	—	From input OD to output QN	—	—	6.0	
	t_{pHL}		$R_{L(QN)}$ = 2kΩ, C_L = 15pF	—	—	2.0	



OUTLINE DRAWING

DIP18-P-300-2.54D

Unit : mm



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