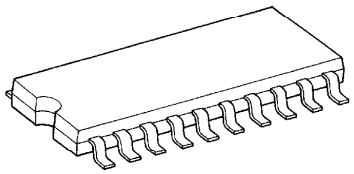
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD7614F

3-WIRE BUS, 1.3GHz-FREQUENCY SYNTHESIZER IC

FEATURES

- 3-wire bus system (software-compatible with TD6380 series).
- Built-in 4-band switch transistor.
- Built-in tuning amp (high withstanding voltage of 35V).
- Select switch can be selection of 31.25kHz, 50kHz or 62.5kHz frequency steps.
  (Selected by open, V_{CC} or GND)
- Effects on sound signal suppressed by raising reference frequency.
- Compact flat package : 20-pin FP (1.27mm pitch).
- Pin layout is mirror image of TD6380 series.



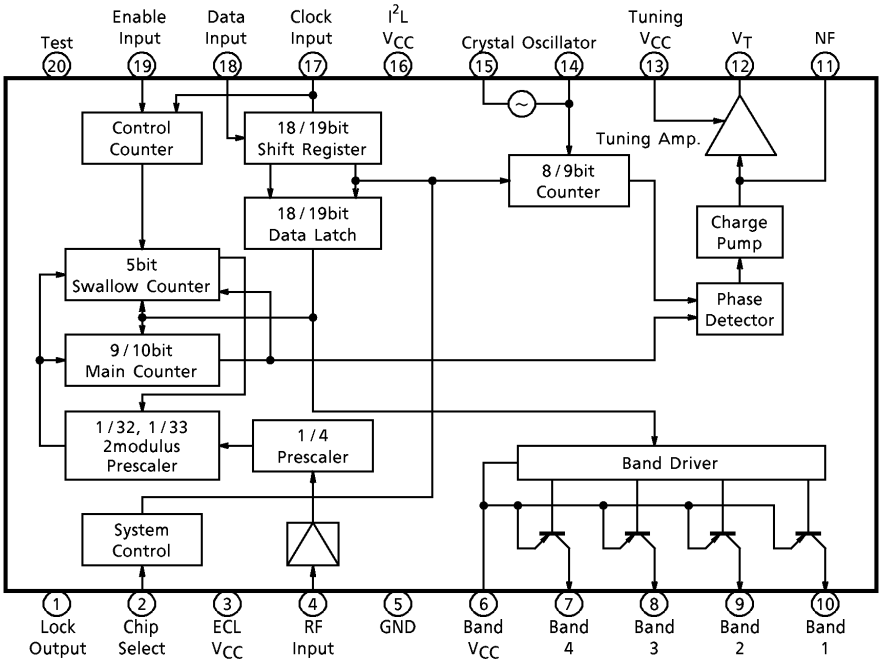
SOP20-P-300-1.27

Weight : 0.25g (Typ.)

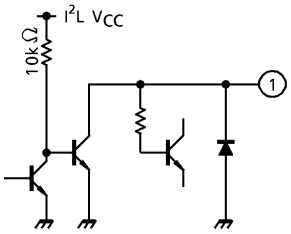
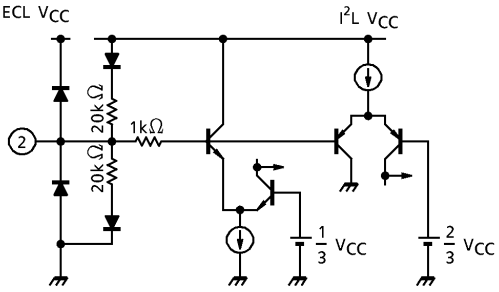
FREQUENCY STEPS	CRYSTAL OSCILLATOR	SELECT SWITCH
31.25kHz	4.0MHz	GND
50.0kHz	3.2MHz	V_{CC}
62.5kHz	4.0MHz	Open

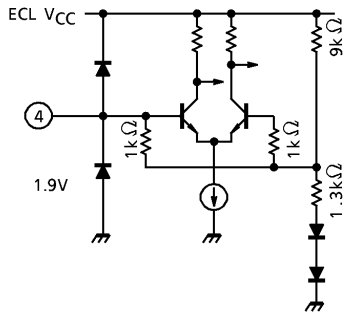
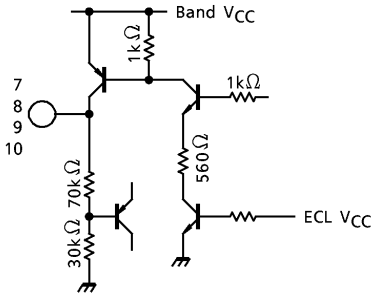
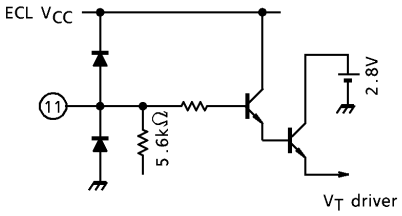
(Note) This product is susceptible to surge voltages, so should be used with extreme care.

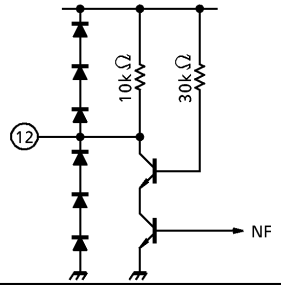
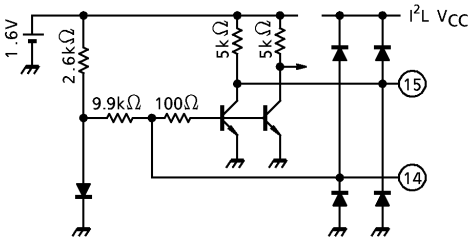
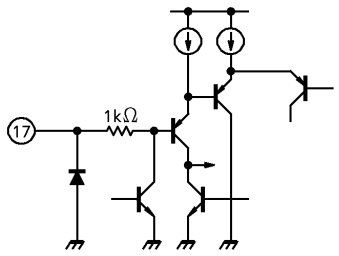
BLOCK DIAGRAM

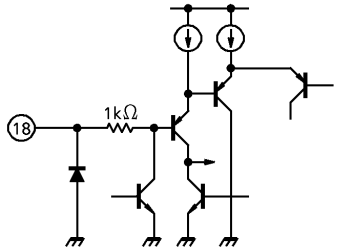
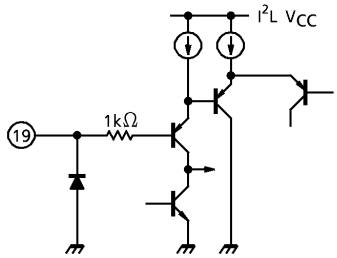
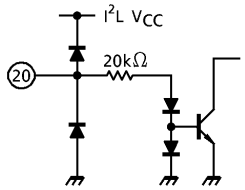


TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	$\overline{\text{Lock}}$ Output	In normal use, connecting a 5.1kΩ pull-up resistor to V_{CC} sets this output to low level when the phase-locked loop (PLL) is locked. When the phase error of phase comparator continues less than 2μs and more than three cycles, the loop is regarded as locked. In test modes, this terminal switches test mode 1 or 2. In test mode 3, this pin functions as an output pin for the frequency divided (1 / 128) by the prescaler. When measuring the input sensitivity of the prescaler, connect a 1kΩ pull-up resistor to the 0.4V power supply. The incoming current fluctuates the internal GND therefore avoid the apparent drop in input sensitivity.	
2	Chip Select	The internal reference frequency varies depending on the voltage applied. There are two internal thresholds ; 1 / 3 V_{CC} and 2 / 3 V_{CC}. With open, the internal bias becomes 1 / 2 V_{CC}. The frequency steps are as follows. Open : 4.0MHz ÷ 2^8 × 4 = 62.5kHz GND : 4.0MHz ÷ 2^9 × 4 = 31.25kHz V_{CC} : 3.2MHz ÷ 2^8 × 4 = 50.0kHz	
3	ECL V_{CC}	This teminal supplies current to the prescaler. Connect a capacitor to reduce impedance and thus eliminate power supply ripples.	—

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
4	RF Input	Unlike current ICs, this IC has no reference terminal for input. Therefore, the GND and V_{CC} impedance must be reduced sufficiently to suppress input terminal bias fluctuation due to interference.	
5	GND	Since the current for all blocks flows out of GND, be sure to make the pattern line as wide and short as possible, and certain to connect a capacitor to the power supply line.	—
6	Band V_{CC}	Due to the structure of the band driver circuit, use a voltage of between 8V and 14V.	—
7	Band 4	Can be driven at up to maximum 50mA per band. The voltage drop is below 0.15V (when V_{CC} is 12V). Do not drive more than 2 bands simultaneously because of heat due to power consumption. These terminals are built in overcurrent protection circuits. When the terminal voltage drops below 4.5V, the internal comparator is activated and driving stops. This mode continues until the terminal is no longer overloaded.	
8	Band 3		
9	Band 2		
10	Band 1		
11	NF	This terminal provides negative feedback for the active filter. The filtered current is amplified by the Darlington transistor then passed to the tuning amp.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
12	V_T	This terminal is for high-withstanding-voltage tuning amp output. There is no output voltage drop when V_{CC} = 33V is applied.	
13	Tuning V_{CC}	This terminal supplies current to the 30V tuning amp. Connect a capacitor between this terminal and GND.	—
14 15	Crystal Oscillator	These are crystal oscillator terminals used to generate the reference signal. The circuit consists of an inverter amp with a transistor. Since the reference signal is transmitted forward from the base of the transistor, when the reference signal is derived from other than the crystal oscillator, connect them to pin 14. Pin 15 is not used.	
16	I^2L V_{CC}	This terminal supplies current to the logic. Connect a capacitor between this terminal and GND.	—
17	Clock Input	In normal use, this terminal is used to input clock pulses. Since the input is received by the base of a PNP transistor, the incoming current is extremely small. In test modes 1 and 2, this terminal is used to output the reference signal obtained by dividing the crystal oscillator frequency. In test mode 3, the reference signal can be input externally, and the operation of the phase comparator can be monitored.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
18	Data Input	Input interface circuit is the same as clock pin. In test modes 1 and 2, this terminal is used for main counter output. In test mode 3, this terminal is used to input comparison signal of the phase comparator in order to compare the phase with that of the signal input from pin 17. (Data are output to the NF terminal).	
19	Enable Input	Input interface circuit is the same as clock terminal. In normal use, this terminal counts clocks from rise to fall of the enable signal. Clocks other than 18 or 19 are ignored. In the case of test mode, this terminal switches test modes.	
20	Test	Setting this terminal to low level (GND or open) results in normal tuning. Setting this terminal to high level (V_{CC} : 5V) switches mode to test mode, enabling tests 1-3.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 1	V_{CC1}	6.0	V
Supply Voltage 2	V_{CC2}	6.0	V
Supply Voltage 3	V_{CC3}	15	V
Supply Voltage 4	V_{CC4}	35	V
Power Dissipation	P_D	925	mW
Operating Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 7.4mW for each increase of 1°C.

RECOMMENDED SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
3	ECL V_{CC}	4.5	5.0	5.5	V
16	I^2L V_{CC}	4.5	5.0	5.5	V
6	Band Driver V_{CC}	8	12	13.2	V
13	Tuning V_{CC}	—	33	34	V

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 33V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1		I_{CC1}	1	ECL	20		50	mA
Supply Current 2		I_{CC2}		I^2L			25	
Supply Current 3		I_{CC3}		Turns on a band driver		55	65	
Supply Current 4		I_{CC4}				5	10	
Band Driver Drive Current		I_{BD}	1			50	55	
Band Driver Drive Voltage Drop		$V_{BD\ SAT}$	1	I_{BD} = 50mA			0.15	V
Tuning Amp Output Low-Level Voltage		V_{TOUT}	2			0.6		
Prescaler Input Sensitivity		V_{IN1}	3	f = 80~150MHz	– 20	—	3	dBmW (50Ω)
		V_{IN2}		f = 150~1000MHz	– 27	—	3	
		V_{IN3}		f = 1.0~1.3GHz	– 20	—	3	
Clock Pulse Width		T_C	2	duty = 50%	3			μs
Data Hold Time		T_H		duty = 50%	3			
Enable Set Up Time		T_L			10			
Enable Hold Time		T_{SL}			3			
Next Clock Disable Time		T_{NC}			7			
Selector Switch Threshold Voltage	High Level	V_{th} H	2		3.0	3.3	3.6	V
	Low Level	V_{th} L			1.4	1.7	2.0	
Bus Interface Pin Input Current	High Level	I_{BI} H	2	Applies to enable, data, and clock			10	μA
	Low Level	I_{BI} L		Applies to enable, data, and clock	– 20			
Bus Interface Pin Input Voltage	High Level	V_{BI} H	2	Applies to enable, data, and clock	3.0			V
	Low Level	V_{BI} L		Applies to enable, data, and clock			0.8	

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Mode Output Voltage	High Level	V_{LO} H	4	Applies to lock, data, and clock	3.0			V
	Low Level	V_{LO} L		Applies to lock, data, and clock			0.8	
Selector Switch Open Voltage		V_{th} O	2		2.2	2.5	2.8	V

TEST MODE OPERATION

Setting the test terminal (pin 20) to high level enters test modes. There are three kinds of test modes as follows :

(1) Test modes 1 and 2

Test modes 1 and 2 are used to test the PLL lock state. After data are input to the main counter and swallow counter, set the test terminal (pin 20) to high level while keeping the enable terminal (pin 19) at low level. In this state, the comparison frequency signal is output to the clock terminal (pin 17) and main counter division signal to the data terminal (pin 18). The high-frequency signal is input from the RF input terminal (pin 4).
The prescaler divider ratio can be switched by changing the voltage applied to the $\overline{\text{lock}}$ output terminal (pin 1).

Lock output (pin 1) applied voltage at high level : 1 / 4 divider ratio
Lock output (pin 1) applied voltage at low level : 1 / 1 divider ratio

(2) Test mode 3

Test mode 3 is used to test the prescaler, phase comparator, and charge pump. Setting both the test terminal (pin 20) and the enable terminal (pin 19) to high level enters test mode 3. The comparison frequency signal of phase comparator is input from the clock terminal (pin 17), the comparated frequency signal is input from the data terminal (pin 18), and the prescaler output (fixed at 1 / 128 divider ratio) is output to the lock output terminal (pin 1).

The output polarity of phase comparator is as follows.

INPUT FREQUENCY	NF OUTPUT PIN (pin 11)
Input frequency > programmed frequency	High level
Input frequency < programmed frequency	Low level

TEST MODE

PIN NAME	MODE 1	MODE 2	MODE 3
Lock output (pin 1)	High level 1 / 4	Low level 1 / 1	1 / 128
RF input (pin 4)	RF input (1 / 4 normal mode frequency input)	RF input	RF input
Clock input (pin 17)	Select switch (pin 2) Open : 15.625kHz V_{CC} : 12.5kHz GND : 7.8125kHz	Select switch (pin 2) Open : 15.625kHz V_{CC} : 12.5kHz GND : 7.8125kHz	The reference signal input of phase comparator
Data input (pin 18)	Main counter output	Main counter output	The comparated frequency signal input of phase comparator
Enable input (pin 19)	Low level	Low level	High level
Test (pin 20)	High level	High level	High level

TIMING OF DATA INPUT

The method of inputting data will be indicated in the diagram 1.

COMPUTATION OF LOCK FREQUENCY

Lock frequency is calculated as follows :

$$f_{OSC} = f_r \times 4 \times (32M + S)$$

f_{OSC} : The oscillation frequency of VCO (the input frequency signal of a prescaler)

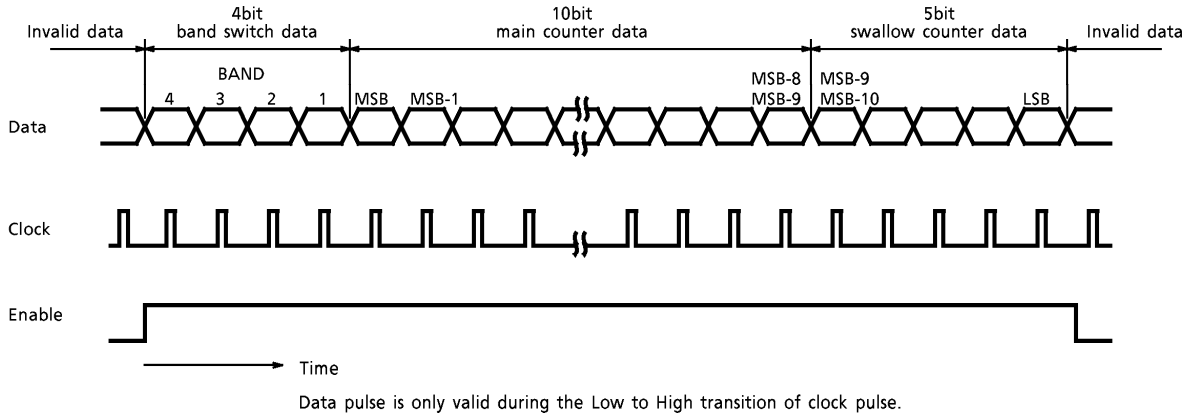
f_r : Reference frequency : it will be $1/2^8$ or $1/2^9$ of the oscillation frequency of a crystal oscillator.

M : Preset value of Main counter.

S : Preset value of Swallow counter.

SELECTION (Pin 2) / ITEM	OPEN	V_{CC}	GND
Main Counter	9bit	10bit	10bit
Swallow Counter	5bit	5bit	5bit
Reference Frequency	15.625kHz 4MHz / 2^8	12.5kHz 3.2MHz / 2^8	7.8125kHz 4MHz / 2^9
Frequency Step	62.5kHz	50kHz	31.25kHz

Fig.1 Normal use



Data pulse is only valid during the Low to High transition of clock pulse.

Fig.2 Test mode (mode 1, 2)

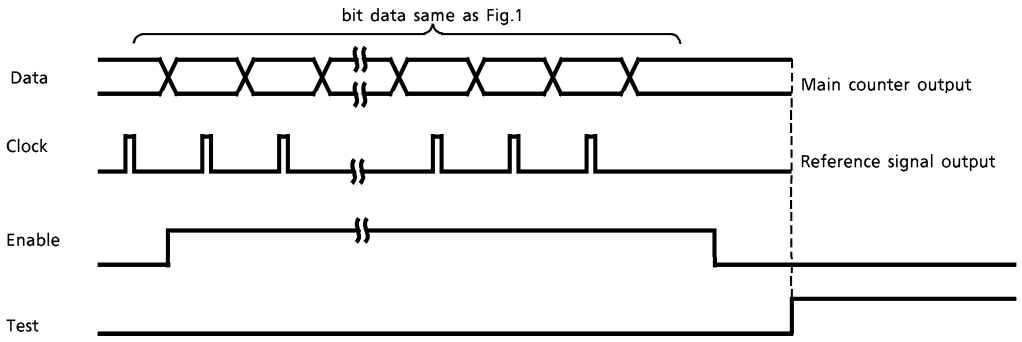
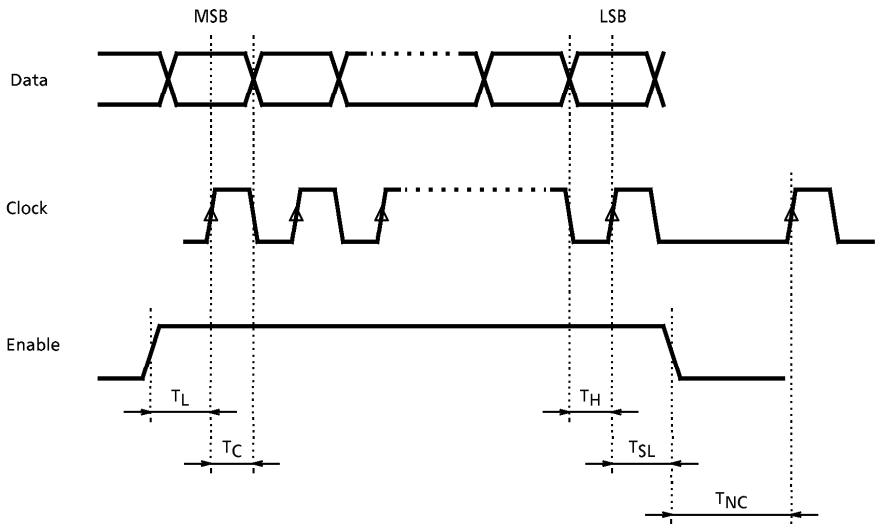
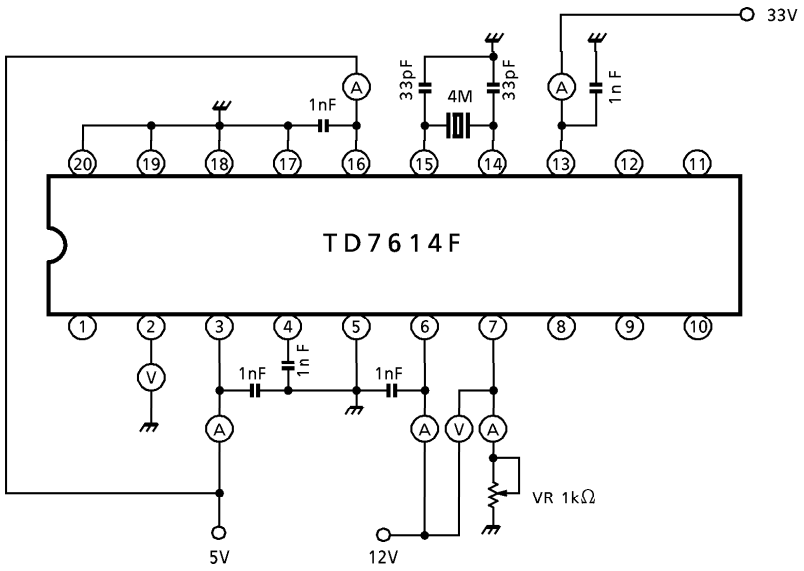


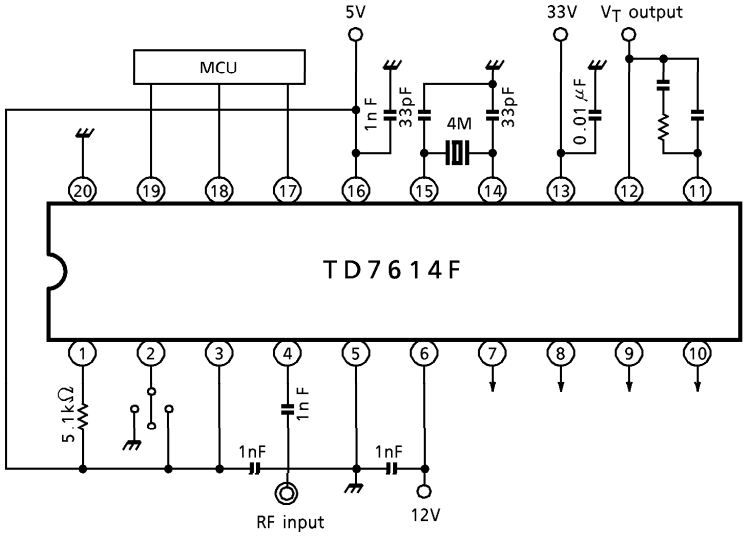
Fig.3 Timing chart of 3 wire-bus (rising timing)



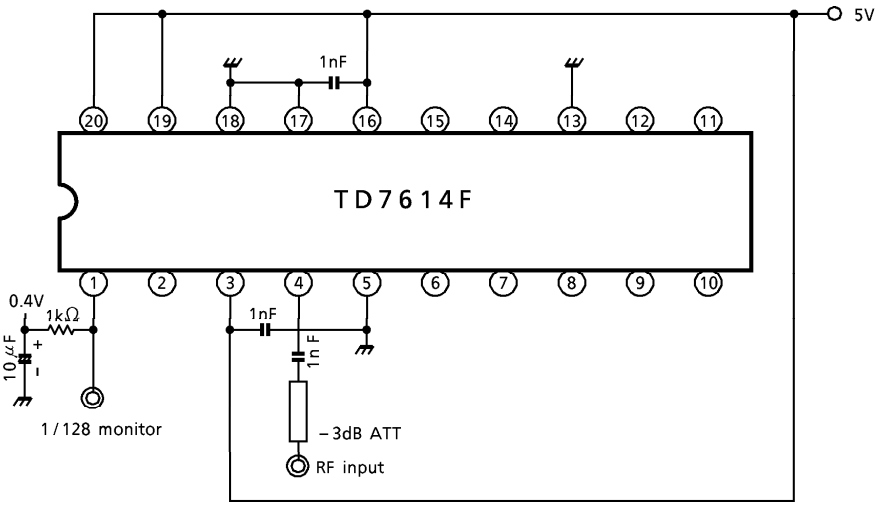
TEST CIRCUIT 1. Supply test circuit



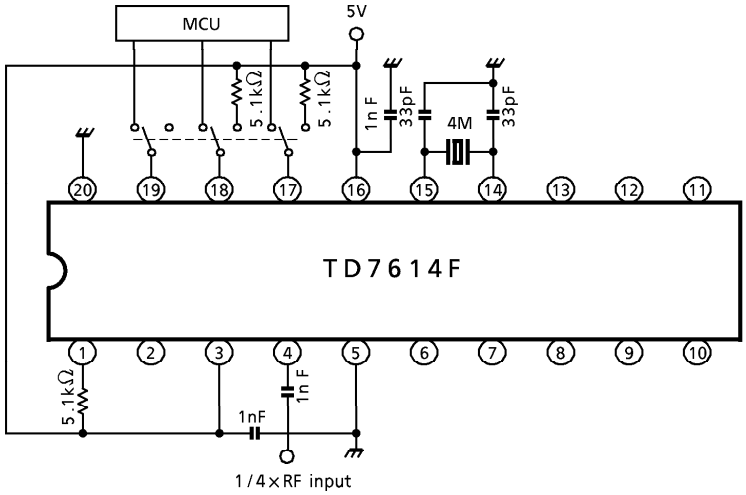
TEST CIRCUIT 2. AC operating test circuit

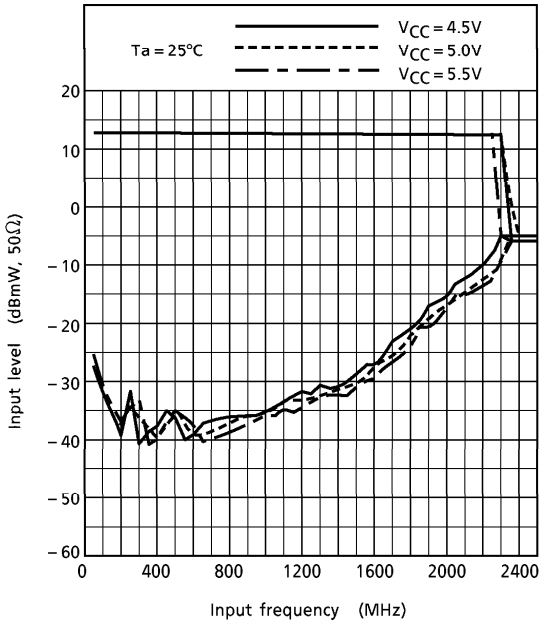


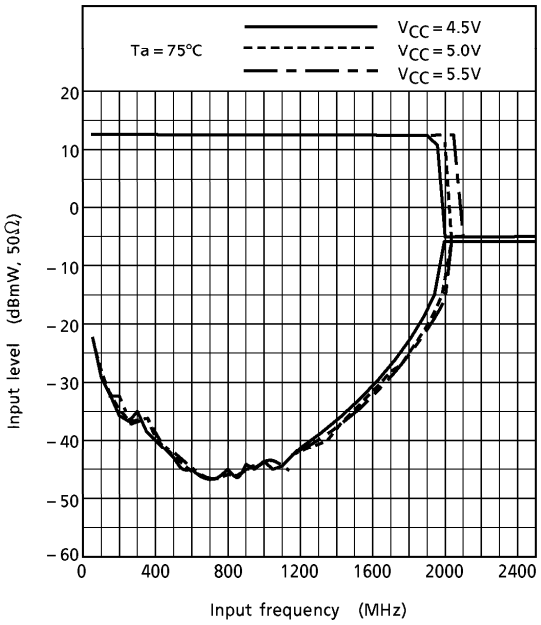
TEST CIRCUIT 3. Input sensitivity test circuit

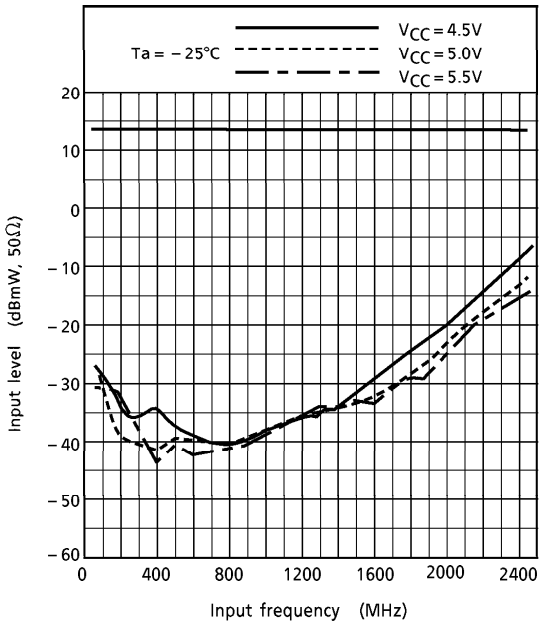


TEST CIRCUIT 4. Output mode test circuit

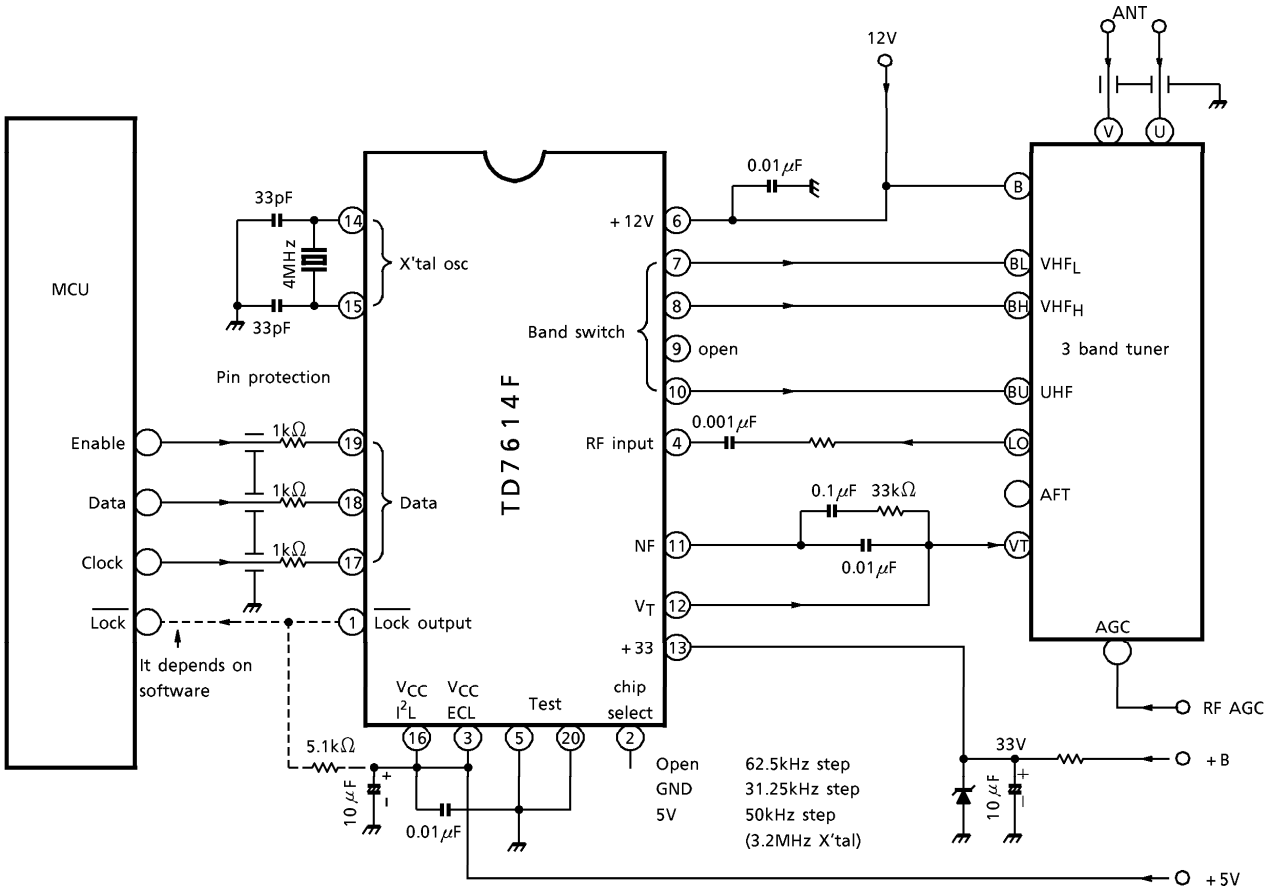



Ta = 25°C
VCC = 4.5V
VCC = 5.0V
VCC = 5.5V
Input level (dBmW, 50Ω)
20
10
0
−10
−20
−30
−40
−50
−60
0
400
800
1200
1600
2000
2400
Input frequency (MHz)


Ta = 75°C
VCC = 4.5V
VCC = 5.0V
VCC = 5.5V
Input level (dBmW, 50Ω)
20
10
0
−10
−20
−30
−40
−50
−60
0
400
800
1200
1600
2000
2400
Input frequency (MHz)


Ta = −25°C
VCC = 4.5V
VCC = 5.0V
VCC = 5.5V
Input level (dBmW, 50Ω)
20
10
0
−10
−20
−30
−40
−50
−60
0
400
800
1200
1600
2000
2400
Input frequency (MHz)

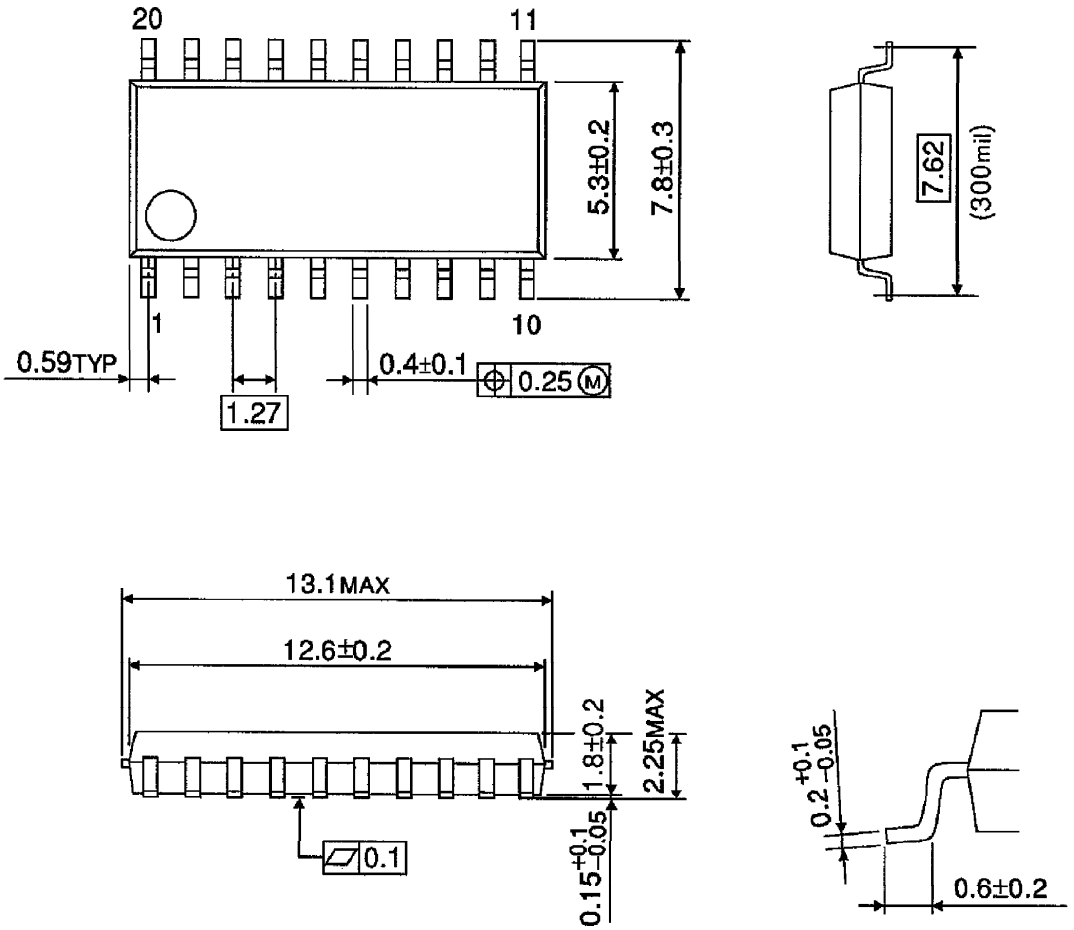
APPLICATION CIRCUIT EXAMPLE OF FREQUENCY SYNTHESIZER



OUTLINE DRAWING

SOP20-P-300-1.27

Unit : mm



Weight : 0.25g (Typ.)