OPERATIONAL AMPLIFIER

The TDA0741D is a silicon monolithic integrated operational amplifier intended for use in hybrid modules and applications where small outline dimensions are important.

Features:

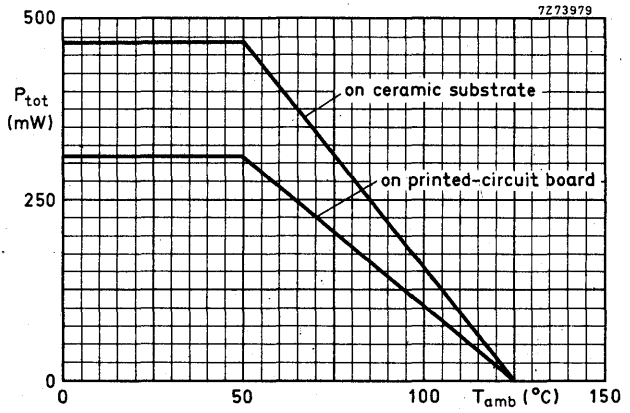
- no frequency compensation required
- short-circuit protection
- large input and output voltage range
- offset voltage adjustable to zero

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain at R_L = 2 kΩ; V_o = ±10 V	G_v	typ.	200 000	
Common mode rejection ratio	CMRR	typ.	90	dB
Differential input resistance	R_i	typ.	2	MΩ
Output voltage swing at R_L = 10 kΩ	V_o	>	±12	V
Input voltage range	V_i	>	±12	V

PACKAGE OUTLINE SOT-96A (plastic 8-lead flat pack) (see general section).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

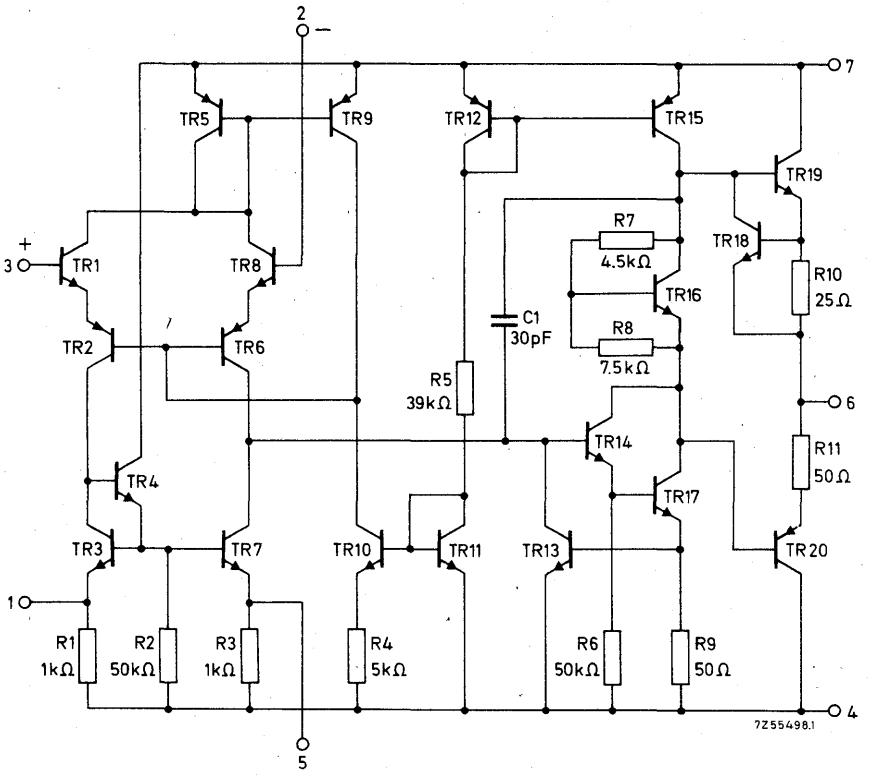
Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	$-V_N$	max.	18	V
Common mode input voltage [1]	V_i	max.	±15	V
Differential input voltage	V_{2-3}	max.	±30	V
Power dissipation (see derating curve below)				
Total power dissipation (free air, T_{amb} = 50 °C)				
mounted on a ceramic substrate (4 cm^2)	P_{tot}	max.	470	mW
mounted on printed-circuit board (4 cm^2)	P_{tot}	max.	310	mW
Output short-circuit duration [2]	indefinite			
Temperatures				
Operating ambient temperature see derating curve below	T_{amb}	−25 to	+85	°C
Storage temperature	T_{stg}	−65 to	+125	°C



[1]) For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

[2]) Continuous short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

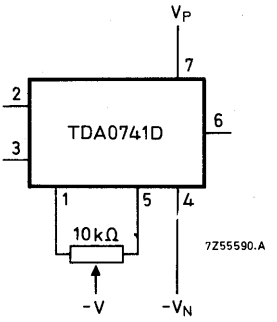


CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 25 °C unless otherwise specified

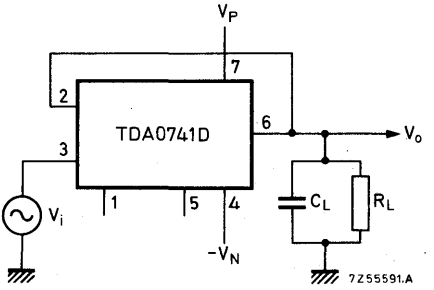
Input offset voltage	V_{io}	typ. 	2 6	mV mV
Input bias current	I_i	typ. 	80 500	nA nA
Input offset current	I_{io}	typ. 	20 200	nA nA
Input voltage range	V_i	> typ.	±12 ±13	V V
Common mode rejection ratio	CMRR	> typ.	70 90	dB dB
Differential input resistance	R_i	> typ.	0,3 2,0	MΩ MΩ
Power supply voltage rejection ratio	PSRR	typ. 	30 150	μV/V μV/V
Voltage gain at R_L = 2 kΩ; V_o = ±10 V	G_v	> typ.	20 000 200 000	
Output voltage swing at R_L = 2 kΩ	V_o	> typ.	±10 ±13	V V
at R_L = 10 kΩ	V_o	> typ.	±12 ±13	V V
Output resistance at f = 1 kHz	R_o	typ.	60	Ω
Output short-circuit current	I_{sc}	typ.	25	mA
Supply current at I_o = 0	$I_{P;N}$	typ. 	1,7 2,8	mA mA
Transient response (unity gain; voltage follower) V_i = 20 mV; R_L = 2 kΩ; C_L = 100 pF Rise time Overshoot		 typ. typ.	 0,3 5	 μs %
Slew rate (unity gain) at R_L = 2 kΩ	S	typ.	0,5	V/μs

CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 0 to 70 °C unless otherwise specified

Voltage gain at R_L = 2 kΩ; V_o = ±10V	G_v	>	15 000	
Input offset voltage	V_{io}	<	7,5	mV
Input bias current	I_i	<	0,8	μA
Input offset current	I_{io}	<	0,3	μA
Output voltage swing at R_L = 2 kΩ	V_o	>	±10	V
		typ.	±13	V



Offset voltage zeroing circuit



Transient response test circuit