

High-speed single sample-and-hold amplifier

TDA1535B

GENERAL DESCRIPTION

The TDA1535B is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

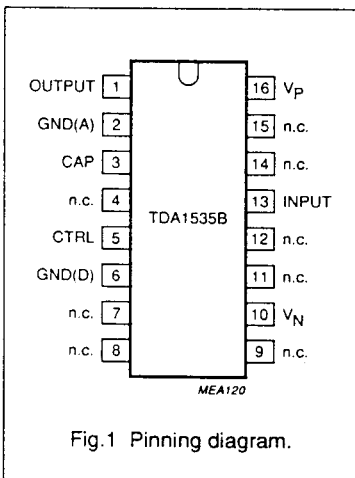
The excellent performance of the circuit makes it suitable for data acquisition systems with resolution up to 16 bits. The control input is TTL compatible.

FEATURES

- High-speed: fast acquisition, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Low noise: low total harmonic distortion and high signal-to-noise ratio
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a single Sample-and-Hold circuit. The several parts of the diagram will be described in the next sections.



QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------|---------------------------------------|------|---------------|------|---------|
| V _P | positive supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _N | negative supply voltage | -5.5 | -5.0 | -4.5 | V |
| THD | total harmonic distortion | - | -100 0.001 | - | dB % |
| S/N | signal-to-noise ratio | - | 110 | - | dB |
| t _{ac} | acquisition time to 0.001% (8 V step) | - | 2 | - | μs |
| t _{av} | aperture uncertainty | - | 0.1 | - | ns |
| B | small signal bandwidth | - | 2 | - | MHz |
| V _{SHO} | sample-to-hold offset step | - | 2 | - | mV |
| dV/dt | droop rate | - | 40 | - | mV/s |
| t _{sh} | hold-mode settling time | - | 1 | - | μs |
| P _{tot} | total power dissipation | - | 225 | - | mW |
| T _{amb} | operating ambient temperature range | -30 | - | +85 | °C |

ORDERING AND PACKAGE INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|----------------------|---------|--------------|----------|-------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA1535B | 16 | DIL | plastic | SOT38 |

PINNING

| SYMBOL | PIN | DESCRIPTION |
|----------------|-----|-------------------------|
| OUTPUT | 1 | output |
| GND(A) | 2 | analog ground |
| CAP | 3 | S/H capacitor |
| n.c. | 4 | not connected |
| CTRL | 5 | S/H control |
| GND(D) | 6 | digital ground |
| n.c. | 7 | not connected |
| n.c. | 8 | not connected |
| n.c. | 9 | not connected |
| V _N | 10 | negative supply voltage |
| n.c. | 11 | not connected |
| n.c. | 12 | not connected |
| INPUT | 13 | input |
| n.c. | 14 | not connected |
| n.c. | 15 | not connected |
| V _P | 16 | positive supply voltage |

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Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 V_{tt}, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of a current source circuit which contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has its + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

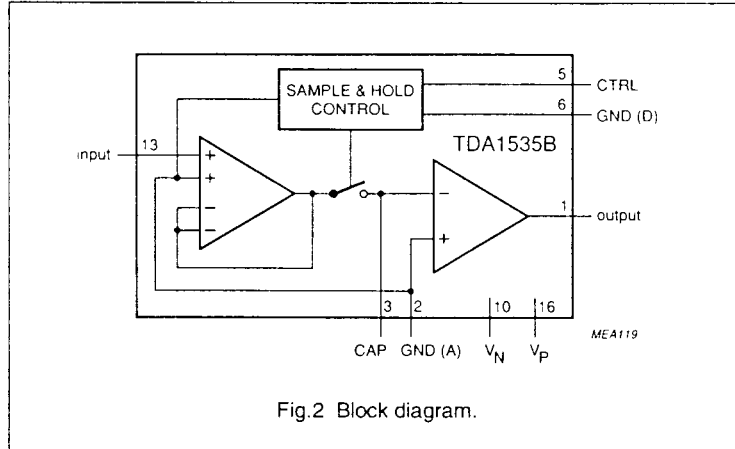


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|-------------------------------------|------------|-------|-------|------|
| V _P | positive supply voltage | | - | 6 | V |
| V _N | negative supply voltage | | -6 | - | V |
| T _{stg} | storage temperature range | | -55 | +150 | °C |
| T _{amb} | operating ambient temperature range | | -30 | +85 | °C |
| V _{es} | electrostatic handling | see note 1 | -2000 | +2000 | V |

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

| SYMBOL | PARAMETER | MAX. | UNIT |
|---------------------|--------------------------|------|------|
| R _{th j-a} | from junction-to-ambient | 75 | K/W |

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Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is

achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than -100 dB for input

frequencies up to 20 kHz and output voltages up to 8 Vt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned in the above sections in the correct timing order. The supply is taken from the 'V_p' pin via an on-chip separate supply line.

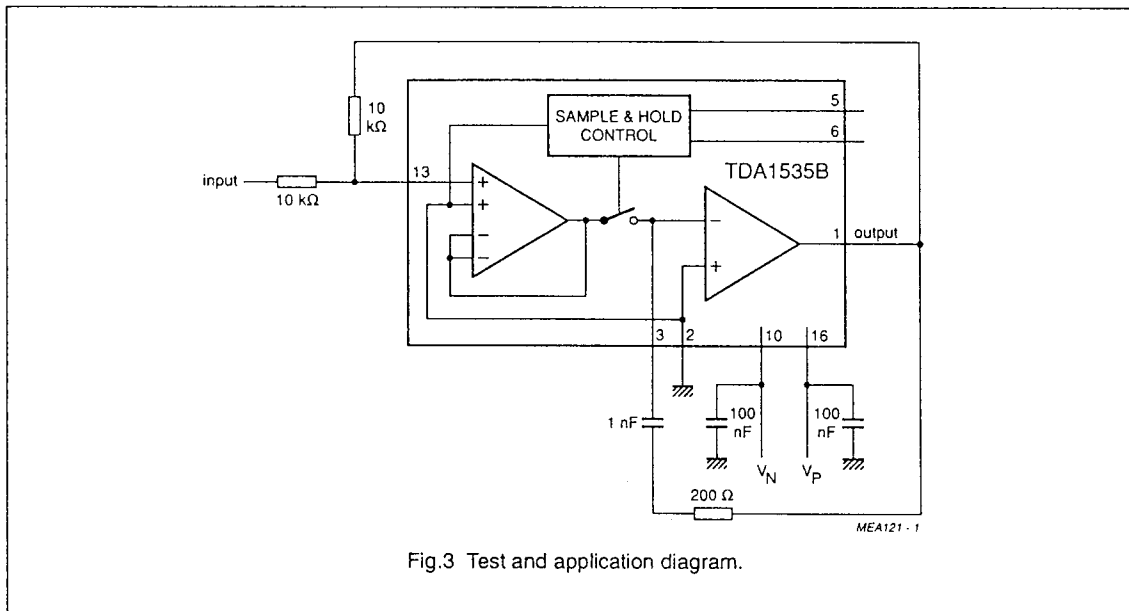


Fig.3 Test and application diagram.

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CHARACTERISTICS
 $V_P = +5\text{ V}$; $T_{\text{amb}} = +25\text{ }^\circ\text{C}$, unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------------------------|----------------------------------------------|--------------------------------|------|------|-------|---------------|
| Supply | | | | | | |
| V_P | positive supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_N | negative supply voltage | | -5.5 | -5.0 | -4.5 | V |
| I_P | positive supply current | | - | 22 | - | mA |
| I_N | negative supply current | | - | -23 | - | mA |
| P_{tot} | total power dissipation | | - | 225 | - | mW |
| Input/Output | | | | | | |
| A_v | gain | note 2 | - | -1 | - | V/V |
| V_i | input voltage (RMS value) | | - | - | 2.82 | V |
| Sample mode | | | | | | |
| THD | total harmonic distortion | notes 1,2,3 | - | -100 | - | dB |
| SNR | S/N ratio | notes 1,2,3 | - | 110 | - | dB |
| B | small signal band width | | - | 2 | - | MHz |
| Sample/hold mode | | | | | | |
| t_{ad} | aperture delay time | see Fig.4 | - | 100 | - | ns |
| t_{av} | aperture uncertainty (RMS) | see Fig.4 | 0 | 0.1 | 0.2 | ns |
| V_{SHO} | sample-to-hold (pedestal) | see Fig.4 | - | 2 | - | mV |
| dV/dt | offset step droop rate | see Fig.4 | - | 40 | - | mV/s |
| t_{ac} | acquisition time to 0.001% | see Fig.4 | - | 2 | - | μs |
| t_{se} | hold-mode settling time | see Fig.4 | - | 1 | - | μs |
| THDF | total harmonic distortion functional | notes 1,4 | - | -100 | -96 | dB |
| Supply voltage ripple rejection | | | | | | |
| SVRR | | note 5 | - | 80 | - | dB |
| SVRR | | note 5 | 55 | 80 | - | dB |
| Digital inputs | | | | | | |
| V_{IH} | digital input voltage, hold mode (logic 1) | | 2 | - | V_P | V |
| I_{IH} | digital input current, sample mode | $V_{\text{IH}} = 2.4\text{ V}$ | - | - | 20 | μA |
| V_{IL} | digital input voltage, sample mode (logic 0) | | 0 | - | 0.8 | V |
| I_{IL} | digital input current, hold mode | $V_{\text{IL}} = 0.4\text{ V}$ | -400 | - | - | μA |

Notes

- Over audio band (20 Hz to 20 kHz).
- In sampling mode.
- At maximum input signal.
- Distortion of sampled signal at a sample frequency of 50 kHz.
- The ripple rejection is measured at the output of the hold amplifier; amplitude = 0.5 Vtt. $f = 100\text{ Hz}$ to 10 kHz.

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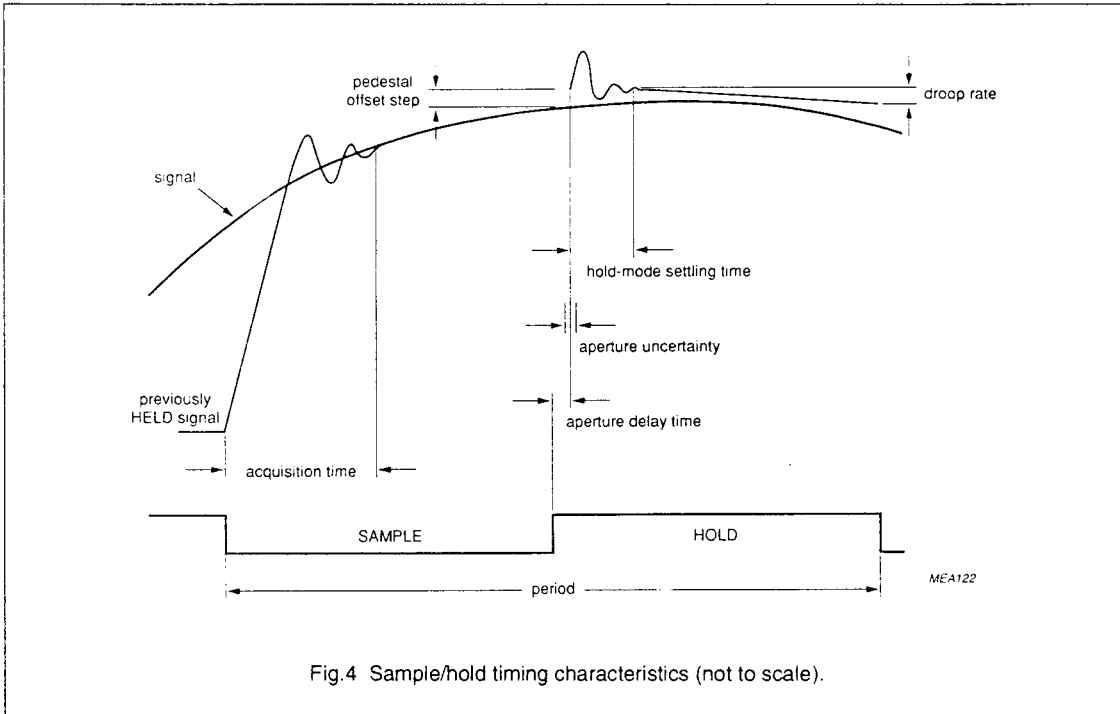


Fig.4 Sample/hold timing characteristics (not to scale).

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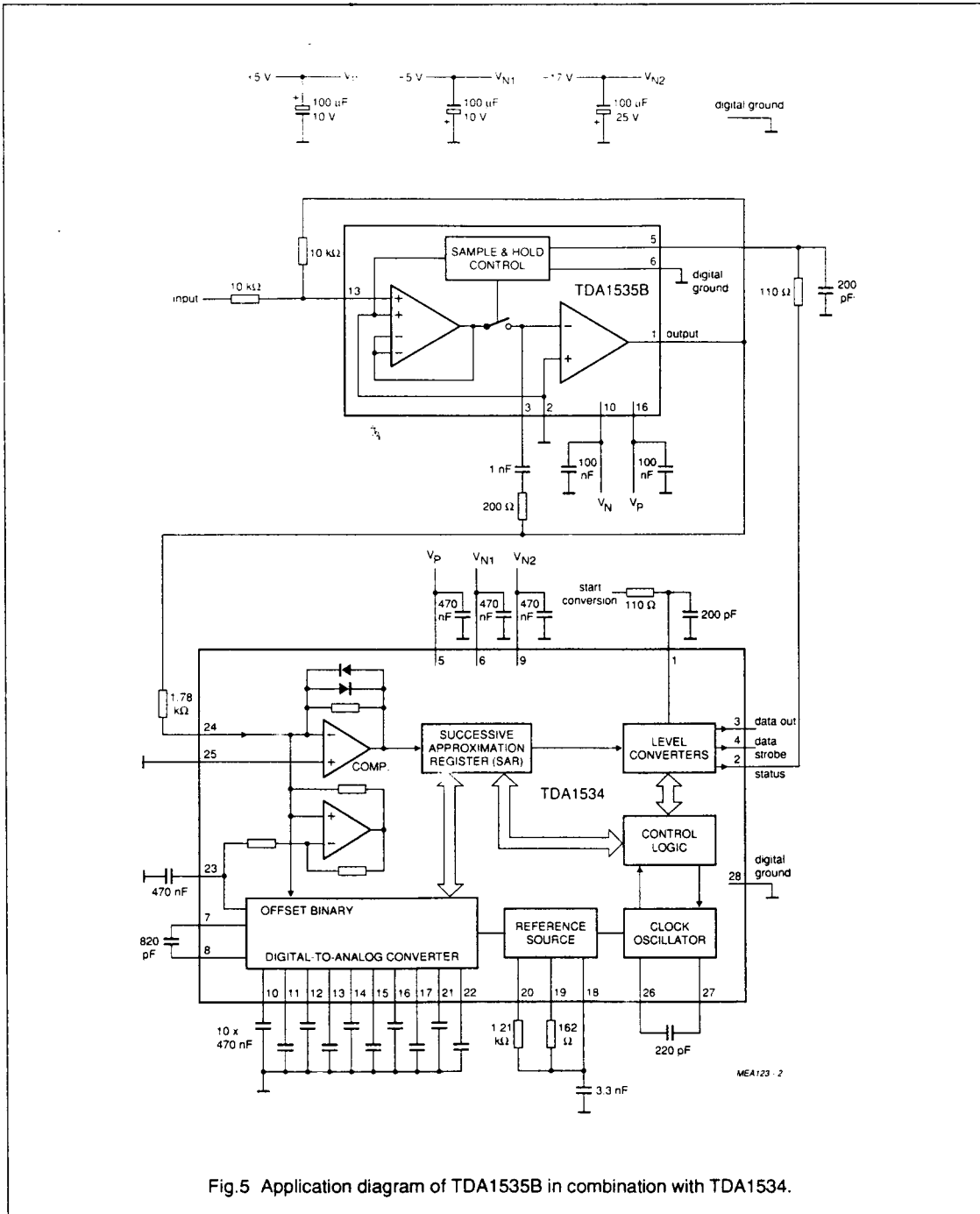


Fig.5 Application diagram of TDA1535B in combination with TDA1534.