



TDA 2054M

LINEAR INTEGRATED CIRCUIT

PREAMPLIFIER WITH ALC FOR C_rO₂ CASSETTE RECORDERS

- EXCELLENT VERSATILITY IN USE (V_S from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- STEREO MATCHING BETTER THAN 3 dB (matched pair)

The TDA 2054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- low noise preamplifier
- automatic level control system (ALC)
- high gain equalization amplifier

It is intended as preamplifier in tape and cassette recorders and players (C_rO₂), dictaphones, compressor and expander in telephonic equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

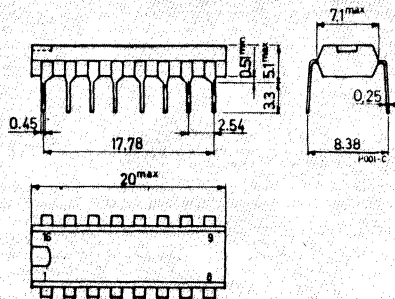
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} = 50^\circ\text{C}$	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

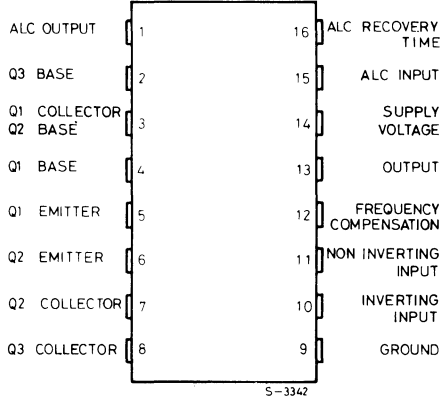
ORDERING NUMBERS: TDA 2054M mono applications
2 TDA 2054M stereo applications

MECHANICAL DATA

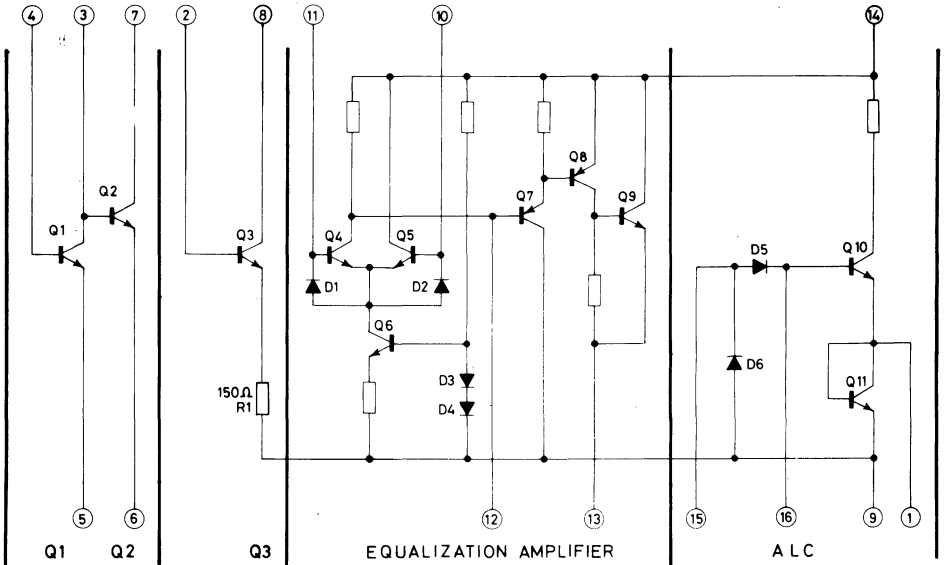
Dimensions in mm



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM

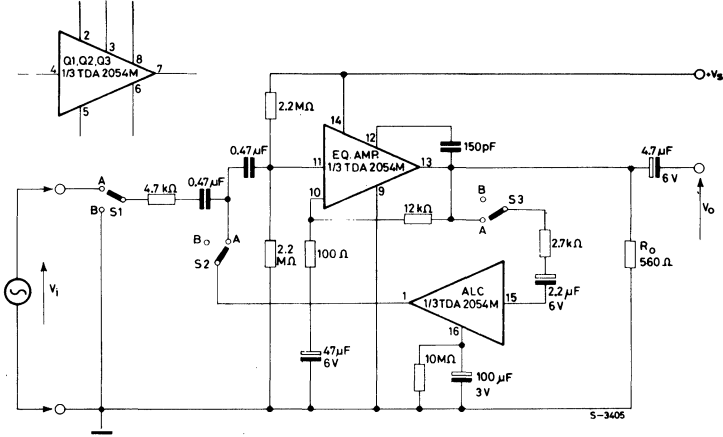


5-3404



TDA2054M

TEST CIRCUIT



THERMAL DATA

R _{th j-amb}	Thermal resistance junction-ambient	max	200	°C/W
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ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	
V _s	Supply voltage	4		20	V	
I _d	Quiescent drain current	V _s = 9V S1 = S2 = S3 = at B	10		mA	
h _{FE}	DC current gain (Q1, Q2, Q3)	I _c = 0.1 mA V _{CE} = 5V	300	500	—	
e _N	Input noise voltage (Q1, Q2, Q3)	I _c = 0.1 mA V _{CE} = 5V f = 1 KHz		2	$\frac{nV}{\sqrt{Hz}}$	
i _N	Input noise current (Q1, Q2, Q3)		0.5		$\frac{pA}{\sqrt{Hz}}$	
NF	Noise figure (Q1, Q2, Q3)	I _c = 0.1 mA V _{CE} = 5V R _g = 4.7 KΩ B (-3 dB) = 20 to 10000 Hz	0.5	4	dB	
G _v	Open loop voltage gain (for equalization amplifier)	V _s = 9V f = 1 KHz	60		dB	
V _o	Output voltage with A.L.C.	V _s = 9V V _i = 100 mV f = 1 KHz S1 = S2 = S3 at A	0.6		V	
e _N	Equivalent input noise voltage (for equalization amplifier pin 11)	V _s = 9V G _v = 40 dB S1 at B B (-3 dB) = 20 to 20000 Hz	1.3		μV	
R ₁	Q3 emitter resistance		105	150	195	Ω

Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (transistors Q1, Q2, Q3)

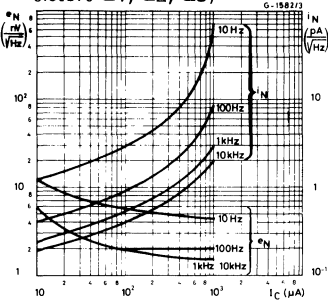


Fig. 2 - Equivalent input noise current vs. frequency (transistors Q1, Q2, Q3)

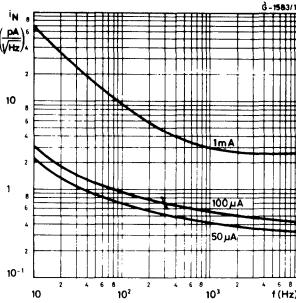


Fig. 3 - Equivalent input noise voltage vs. frequency (transistors Q1, Q2, Q3)

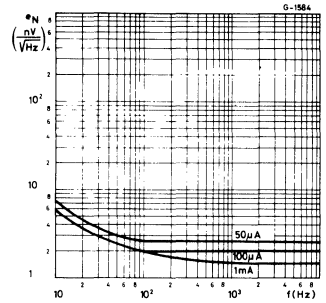


Fig. 4 - Noise figure vs. bias current (transistors Q1, Q2, Q3)

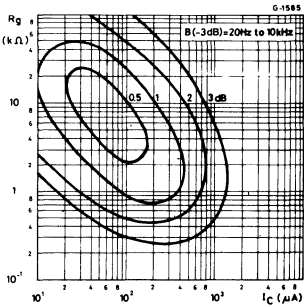


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (transistors Q1, Q2, Q3)

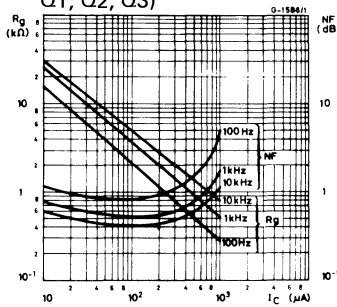


Fig. 6 - Current gain vs. collector current (transistors Q1, Q2, Q3)

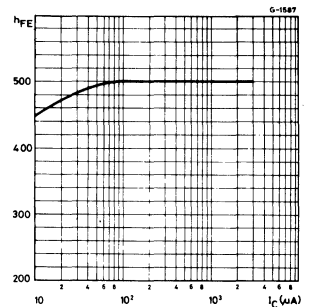


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

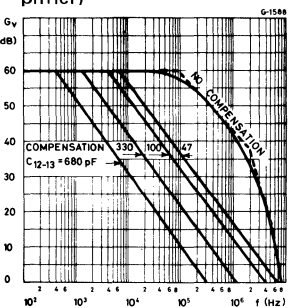


Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)

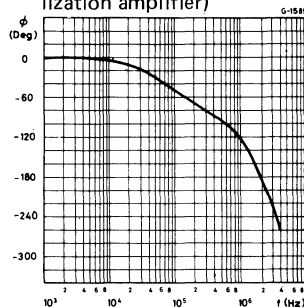
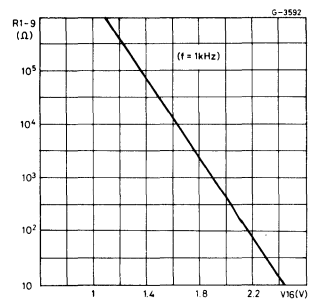


Fig. 9 - Dynamic resistance R1-9 vs. ALC voltage V16





TDA2054M

APPLICATION INFORMATION

Fig. 9 - Application circuit for C_rO₂ cassette player and recorder

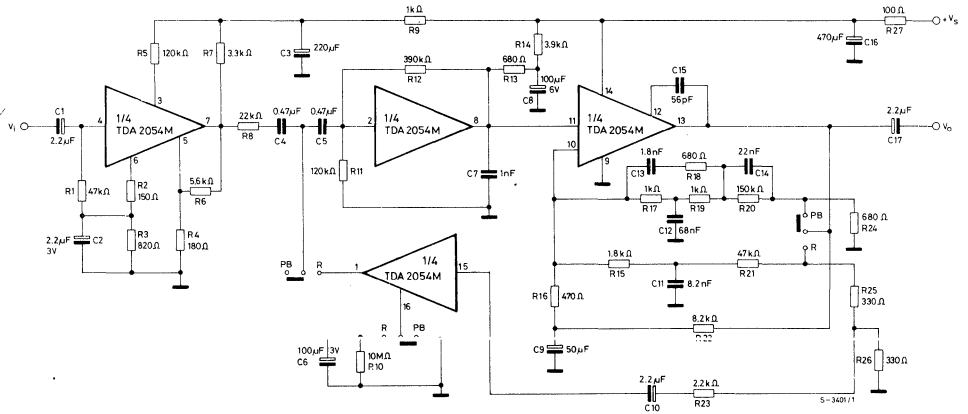
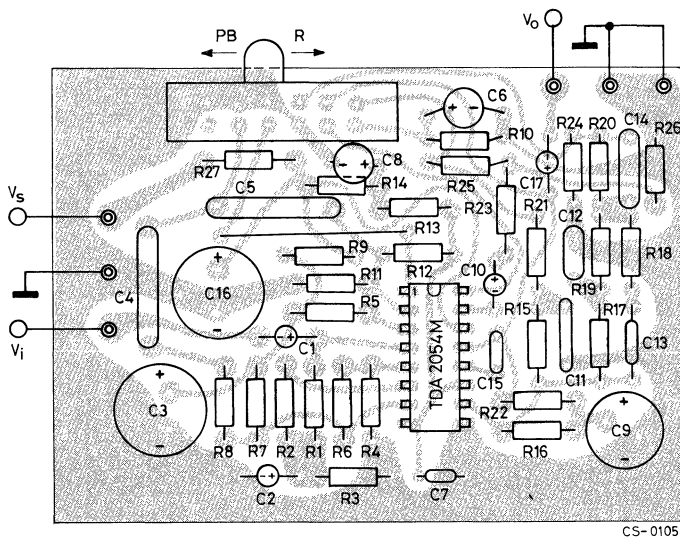


Fig. 10 - P.C. board and component layout for the circuit of Fig. 9 (1:1 scale)



CS-0105

TYPICAL PERFORMANCE OF CIRCUIT IN FIG. 9 ($T_{amb} = 25^{\circ}\text{C}$, $V_s = 9\text{V}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK					
G_v	Voltage gain (open loop)	$f = 20$ to 20000 Hz		134	dB
G_v	Voltage gain (closed loop)	$f = 1$ KHz		60	dB
Z_i	Input impedance	$f = 100$ Hz		10	$\text{K}\Omega$
		$f = 1$ KHz		41	$\text{K}\Omega$
		$f = 10$ KHz		43	$\text{K}\Omega$
Z_o	Output impedance	$f = 1$ KHz		12	Ω
B	Frequency response		see fig. 11		
d	Distortion	$V_o = 1\text{V}$ $f = 1$ KHz		0.2	%
	Output background noise	$Z_g = 300\Omega + 120$ mH (DIN 45405)		1.5	mV
***	Output weighted background noise			1	mV
$\frac{S+N}{N}$	Signal to noise ratio	$V_o = 1.5\text{V}$ $Z_g = 300\Omega + 120$ mH		60	dB
t_{on}^*	Switch-on time	$V_o = 1\text{V}$		500	ms

RECORDING

G_v	Voltage gain (open loop)	$f = 20$ to 20000 Hz		134	dB
G_v	Voltage gain (closed loop)	$f = 1$ KHz		72	dB
B	Frequency response		see fig. 13		
d	Distortion with ALC	$V_o = 1\text{V}$ $f = 10$ KHz		0.5	%
ALC	Automatic level control range (for 3 dB of output voltage variation)	$V_i \leq 40$ mV $f = 10$ KHz		54	dB
V_o	Output voltage before clipping without ALC	$f = 1$ KHz		3	V
V_o	Output voltage with ALC	$V_i = 30$ mV $f = 1$ KHz		1.1	V
t_l^*	Limiting time (see fig. 17)			75	ms
t_{set}^*	Level setting time (see fig. 17)	$\Delta V_i = +40$ dB $f = 1$ KHz		300	ms
t_{rec}^*	Recovery time (see fig. 17)	$\Delta V_i = -40$ dB $f = 1$ KHz		150	sec.
t_{on}^*	Switch-on-time	$V_o = 1\text{V}$		500	ms
$\frac{S+N}{N}^{***}$	Signal to noise ratio with ALC	$V_o = 1\text{V}$ $R_g = 470\Omega$		64	dB

* This value depends on external network.

** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 15 KHz can be avoided - so halving the output noise.

*** Weighted noise measurement (DIN 45405).

Fig. 11 - Frequency response for the circuit in fig. 9 (playback)

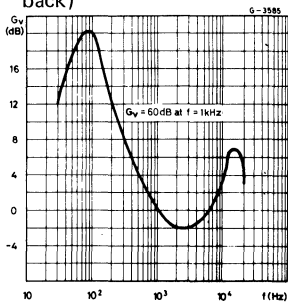


Fig. 12 - Distortion vs. frequency for the circuit in fig. 9 (playback)

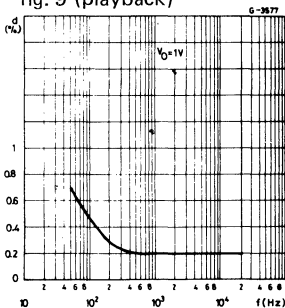


Fig. 13 - Frequency response for the circuit in fig. 9 (recording)

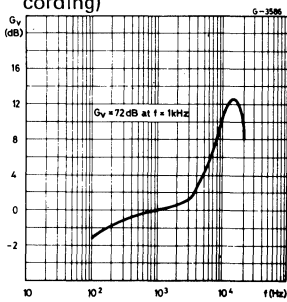


Fig. 14 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

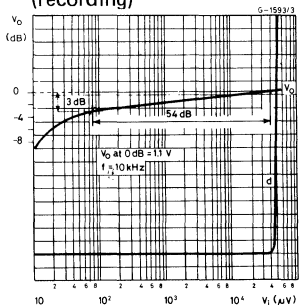


Fig. 15 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

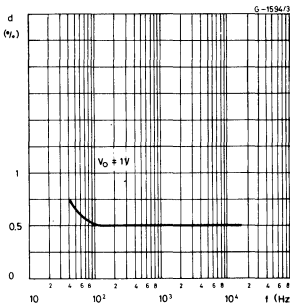


Fig. 16 - Limiting and level setting time vs. input signal variation

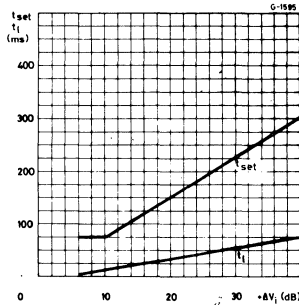


Fig. 17 - Limiting, level setting, recovery time

