Synchroneous Demodulator Combination for PAL Colour TV Sets

TDA 2522

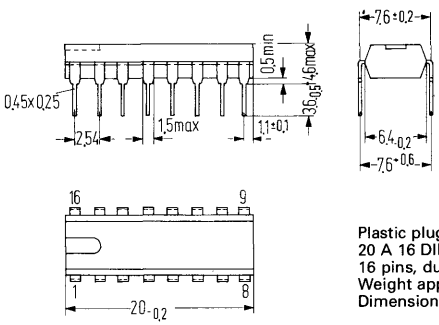
Preliminary data

The monolithic integrated circuit TDA 2522 entains a 8.8-MHz colour subcarrier oscillator with divider stage for the production of both 4.4-MHz reference signals.

- Circuit for the production of the chrominance signal control voltage and a reference voltage
- Circuit for the production of the colour-killer and identification signal
- Colour-killer delay
- Two synchronous demodulators for (B–Y) and (R–Y) signals
- Matrix for (G–Y)-signals
- PAL flipflop and PAL switch
- Blanking in the synchroneous demodulators

Type	Ordering code
TDA 2522	Q67000-A1230

Package outlines



Plastic plug-in package
20 A 16 DIN 41866 (SOT-38)
16 pins, dual-in-line
Weight approx. 1.2 g
Dimensions in mm

Absolute maximum ratings

Supply voltage	$V_{11/4max}$	14	V
Storage temperature	T_s	−20 to +125	°C
Ambient temperature in operation	T_{amb}	−20 to +60	°C
Total power dissipation	P_{tot}	600	mW

Preliminary data

Electrical characteristics ($V_{P(11/4)}$ = 12 V, T_{amb} = 25 °C)

Typical current consumption		$I_{P(11)}$	40	mA
Ratio of demodulated signals at $V_{F(B-Y)} = V_{F(R-Y)}$		$V_{(B-Y)}$	1.78 $V_{(R-Y)}$	
Matrix for (G–Y)-signal		(G–Y)	−0.51 (R–Y) −0.19 (B–Y)	
Input resistance of the chrominance signal inputs		$R_{ch(R-Y)}$	≥ 800	Ω
		$R_{ch(B-Y)}$	≥ 800	Ω
Input capacitance of the chrominance signal inputs		$C_{ch(R-Y)}$	≤ 10	pF
		$C_{ch(B-Y)}$	≤ 10	pF
Output voltages of colour difference signal		$V_{(R-Y)}$	≥ 2.4	V_{pp}
		$V_{(G-Y)}$	≥ 1.35	V_{pp}
		$V_{(B-Y)}$	≥ 3.0	V_{pp}
DC voltage at the colour difference signal outputs		$V_{3/4}$	5.6	V
		$V_{2/4}$	5.6	V
		$V_{1/4}$	5.6	V
Impedance of the colour difference signal outputs		$Z_{(R-Y)}$	250	Ω
		$Z_{(G-Y)}$	250	Ω
		$Z_{(B-Y)}$	250	Ω
H/2 ripple voltage at (R–Y)-output		$V_{H/2}$	≤ 10	mV_{pp}
Input resistance of the 8.8 MHz oscillator		$R_{9/4}$	270	Ω
Output resistance of the 8.8 MHz oscillator		$R_{10/4}$	200	Ω
Total holding range		Δf	± 500	Hz
Key pulses (at pin 15) coming from horizontal combination TDA 2590				
Colour sync. signal keying	ON	$V_{15/4}$	≥ 7.5	V
	OFF	$V_{15/4}$	≤ 6.5	V
Blanking	ON	$V_{15/4}$	≥ 2.0	V
	OFF	$V_{15/4}$	≤ 1.0	V

Preliminary data

Electrical characteristics (contin.)

Voltage at pin 14			
without colour sync signal	$V_{14/4}$	7.0	V
with colour sync signal (peak-to-peak value) of 0.25V at pins 5 and 6	$V_{14/4}$	5.5	V
Reference output voltage	$V_{12/4}$	7.0	V
Chrominance signal control voltage (depending on $V_{14/4}$) at $\pm I_{13} \leqq 200$ µA	$V_{13/4}$	.5 . . . 5.0	V
at $V_{14/4} \leqq 5.5$V	$V_{13/4}$	≤1.0	V
Phase difference between reference signal and colour syncsignal at ±400 Hz frequency deviation	φ	±5°	
Colour killing at	$V_{14/4}$	≧6	V
or at	$V_{16/4}$	12	V
Colour setting at	$V_{14/4}$	≤5.6	V
or at	$V_{16/4}$	0	V
Colour setting delay (by C_Y at pin 16)	t_Y	24	ms/µF

Block diagram with application hint