Preliminary data

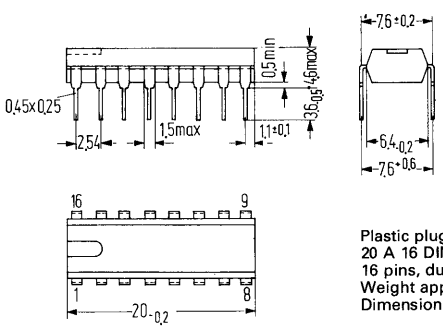
The monolithic integrated circuit TDA 2560 contains

luminance amplifier
with adaptation circuit for Y-delay line
contrast and brightness adjustment
blanking and keying
additional video output with positively directed synchronous level

chrominance amplifier
with controlled chrominance signal amplifier
saturation and contrast adjustment
direct driving of the PAL delay line
common output for chrominance and colour sync signal (without influencing the colour sync signal amplitude by contrast and saturation adjustment)

Type	Ordering code
TDA 2560	Q67000-A1231

Package outlines



Plastic plug-in package
20 A 16 DIN 41866 (SOT-38)
16 pins, dual-in-line
Weight approx. 1.2 g
Dimensions in mm

Absolute maximum ratings

Supply voltage	$V_{8/5\,max}$	14	V
Storage temperature	T_s	−25 to +125	°C
Ambient temperature in operation	T_{amb}	−25 to +65	°C
Total power dissipation	P_{tot}	930	mW

Preliminary data

Electrical characteristics ($V_{P(8/5)}$ = 12 V; T_{amb} = 25 °C) according to application circuit

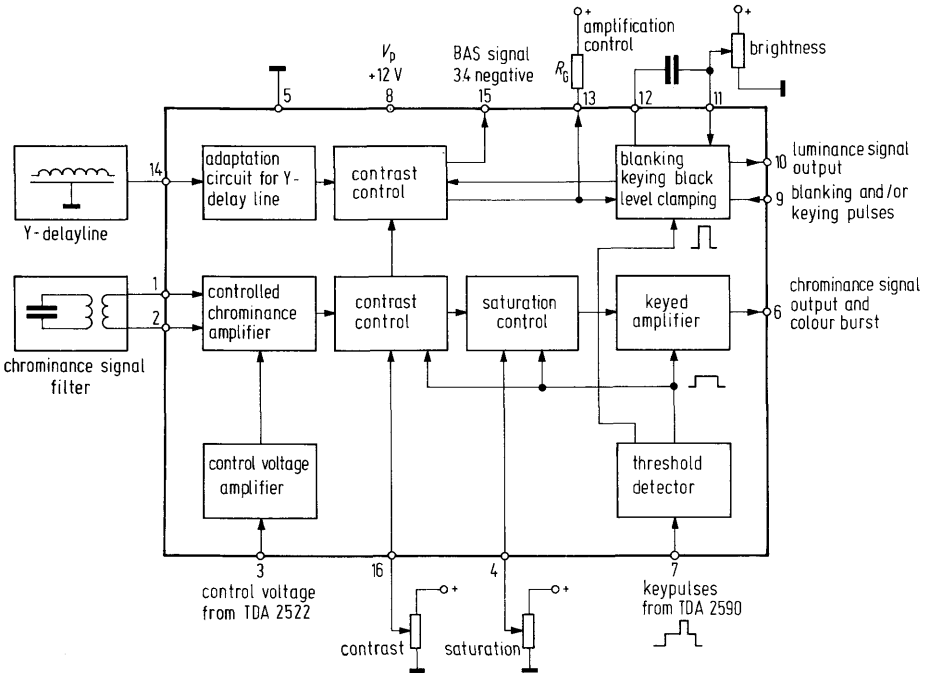
Current consumption	$I_{P(8)}$	46	mA
Luminance amplifier[2])			
Input current	I_{14}	.2	mA_{pp}
Input impedance	$Z_{14/5}$	150	Ω
Contrast adjusting range	E_c	> 20	dB
Brightness adjusting range (black level)	$V_{10/5}$	1 . . 3	V
Brightness adjusting voltage	$V_{11/5}$	1 . . 3	V
Black level shifting by contrast adjustment, picture contents and temperature	ΔV	< ±20	mV
3 dB band width	B	5	MHz
BAS output voltage with positively directed sync level	$V_{15/5}$	3.4	V_{pp}
Black level clamping pulse[3])	$V_{7/5}$	8	V
Blanking pulses[4])			
for 0 V at output (pin 10)	$V_{9/5}$	3	V
for 1.55 V at output (pin 10)	$V_{9/5}$	6	V
Chrominance amplifier			
Input voltage	$V_{2/1}$	4 . . 80	mV_{pp}
Reachable output signal[5])	$V_{6/5}$	2	V_{pp}
Control range of the chrominance signal amplifier		> 30	dB
Starting of the chrominance signal control[6])	$V_{3/5}$	1.1	V
Contrast synchronism (at 10-dB contrast variation)		± 1	dB
Saturation adjustment range[7])	E_s	+6 . . . −50	dB
Colour sync signal gating[3])	$V_{7/5}$	2	V
Signal-noise ratio at nominal input voltage	S/N	> 50	dB
Phase shifting of the colour sync signal to the chrominance signal	φ	< ±5°	

See remarks next page

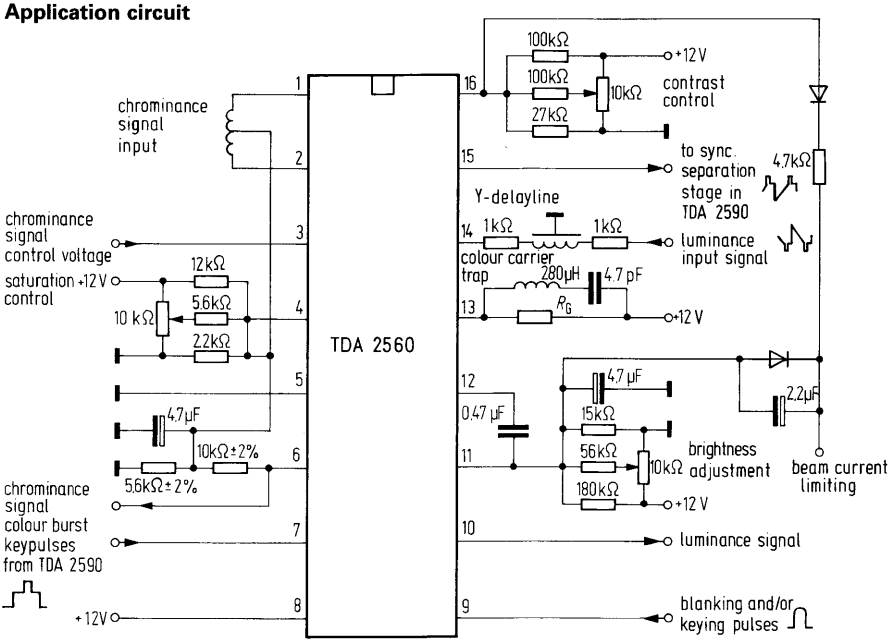
Remarks to the previous page

1) Supply voltage range $V_P = 9 \ldots 14$ V,
admissible hum voltage $V_P = 100\ mV_{pp}$
2) The gain of the luminance amplifier can be influenced by the load resistance R_9 at pin 13. The scattering of the gain is reduced to a minimum, since it depends only from the scattering of the relationship between Y delay line end resistor and the resistor R_9.
3) Key pulses (from TDA 2590) for colour sync signal keying and for black level clamping are sent to pin 7.
The black level clamping becomes effective at +8 V, key pulses must be in that time that clamping only becomes effective at the back slope of the black shoulder.
The colour sync signal gate circuit, which switches the gain of the chrominance signal amplifier during its return to maximum, becomes effective at +2 V.
4) The luminance signal is keyed via pin 9:
when the key pulse reaches +3 V, the luminance signal output (10) is blanked;
at +6 V, a standard level of approx. 1.55 V is keyed which can be used for clamping.
5) Chrominance signal and colour sync signal are both available at pin 6. The colour sync signal is not influenced by contrast and saturation adjustment; it remains stable by means of the control voltage of TDA 2522.
The ratio of the chrominance signal to the colour sync signal is at nominal contrast (3 dB below maximum) and at nominal saturation (6 dB below maximum) the same at the output and at the input.
6) When the voltage becomes more negative, the gain is reduced.
7) Linear range up to −40 dB

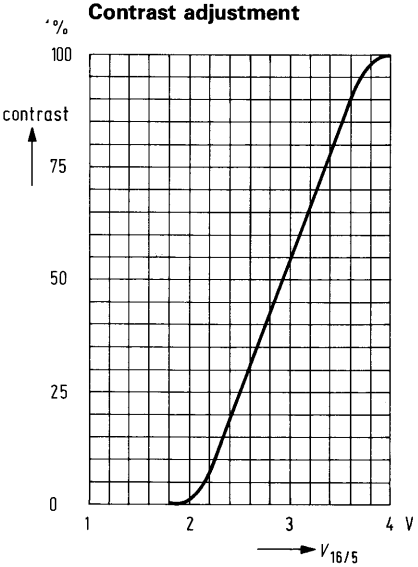
Block diagram



Application circuit



Contrast adjustment



Saturation adjustment