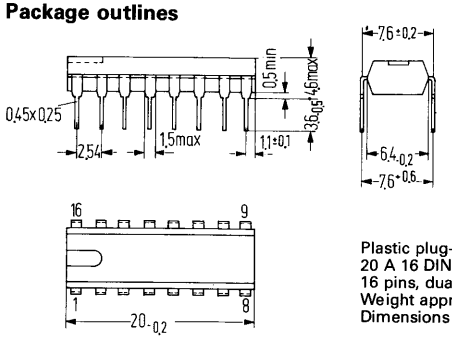
Preliminary data

The monolithic integrated circuit TDA 2590 is adapted to the integrated colour circuits TDA 2522 and TDA 2560

with line oscillator according to the threshold switch principle
phase comparation between sync pulse and oscillator (φ_1)
phase discriminator φ_2 for phase position between line flyback pulse and oscillator
capture range extension by coincidence detector φ_3
time constant and gate switching (VCR operation)
sync pulse separation stage
blanking circuit for interference signal
vertical sync pulse separation stage
production of key pulses for colour sync signal and for line flyback blanking pulses
phase shifter for control pulse
switching of control pulse width and switch-off
output stage with separate supply voltage for direct triggering of thyristor deflection circuits

Type	Ordering code
TDA 2590	Q67000-A1232

Package outlines



Plastic plug-in package
20 A 16 DIN 41866 (SOT-38)
16 pins, dual-in-line
Weight approx. 1.2 g
Dimensions in mm

Absolute maximum ratings

Ambient temperature in operation	T_{amb}	−20 to +60	°C
Storage temperature	T_s	−25 to +125	°C
Voltages	$V_{p(1/16)}$	13.2	V[1])
	$V_{Pr(2/16)}$	18.0	V
	$V_{4/16}$	13.2	V
	$\pm V_{9/16}$	6.0	V
	$\pm V_{10/16}$	6.0	V
	$V_{11/16}$	13.2	V
Currents	I_{2M}	400	mA
	$-I_{3M}$	400	mA
	I_4	1	mA
	$\pm I_6$	10	mA
	$-I_7$	10	mA
	I_{11}	2	mA

[1]) with power supply

Preliminary data

Electrical characteristics ($V_{P(1/16)}$ = 12 V; T_{amb} = 25 °C)

Inputs

Sync pulse separating stage (pin 9)			
Input switching voltage	V_{9s}	.8	V
Input switching current	I_{9s}	5 to 100	μA
Input leakage current (at V_9 = −5 V)	I_{9lk}	≤1	μA
Interference signal blanking circuit (pin 10)			
Input modulation voltage	V_{10mod}	1.0	V
Input switching voltage	V_{10s}	1.4	V
Input modulation current	I_{10mod}	5 to 100	μA
Input switching current	I_{10s}	150	μA
Input leakage current (at V_{10} = −5 V)	I_{10lk}	≤1	μA
Line flyback pulse input (pin 6)			
Input current	I_6	≥10	μA
Input switching voltage	V_{6s}	1.4	V
Input voltage limitation	V_{6l}	−0.7/+1.4	V
Input resistance	R_{i6}	400	Ω
Switching to VCR operation (pin 11)			
Input voltage	V_{11}	0 to 1.5	V
Input current	$-I_{11}$	≥200	μA
or			
Input voltage	V_{11}	9.0 to 13.2	V
Input current	I_{11}	1 to 2	mA
Switching of control pulse widths (pin 4)			
for t = 6 μs input voltage	V_4	9.4 to 13.2	V
input current	I_4	≥200	μA
for t = 14 μs+t_d input voltage	V_4	0 to 4	V
input carrent	$-I_4$	≥200	μA
for t = 0 (V_3 = 0) input voltage[1])	I_4	0	V

[1]) or input 4 open

Preliminary data

Electrical characteristics (contd.)

Outputs

Vertical sync pulses, positive (pin 8)			
Output voltage	V_8	11 (≧10)	V_{pp}
Output resistance	R_{q8}	2	kΩ
Colour sync key pulses, positive (pin 7)			
Output voltage	V_7	11 (≧10)	V_{pp}
Output resistance	R_{q7}	400	kΩ
Line flyback blanking pulses, positive (pin 7)			
Output voltage	V_7	2.5 to 3.5	V_{pp}
Output resistance	R_{q7}	400	Ω
Control pulses, positive (pin 3)			
Output voltage	V_3	10.5	V_{pp}
Output current, average value	$-I_{3AV}$	2.5	mA
Output resistance for front slope	R_{qf3}	2.5	Ω
Output resistance for back slope	R_{pr3}	20	Ω

Oscillator (pins 14 and 15)

lower threshold voltage	V_{14thl}	4.4	V
upper threshold voltage	V_{14thu}	7.6	V
Reverse current	I_{15}	± .47	mA

Phase comparison φ_1 sync pulse/oscillator (pin 13)

Control voltage range	V_{13}	3.8 to 8.2	V
Control current	$\pm I_{13M}$	1.9 to 2.3	mA_{pp}
Output leakage current at $V_{13} = 4 \ldots 8$ V	I_{13q}	≤1	µA
Output resistance, $V_{13} = 4 \ldots 8$ V	R_{q13}	high ohmic	[1]
Output resistance, $V_{13} < 3.8$ V/> 8.2 V	R_{q13}	low ohmic	[2]

Output of the time constant switch (pin 12)

Output voltage	V_{12}	6.0	V
Output current	$\pm I_{12}$	≤1	mA
Output resistance, $V_{11} = 2.5 \ldots 7.0$ V	R_{q12}	100	Ω
Output resistance, $V_{11} \leq 1.5$ V/≧9 V	R_{q12}	30	kΩ

Coincidence detector φ_3 (pin 11)

Output voltage	V_{11}	.5 to 6.0	V
Output current, no coincidence	I_{11M}	.1	mA
Output current, with coincidence	$-I_{11M}$	.5	mA

[1]) Current source output
[2]) Emitter follower

Preliminary data

Electrical characteristics (contd.)

Phase comparison φ_2 line flyback pulse/oscillator (pin 6)			
Control voltage range	V_6	5.4 to 7.6	V
Control current	$\pm I_{5M}$	1	mA_{pp}
Output and/or input resistance			
at $V_6 = 5.4 \ldots 7.6$ V	$R_{q/16}$	high ohmic	[1]
at $V_6 < 5.4$ V/> 7.6 V	$R_{q/16}$	8	kΩ
Input current with blocked phase detector and V_6 = 6.5 V	I_6	≤5	µA
Operating data at $V_{P(1/16)}$ = 12 V and the indicated external circuitry			
Sync pulse separation stage (pin 9)			
Input signal (BAS)	V_9	3 to 4	V_{pp} [2]
Input key current	I_{9k}	≤100	µA
Interference signal blanking circuit (pin 10)			
Input signal (BAS)	U_{10}	3 to 4	V_{pp} [2]
Input key current	I_{10k}	≤100	µA
Admissible superposed interference signal	V_{10}	≤7	V_{pp}
Vertical sync pulse separation			
Delay between front slopes of input signal and output signal	$t_{S\ on}$	12	µs
Delay between back slopes of input signal and output signal	$t_{V\ off}$	≥$t_{V\ on}$	
Output voltage	V_8	11	V_{pp}
Output resistance	R_{q8}	2	kΩ
Oscillator			
Oscillator frequency (unsynchronized) with C_{osc} = 4.7 nF, R_{osc} = 12 kΩ	f_o	15.625	kHz
Scattering of oscillator frequency	Δf_o	≤+5	% [3]
Frequency-adjusting level	$\Delta f_o/\Delta I$	31	Hz/µA
Adjusting range for the indicated external circuitry	Δf_o	±10	%
Dependence of the oscillator frequency from the supply voltage	$\frac{\Delta f_o/f_o}{\Delta V_{cc}/V_{cc}}$	≤±0.05	[2]
Frequency modification with supply voltage lowered to 4 V	Δf_o	≤±10	% [3]
Temperature coefficient of oscillator frequency	TC_f	≤$\pm 10^{-4}$/K	[3]

[1] Current source switching
[2] Admissible range 1 to 7 V
[3] Scattering of external components is not considered.

Preliminary data

Operating data (contd.)

Phase comparison φ_1 sync pulse/oscillator

Control sensitivity	$S\varphi$	2	kHz/µs
Scattering of control sensitivity	$\Delta S\varphi$	± 10	%[1])
Catching and holding range	Δf	± 780	Hz
Scattering of catching and holding range	$\Delta(\Delta f)$	± 10	%[1])

Time constant switch — compare electrical characteristics

Coincidence detector φ_3 — compare electrical characteristics

Phase comparison φ_2 line flyback pulses / oscillator

Admissible delay between front slope and line flyback pulse (t_{fl} = 12 µs)	t_{dmax}	15	µs
Static control error	$\Delta t/\Delta t_d$	≤ .2	%

Total phase position

Phase position between mid sync pulse and mid line flyback pulse	Δt	2.6	µs
Phase position tolerance	$\Delta(\Delta t)$	≤ .7	µs

Total phase position and phase position of front slope of control pulse is set automatically by phase comparison φ_2.

For any additional setting:

Voltage supply	$\Delta V/\Delta t$	.1	V/µs
Current supply	$\Delta I/\Delta t$	30	µA/µs
Scattering of supply current	$\Delta(\Delta I)$	≤ 10	%[1])

Colour sync signal key pulse

Phase position between mid sync pulse at input and back slope of colour sync signal key pulse at V = 7 V	Δt	6.75 (5.8 to 7.7)	µs
Width of colour sync signal key pulse	t	5.0 (4.3 to 5.6)	µs

[1]) Scattering of external components is not considered.

Preliminary data

Operating data (contd.)

Control pulse switch		compare electrical characteristics	
Control pulse output			
Duration of control pulse			
at $V_4 \geqq 9.4$ V	t	6.0 (4.5 to 7.5)	µs
at $V_4 \leqq 4$ V	t	14 µs+t_d	
Control pulse switch off with supply voltage	V_{cc}	$\leqq 4$	V
Key pulse			
Duration of key pulse	t	8	µs
Time between front slope of key pulse and mid of sync pulse	Δt	4 ($\geqq 2.75$)	µs
Time between back slope of key pulse and mid of sync pulse	Δt	4 ($\geqq 2.75$)	µs

Block diagram with application note