

## PAL CHROMINANCE SIGNAL PROCESSOR FOR VIDEO RECORDERS

### GENERAL DESCRIPTION

The TDA3760 is a monolithic integrated circuit for chrominance signal processing in video recorders.

### Features

- Automatic gain controlled pre-amplifier with record/playback selection
- Signal mixer with balancing stage
- Output stage for the 627 kHz chrominance signal, with facility for being disabled by colour killer and record/playback mode switch
- Amplitude detector with automatic gain control for the preamplifier
- 4,43 MHz voltage controlled oscillator (VCO) for recording and playback
- 4,43 MHz fixed oscillator for playback
- Phase detector controlled synchronization of the VCO
- Subcarrier mixer
- H/2 demodulator for the production of PAL identification and colour killing signals
- Flip-flop for PAL identification
- Sandcastle pulse processing
- Colour killing stage with hysteresis
- Internal record/playback selection
- Second phase detector for fast phase correction of sub-carrier

### QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_p = V_{9-15}$	typ.	10 V
Supply current (pin 9)	$I_p = I_9$	typ.	45 mA
<b>Inputs</b>			
Chrominance signal			
4,43 MHz for record (peak-to-peak value)	$V_{2-15(p-p)}$	typ.	200 mV
627 kHz for playback (peak-to-peak value)	$V_{1-15(p-p)}$	typ.	200 mV
<b>Outputs</b>			
Chrominance signal			
4,43 MHz (peak-to-peak value)	$V_{24-15(p-p)}$	typ.	490 mV
627 kHz (peak-to-peak value)	$V_{26-15(p-p)}$	typ.	2 V

### PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

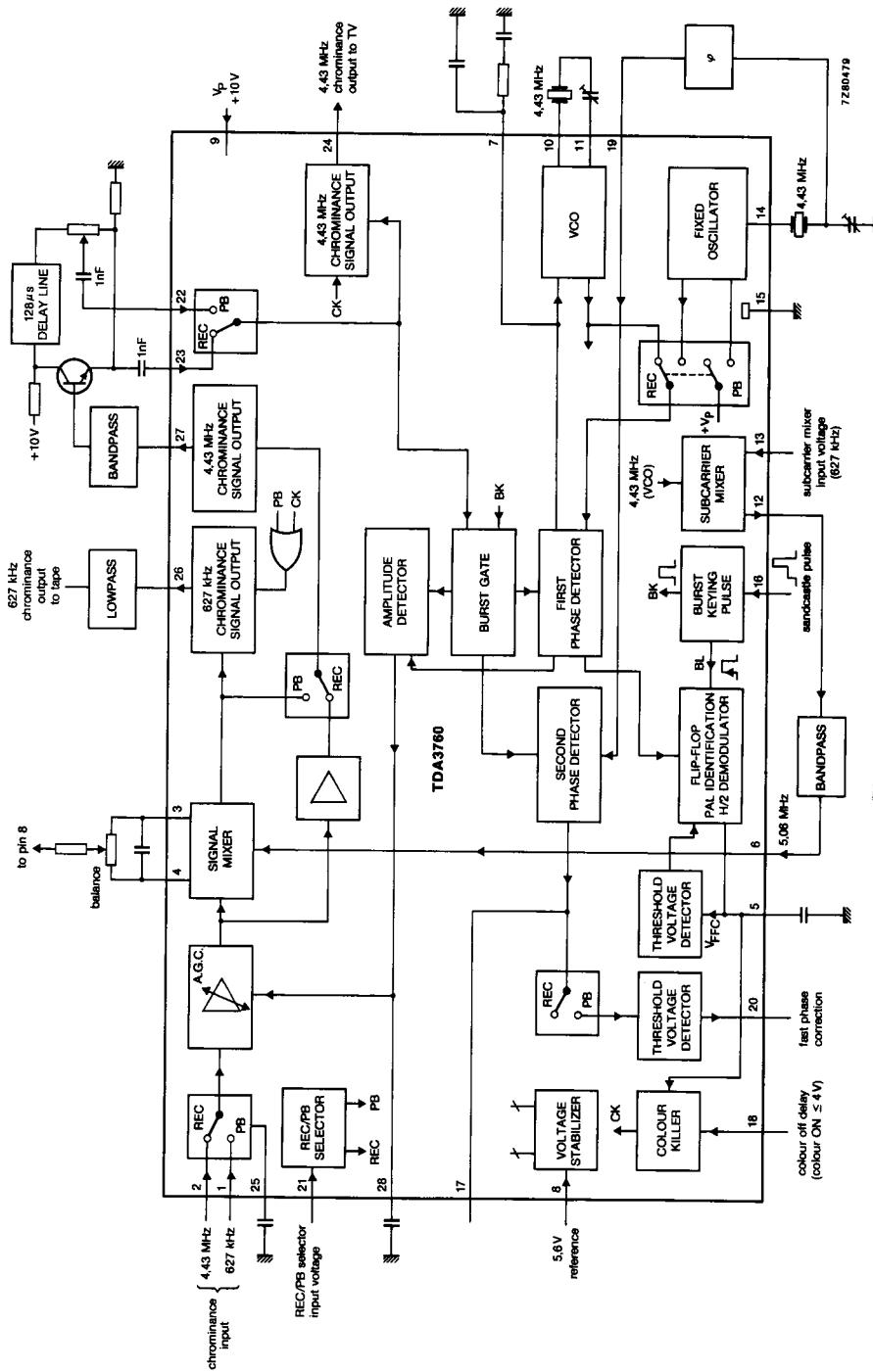


Fig. 1 Block diagram.

**REC** = burst key pulse  
**PB** = blanking pulse  
**CK** = colour killer

**BK** = burst key pulse  
**BL** = blanking pulse  
**FFC** = flip-flop correction  
**FPC** = fast phase correction

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_P = V_{9-15}$	max.	13,2 V
Voltage range at pins 1, 2, 5, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23 to pin 15 (ground)	$V_{n-15}$	0 to $V_P$	V
Voltage ranges			
at pins 3, 4, 28*	$V_{3, 4, 28-15}$	3 to 6	V
at pin 6, 25*	$V_{6, 25-15}$	0 to 5	V
at pin 10*	$V_{10-15}$	1,5 to 4	V
at pin 13*	$V_{13-15}$	0 to 3	V
at pin 14*	$V_{14-15}$	0 to 8	V
Voltages			
at pin 12	$V_{12-15}$	max.	$V_P$ V
at pin 24	$V_{24-15}$	max.	7 V
Currents			
at pins 11, 18	$-I_{11, 18}$	max.	2 mA
at pins 12, 26, 27	$-I_{12, 26, 27}$	max.	5 mA
at pin 24	$-I_{24}$	max.	3 mA
Total power dissipation	$P_{tot}$	max.	1,4 W
Storage temperature range	$T_{stg}$	-25 to +150	°C
Operating ambient temperature range	$T_{amb}$	0 to +70	°C

\* Measured with  $V_{8-15} = 5,6$  V

## CHARACTERISTICS

$V_P = V_{9-15} = 10 \text{ V}$ ;  $V_{8-15} = 5,6 \text{ V}$ ;  $T_{\text{amb}} = 25^\circ\text{C}$ ; burst key duration  $4 \mu\text{s}$ ; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 9)</b>					
Supply voltage	$V_P = V_{9-15}$	9,6	—	13,2	V
Supply current for playback and burst keying at $-I_{12, 18, 24, 26, 27} = 0$	$I_P = I_9$	—	45	—	mA
at $-I_{12, 18, 24, 26, 27} = 0$ ; $V_P = 12 \text{ V}$	$I_P = I_9$	—	46	—	mA
<b>A.G.C. preamplifier (pins 1 and 2)</b>					
Input voltage* ( $f = 4,43 \text{ MHz}$ ) during record (peak-to-peak value)	$V_{2-15(\text{p-p})}$	20	—	400	mV
Input voltage* ( $f = 627 \text{ kHz}$ ) during playback (peak-to-peak value)	$V_{1-15(\text{p-p})}$	30	—	400	mV
Input resistance	$R_{1, 2-15}$	7	—	—	$\text{k}\Omega$
Input capacitance	$C_{1, 2-15}$	—	—	5	pF
<b>627 kHz chrominance signal (pin 26)*</b> (transposed on to 627 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-15(\text{p-p})}$	—	2	—	V
Signal suppression at output for $f = 1,25 \text{ MHz}$	$\alpha_{26}$	—	35	—	dB
for $f = 5,06 \text{ MHz}$ (externally balanced via pins 3 and 4)	$\alpha_{26}$	—	40	—	dB
during colour killing (pin 25)	$\alpha_{26}$	40	—	—	dB
D.C. output voltage	$V_{26-15}$	—	6,7	—	V
<b>4,43 MHz chrominance signal (pin 27)*</b>					
Output voltage during record (peak-to-peak value)	$V_{27-15(\text{p-p})}$	—	1,15	—	V
during playback after signal mixing (peak-to-peak value)	$V_{27-15(\text{p-p})}$	—	—	3,1	V
Signal suppression at output for $f = 5,06 \text{ MHz}$ (externally balanced)	$\alpha_{27}$	—	40	—	dB
for $f = 8,86 \text{ MHz}$	$\alpha_{27}$	—	30	—	dB
for $f = 3,81 \text{ MHz}$	$\alpha_{27}$	—	38	—	dB
for $f = 3,18 \text{ MHz}$	$\alpha_{27}$	—	30	—	dB
D.C. output voltage	$V_{27-15}$	—	7	—	V

\* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	signal	min.	typ.	max.	unit
<b>4,43 MHz chrominance signal amplifier*</b>					
Burst input signal					
at pin 22 (peak-to-peak value)	V <sub>22-15(p-p)</sub>	—	225	—	mV
at pin 23 (peak-to-peak value)	V <sub>23-15(p-p)</sub>	—	225	—	mV
Input resistance					
at pin 22	R <sub>22-15</sub>	6	—	—	kΩ
at pin 23	R <sub>23-15</sub>	6	—	—	kΩ
Output voltage of the chrominance signal					
at pin 24 (peak-to-peak value)	V <sub>24-15(p-p)</sub>	—	490	—	mV
Signal suppression at output (pin 24) during colour killing	α <sub>24</sub>	35	—	—	dB
D.C. output voltage					
during colour-on	V <sub>24-15</sub>	—	2,4	—	V
during colour-off (killed)	V <sub>24-15</sub>	—	0,7	—	V
<b>Subcarrier mixer</b>					
627 kHz input voltage; sine-wave (peak-to-peak value)	V <sub>13-15(p-p)</sub>	220	—	—	mV
Input resistance	R <sub>13-15</sub>	1	—	—	kΩ
D.C. output voltage	V <sub>12-15</sub>	—	7,9	—	V
5,06 MHz output voltage selective** (peak-to-peak value)	V <sub>12-15(p-p)</sub>	—	800	—	mV
Signal suppression at output** for f = 4,43 MHz	α <sub>12</sub>	20	—	—	dB
for f = 5,68 MHz	α <sub>12</sub>	30	—	—	dB
<b>Subcarrier input</b>					
5,06 MHz input voltage (peak-to-peak value)	V <sub>6-15(p-p)</sub>	250	—	—	mV
Input resistance	R <sub>6-15</sub>	1,9	—	—	kΩ
Input capacitance	C <sub>6-15</sub>	—	—	5	pF

\* Chrominance signal values hold for a 75% saturated colour bar signal.

\*\* Measured with a 0,32 V (peak-to-peak), 627 kHz input signal on pin 13 ( $-I_{12} = 1 \text{ mA}$ ).

## CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>4,43 MHz voltage controlled oscillator (VCO)</b>					
Input resistance	R <sub>10-15</sub>	—	430	—	Ω
Input capacitance	C <sub>10-15</sub>	—	—	10	pF
Output resistance	R <sub>11-15</sub>	—	—	200	Ω
PLL-controlled oscillator catching range	Δf	± 500	—	—	Hz
Phase difference between oscillator and burst signal for ± 400 Hz deviation of crystal frequency	ψ	± 7	—	—	deg
<b>4,43 MHz fixed oscillator</b>					
Oscillator temperature coefficient*	TC	—	—	-3	Hz/K
<b>Record/playback selector (pin 21)</b>					
Input voltage for record**	V <sub>21-15</sub>	—	—	4	V
Input current with V <sub>21-15</sub> = 4 V	I <sub>21</sub>	—	—	130	μA
Input voltage for playback	V <sub>21-15</sub>	8	—	—	V
Input current with V <sub>21-15</sub> = 8 V	I <sub>21</sub>	—	—	430	μA
Input resistance	R <sub>21-15</sub>	7	—	—	kΩ
<b>Colour (on/off) killer delay</b>					
Delay for chrominance signal OFF at ΔV = 1 V; C = 1 μF; PNP emitter follower with internal current of 0,1 mA	t <sub>d</sub>	—	10	—	ms
Input voltage (pin 18) for forced colour ON					
for forced colour OFF	V <sub>18-15</sub>	—	—	4	V
	V <sub>18-15</sub>	5,5	—	9	V
<b>Voltage stabilizer (pin 8)</b>					
Range of external reference voltage	V <sub>8-15</sub>	5,3	—	5,8	V
Input current	—I <sub>8</sub>	—	—	120	μA

\* Not considering the effects of external components.

\*\* Pin open: record.

parameter	symbol	min.	typ.	max.	unit
<b>Sandcastle pulse input (pin 16)</b>					
Input voltage for burst keying	V <sub>16-15</sub>	7,1	—	—	V
Input current	I <sub>16</sub>	—	—	5	μA
Delay time of BK	t <sub>d</sub>	—	0,55	—	μs
Input voltage for triggering of flip-flop	V <sub>16-15</sub>	2	—	—	V
<b>Fast phase correction</b>					
Input voltage* (peak-to-peak value)	V <sub>19-15(p-p)</sub>	200	—	400	mV
Input resistance	R <sub>19-15</sub>	3,3	—	—	kΩ
Output voltage <i>without correction</i> below phase differences of ± 50° at I <sub>20</sub> < ± 20 μA and V <sub>17-15</sub> < 6,5 V	V <sub>20-15</sub>	—	—	5,2	V
<i>with correction</i> above phase differences of ± 65° at I <sub>20</sub> < ± 20 μA and V <sub>17-15</sub> > 7,1 V	V <sub>20-15</sub>	9	—	—	V
Output resistance	R <sub>20-15</sub>	—	35	—	kΩ

\* Phase difference between output pin 14 and input pin 19 should be φ = 90°.

## APPLICATION INFORMATION

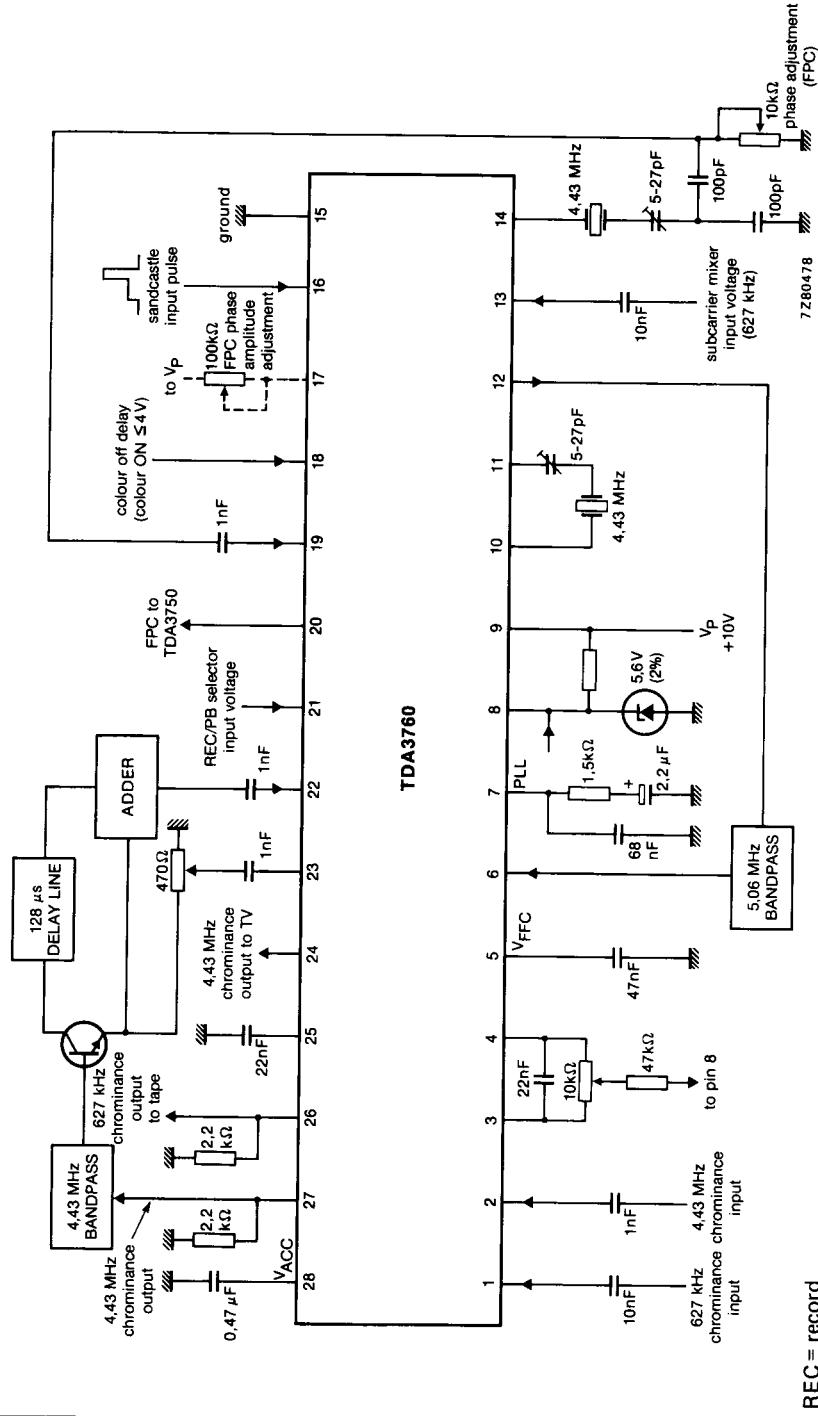


Fig. 2 Application diagram.