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VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		V_{13-16}	4.5	5.0	5.5	V
pin 1		V_{1-16}	11.0	11.25	11.5	V
Supply current	V_{13-16} = 5 V	I_{13}	–	14	–	mA
Operating current	V_{1-16} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

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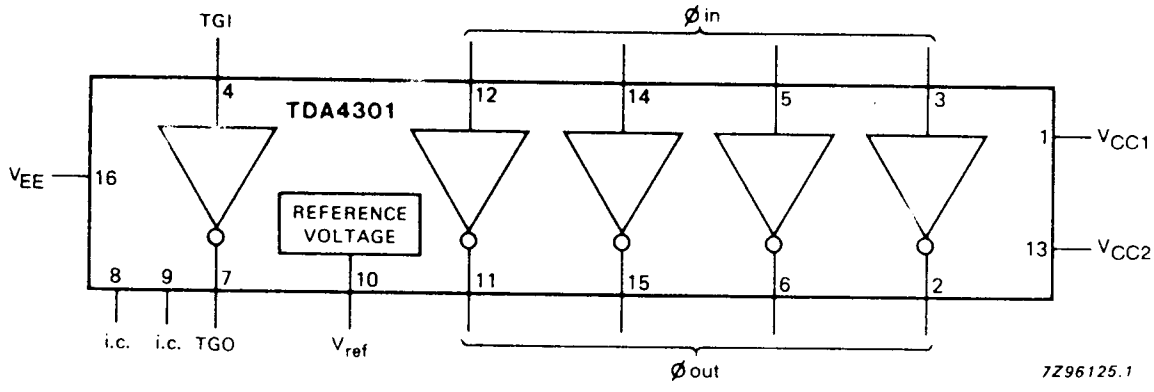

Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

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AC CHARACTERISTICS

$V_{CC1} = V_{1-16} = 11.25$ V; $V_{CC2} = V_{13-16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_{\phi TH}$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

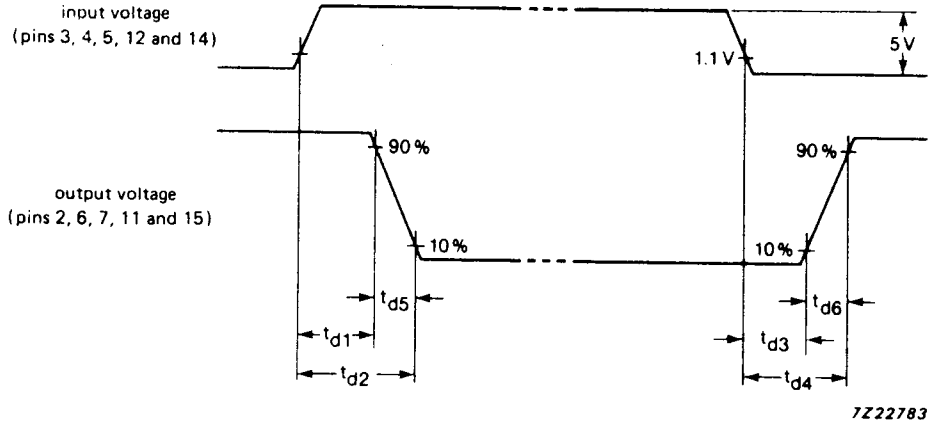

Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

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APPLICATION INFORMATION

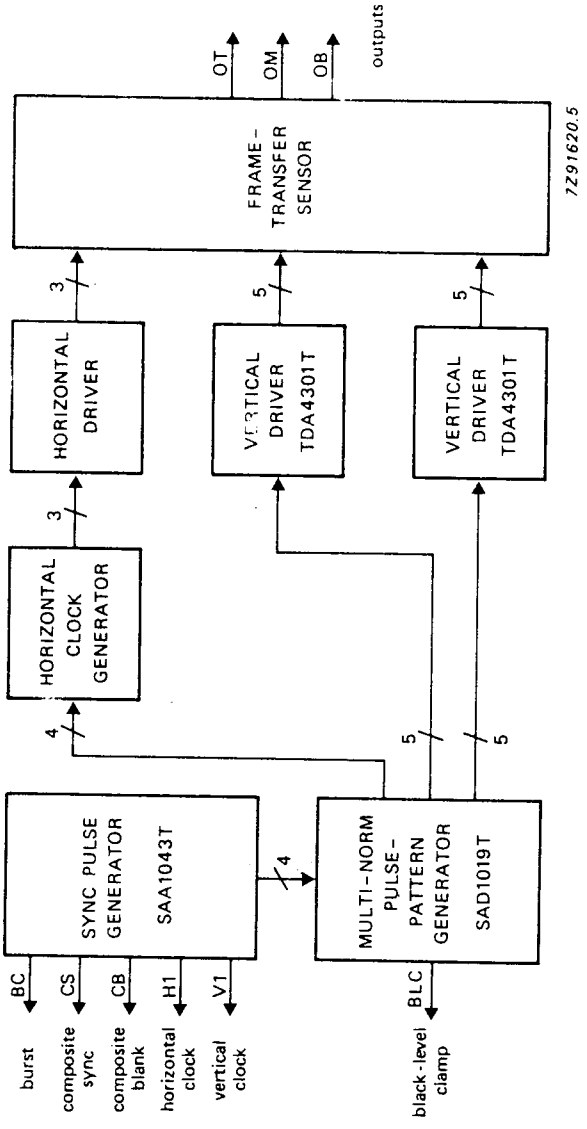

Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

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