TDA4431
TDA4433

TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

The TDA4431 and the TDA4433 are monolithic integrated circuits in a 14 lead dual-in-line plastic package. They integrate the following functions:

– TV signal identificator – Sync. separator – Threshold detector – Digital Interface – Voltage regulator

They are intended for use in Electronic Program Memory tuning systems, the TDA4431 in conjunction with M193B1, while the TDA4433 with M293B1. The circuits features are:

– Identification of true TV stations only.
– Low impedance output of the identification signal.
– Digital control signal for automatic search and AFC operation.
– Thermal compensation of the voltage regulator.

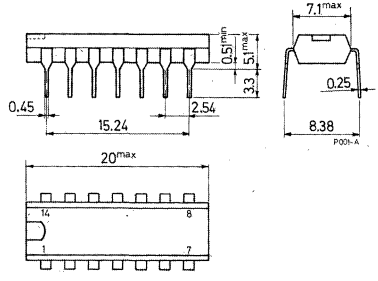
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 1)	16	V
V_3	Voltage at pin 3	16	V
V_{13}	Voltage at pin 13	-5 to +6	V
I_2	Pin 2 current (TDA4431)	± 1	mA
I_6 ; I_2	Pin 6 and pin 2 current (TDA4433)	1	mA
I_{10}	Pin 10 current	2	mA
I_{11}	Pin 11 current	2	mA
I_{12}	Pin 12 current	± 2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBERS: TDA 4431
TDA 4433

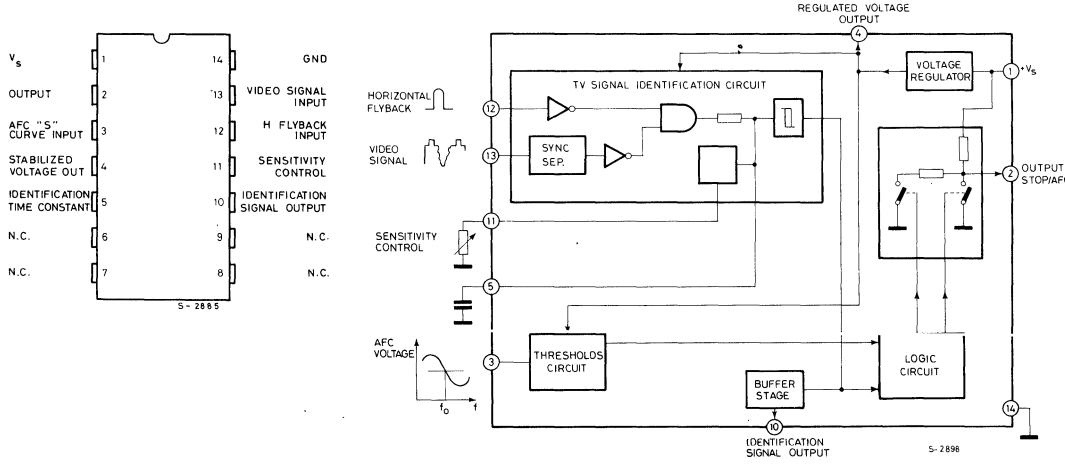
MECHANICAL DATA

Dimensions in mm



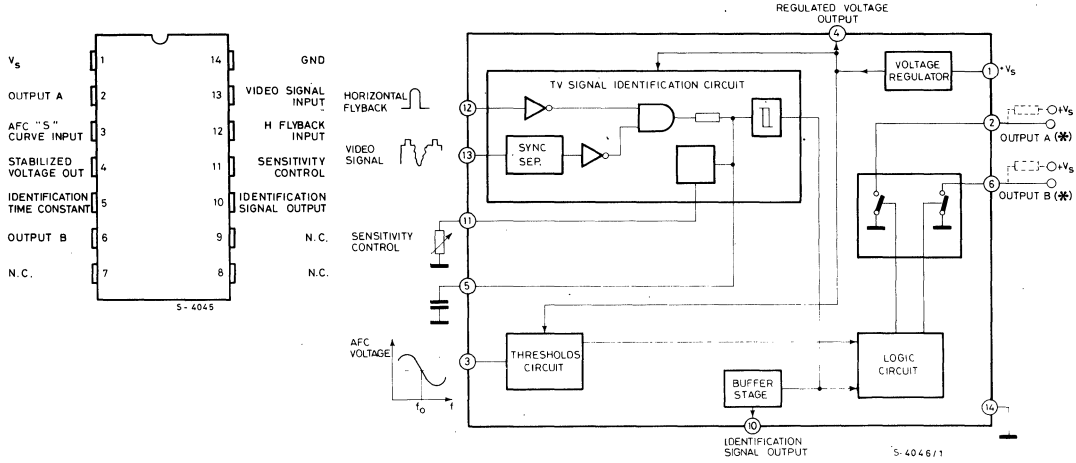
CONNECTION AND BLOCK DIAGRAM (TDA4431)

(Top view)



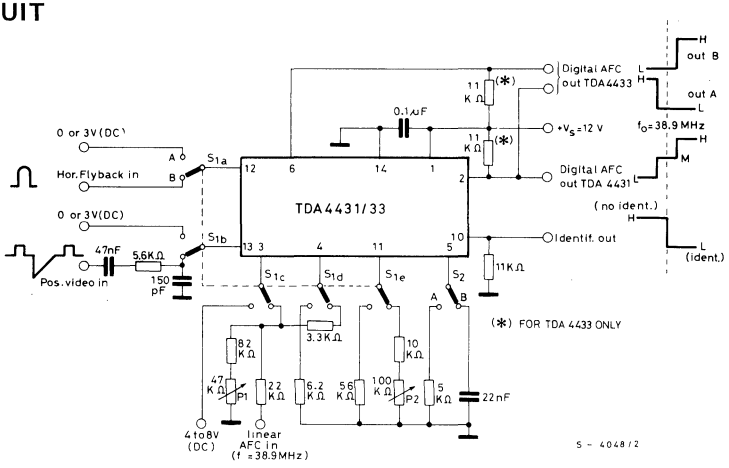
CONNECTION AND BLOCK DIAGRAM (TDA4433)

(Top view)



* Open collector outputs

TEST CIRCUIT



S_1 A : Static tests
B : Functional tests

S_2 A : DC or pulses width
B : Functional tests

P_1 Digital AFC perfect tuning
P_2 Sensitivity control

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit; V_s = 12V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range (pin 1)		10.8		14.5	V
I_s	Supply current (pin 1)	V_s = 14.5V			30	mA
V_2	Output voltage: low	$f_{tuning} < f_o$			0.8	V
	medium	$f_{tuning} = f_o$ V_s = 10.8 to 14.5	5.5		8.5	V
	high (TDA4431)	$f_{tuning} > f_o$	V_s-0.5			V
V_2	Output voltage	$f_{tuning} < f_o$ I_2 = 1mA	V_s-0.5			V
		$f_{tuning} = f_o$			0.8	V
	(TDA4433)	$f_{tuning} > f_o$			0.8	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter			Test conditions	Min.	Typ.	Max.	Unit
V_6	Output voltage		$f_{tuning} < f_o$ $I_6 = 1mA$			0.8	V
			$f_{tuning} = f_o$ $I_6 = 1mA$			0.8	V
	(TDA4433)		$f_{tuning} > f_o$	V_s-0.5			V
I_2	Output current (TDA4431)					± 25	μA
V_3	Input voltage range			4		8	V
V_{3U}	Upper threshold voltage (see fig. 2)			V_4-25	V_4	V_4+25	mV
V_{3L}	Lower threshold voltage (see fig. 2)			V_4-425	V_4-400	V_4-375	mV
R_3	Input resistance		$V_3 = V_4$	1.4			MΩ
V_4	Regulated voltage		$I_4 = 1mA$		6.6		V
I_4	Output current					1	mA
R_4	Output differential resistance				60		Ω
$\frac{\Delta V_4}{\Delta T_s}$	Regulated voltage thermal drift					± 2	mV/°C
V_{10}	Identification output voltage	no identification	$I_{10} = 1mA$	V_s-1.3			V
		identification				20	mV
R_{10}	Output resistance				100		Ω
V_{12}	Switch off threshold voltage					1	V
I_{12}	Input flyback current			0.5		1.5	mA
R_{12}	Input resistance		$V_{12} = 3V$		10		KΩ
t_{fly}	Flyback pulse duration			10		17	μsec.
t	Time delay between leading edges of flyback pulse and sync. pulse			0		3.5	μ sec.
V_{13}	Video input signal (peak to peak)			2.5		4.5	V
V_{13}	Sync. pulse amplitude (above black level)			0.52			V
R_{13}	Input resistance					1.5	KΩ

Fig. 1 - Medium output voltage Vs. Supply voltage.

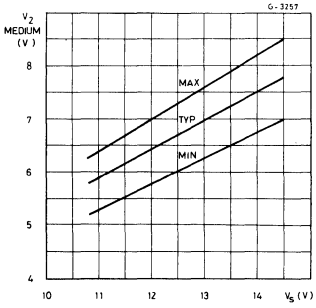
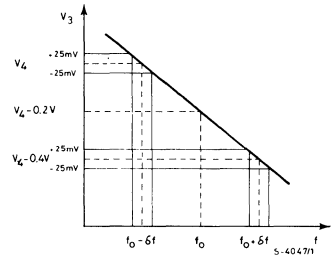


Fig. 2 - Digital AFC threshold voltage vs. frequency.



Input Voltage (V_3)	TDA4431	TDA4433	
	Output voltage (V_2)	Output voltage (V_2)	Output voltage (V_6)
$V_3 > V_4$	Low level	High level	Low level
V_4-0.4V $< V_3 < V_4$	Medium level	Low level	Low level
$V_3 < V_4$-0.4V	High level	Low level	High level

APPLICATION INFORMATION (refer to the block diagram)

TV signal identification circuit:

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.
The signal identification is carried out by charging the capacitor connected to pin 5; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.
When the identification has been made, a signal (level L) is available at pin 10.

Threshold circuit:

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.
With a correct TV signal, the output levels corresponding to the 3 ranges are:

	TDA4431 (V_2)	TDA4433	
		(V_2)	(V_6)
$f_o - \delta f$	L	H	L
f_o	M	L	L
$f_o + \delta f$	H	L	H

L = Low level
M = Medium level
H = High level

Note that the output levels are different for the two devices.

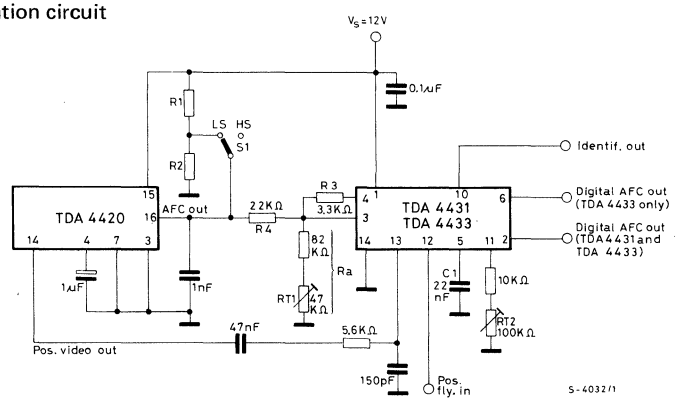
The TDA4431 provides three output levels: low (L), medium (M) and high (H). The output at pin 2 remains at medium level if no video signal is applied at the input or if a video signal is applied but is not identified as a true TV signal.

The TDA 4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

Voltage Regulator

The circuit can deliver 1mA and it can be used as D/A converter reference to supply fine tuning voltage.

Fig. 3 - Application circuit



The passive components should be chosen as follows:

R_1 and R_2 : these define the AFC response slope. For $R_1 = R_2 = 5.1K\Omega$, the typical slope is 750/11 KHz/V (with AFC output unloaded).

S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

R_3 and R_4 : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12V$, the relation is:

$$\delta f = 0.036\,(2\Delta f)\,\frac{R_3 + R_4}{R_3}$$

R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

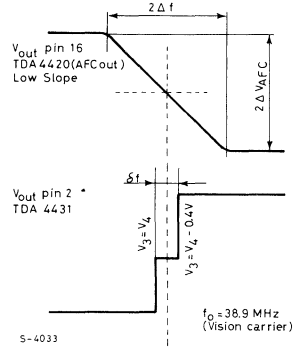
$$R_a = 33\,R_3$$

with $R_3 = 3.3K\Omega$, R_a can be a fixed resistor of $110K\Omega$.

R_{T2} : by means of this trimmer it is possible to choose the better sensitivity. It is possible to put a fixed resistor at pin 11 in the range of 68 KΩ to 100 KΩ.

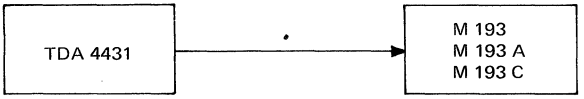
To make a better sensitivity adjustment of trimmer R_{T2}, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Fig. 4 – Linear and digital AFC

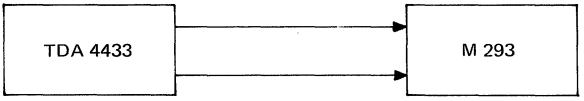


EPM SYSTEM CONFIGURATIONS

1) For 16 channels



2) For 32 channels



3) With microprocessor