RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA5709 is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA5708), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- A.G.C. circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- TTL compatible digital input/output
- Digitalized tracking error signal
- Possibility for car application

QUICK REFERENCE DATA

Supply voltage range	$V_{DD}-V_{BB}$		8 to 13	V
Quiescent supply current	I_Q	typ.	6	mA
Operating ambient temperature range	T_{amb}		−30 to +85	°C

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

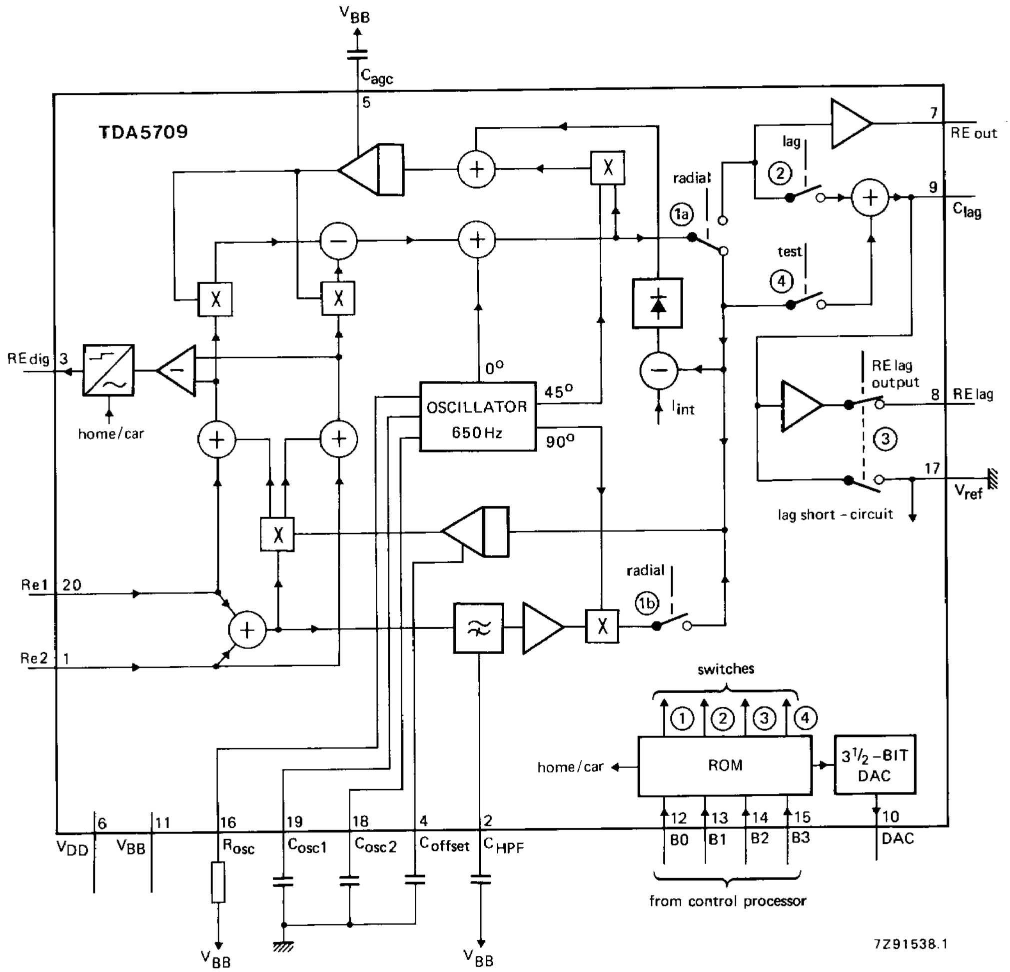

Fig. 1 Block diagram.

DEVELOPMENT DATA

PIN DESCRIPTION

Pin No.	Symbol	Description
1	Re2	Input for amplified currents from photo diodes D1 and D2
2	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
3	REdig	Digital output of sign (Re2 – Re1)
4	C_{offset}	Offset control input for radial offset
5	C_{agc}	Gain control input for radial error signal
6	V_{DD}	Positive supply voltage
7	REout	Current output of amplified (Re2 – Re1) input currents
8	RElag	Voltage output of integrated (Re2 – Re1) input currents
9	C_{lag}	Integrator capacitor for (Re1 – Re2) input currents
10	DAC	Current output for track jumping (3½ bits)
11	V_{BB}	Negative supply connection (also substrate connection)
12	B0	Input control bits for off-, catch-, play-status and DAC output current
13	B1	
14	B2	
15	B3	
16	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
17	V_{ref}	Intermediate supply voltage
18	C_{osc2}	Frequency setting capacitors for oscillator
19	C_{osc1}	
20	Re1	Input for amplified currents from photo-diodes D3 and D4

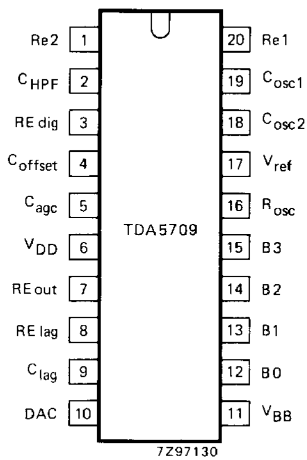

Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range ($V_{DD} - V_{BB}$) pin 6 – pin 11	$V_{DD}-V_{BB}$	–0,3 to	+13	V
Total power dissipation	P_{tot}	see Fig. 3		
Storage temperature range	T_{stg}	–55 to	+150	°C
Operating ambient temperature range	T_{amb}	–30 to	+85	°C
Operating junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	72	K/W

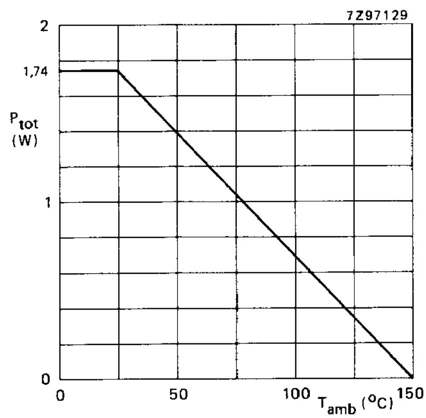

Fig. 3 Power derating curve.

CHARACTERISTICS

V_{DD} = + 5 V; V_{BB} = –5 V; T_{amb} = 25 °C; V_{ref} = 0 V; R_{osc} = 24 kΩ; all voltages with respect to V_{ref}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage					
pin 6 – pin 11 (V_{DD} – V_{BB})		8	–	13	V
pin 17 – pin 11 (V_{ref} – V_{BB})		4,5	5,0	5,5	V
Quiescent supply current	I_Q	–	6	–	mA
REdig output (pin 3)					
Output voltage level					
HIGH (note 1; C)	V_{REdig}	V_{ref} + 2,4	–	–	V
LOW (note 1; A)	V_{REdig}	V_{ref} –0,3	–	V_{ref} + 0,4	V
LOW (note 1; B)	V_{REdig}	V_{BB}	–	V_{BB} + 0,4	V
Output current					
sink current (note 1; A or B)	I_{REdig}	400	–	–	μA
source current (note 1; C)	I_{REdig}	–	–150	–50	μA
Digital inputs (pins 12 to 15)					
B0, B1, B2 and B3					
Input voltage HIGH (note 2)	V_B	V_{ref} + 2	–	V_{DD}	V
Input voltage LOW (note 2)	V_B	V_{BB} + 2	–	V_{ref} + 0,8	V
Input voltage HIGH (note 3)	V_B	V_{BB} + 2	–	V_{DD}	V
Input voltage LOW (note 3)	V_B	V_{BB} –0,3	–	V_{BB} + 0,8	V
Input current					
at V_B = HIGH	I_B	–	0	–	μA
at V_B = LOW	I_B	–	–	–10	μA
DAC output (pin 10)					
Output voltage range					
at I_{DAC} = + 150 μA (sink current)	V_{DAC}	V_{BB} + 1,5	–	V_{DD}	V
at I_{DAC} = – 150 μA (source current)	V_{DAC}	V_{BB}	–	V_{DD} –1	V
Output impedance					
at I_{DAC} = 200 μA	$\|Z_{DAC}\|$	–	50	–	MΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAC output (continued)					
Ratio of output current pin 10 to pin 16 (see Table 1)	I_{10}/I_{16}	3,6	4	4,4	
		−4,6	−4	−3,4	
		0,9	1	1,1	
		−1,2	−1	−0,8	
		0,68	0,75	0,82	
		−0,86	−0,75	−0,64	
		0,45	0,5	0,55	
		−0,58	−0,5	−0,42	
		0,23	0,25	0,27	
		−0,29	−0,25	−0,2	
Analogue input (pin 16)					
Input voltage level	V_{Rosc}	–	V_{BB} + 1,2	–	V
Input current level	I_{Rosc}	–	−50	–	μA
Radial error inputs					
(Re1 pin 20, Re2 pin 1)					
Input voltage level at I_{Re1}, I_{Re2} = −105 μA	V_{Re1}, V_{Re2}	–	V_{BB} + 1,4	–	V
Input current	I_{Re1}, I_{Re2}	–	105	–	μA
Input impedance	$\|Z_{Re1}\|$, $\|Z_{Re2}\|$	–	1	–	kΩ
Gain control input (pin 5)					
Input voltage for minimum radial gain	V_{Cagc}	–	V_{BB} + 3,5	–	V
maximum radial gain	V_{Cagc}	–	V_{BB} + 5,5	–	V
Input impedance	$\|Z_{Cagc}\|$	–	20	–	MΩ
Offset control (pin 4)					
Output current at I_{Re1} = I_{Re2} = −105 μA; V_{Cosc1} = V_{Cosc2} = V_{ref}	$-I_{Coffset}$	–	0,25	–	μA
Input voltage for maximum amplification Re1	$V_{Coffset}$	–	V_{ref} −1	–	V
minimum amplification Re2	$V_{Coffset}$	–	V_{ref} −1	–	V
minimum amplification Re1	$V_{Coffset}$	–	V_{ref} + 1	–	V
maximum amplification Re2	$V_{Coffset}$	–	V_{ref} + 1	–	V
Input impedance	$\|Z_{Coffset}\|$	–	30	–	MΩ

parameter	symbol	min.	typ.	max.	unit
High-pass filter (pin 2)					
Voltage level at $I_{Re1} = I_{Re2} = 0$	V_{HPF}	–	$V_{BB} + 2,8$	–	V
Impedance	$\|Z_{HPF}\|$	–	5	–	kΩ
Oscillator					
(C_{oscl} pin 19, C_{osc2} pin 18)					
Linear input voltage range V_{Coscl}, V_{Cosc2}	V_{Cosc}	$V_{ref} - 2$	–	$V_{ref} + 2$	V
RElag voltage output (pin 8)					
Output voltage range					
at $I_{RElag} = +200\ \mu A$ (sink current)	V_{RElag}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{RElag} = -200\ \mu A$ (source current)	V_{RElag}	V_{BB}	–	$V_{DD} - 1$	V
Maximum source current output	I_{RElag}	–	–2,5	–	mA
Maximum sink current output	I_{RElag}	–	4	–	mA
Output impedance ($f < 10$ kHz)					
with RElag switched on	$\|Z_{RElag}\|$	–	–	50	Ω
with RElag switched off	$\|Z_{RElag}\|$	1	–	–	MΩ
REout push-pull current output (pin 7)					
Output voltage range					
at $I_{REout} = +40\ \mu A$ (sink current)	V_{REout}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{REout} = -40\ \mu A$ (source current)	V_{REout}	V_{BB}	–	$V_{DD} - 1$	V
Output impedance	$\|Z_{REout}\|$	–	2	–	MΩ
C_{lag} push-pull current output/voltage input (pin 9)					
Output voltage range					
at $I_{Clag} = +4\ \mu A$ (sink current)	V_{Clag}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{Clag} = -4\ \mu A$ (source current)	V_{Clag}	V_{BB}	–	$V_{DD} - 1,5$	V
Output impedance	$\|Z_{Clag}\|$	–	15	–	MΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TRANSFER SPECIFICATIONS					
Oscillator (pins 19, 18)					
(V_{osc1}, V_{osc2}: −2 V to + 2 V)					
Transconductance factor					
$\frac{I_{Cosc2}}{V_{Cosc1}} \cdot R_{osc}$		–	0,48	–	
$\frac{I_{Cosc1}}{V_{Cosc2}} \cdot R_{osc}$		–	−0,48	–	
Amplitude stabilization					
$I_{osc1} = f(V_{osc1})$ at $V_{Cosc2} = 0$					
$V_{osc1} = 0$ V (note 4)	I_{osc1}	–	0,1	–	μA
$V_{osc1} = +0,87$ V (note 4)	I_{osc1}	–	$M_2 + 1,4$	–	μA
$V_{osc1} = -0,87$ V (note 4)	I_{osc1}	–	$M_2 - 1,4$	–	μA
$V_{osc1} = +1,2$ V (note 4)	I_{osc1}	–	M_2	–	μA
$V_{osc1} = -1,2$ V (note 4)	I_{osc1}	–	M_2	–	μA
$V_{osc1} = +1,8$ V (note 4)	I_{osc1}	–	$M_2 - 3,5$	–	μA
$V_{osc1} = -1,8$ V (note 4)	I_{osc1}	–	$M_2 + 3,5$	–	μA
Amplitude stabilization					
$I_{osc2} = f(V_{osc2})$ at $V_{Cosc1} = 0$					
$V_{osc2} = 0$ V (note 5)	I_{osc2}	–	0,1	–	μA
$V_{osc2} = +0,87$ V (note 5)	I_{osc2}	–	$M_3 + 1,4$	–	μA
$V_{osc2} = -0,87$ V (note 5)	I_{osc2}	–	$M_3 - 1,4$	–	μA
$V_{osc2} = +1,2$ V (note 5)	I_{osc2}	–	M_3	–	μA
$V_{osc2} = -1,2$ V (note 5)	I_{osc2}	–	M_3	–	μA
$V_{osc2} = +1,8$ V (note 5)	I_{osc2}	–	$M_3 - 3,5$	–	μA
$V_{osc2} = -1,8$ V (note 5)	I_{osc2}	–	$M_3 + 3,5$	–	μA
Transconductance factor					
$\frac{I_{Clag}}{V_{osc1}} \cdot R_{osc}$ with test on; radial off; $I_{Re1} = I_{Re2} = 0$		–	−0,08	–	

parameter	symbol	min.	typ.	max.	unit
Transconductance factor					
$\frac{I_{Clag}}{V_{osc1}} \cdot R_{osc}$					
with lag on; radial on; $I_{Re1} = I_{Re2} = 0$		–	–0,08	–	
Transconductance factor					
$\frac{I_{REout}}{V_{osc2}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$		–	0	–	
$\frac{I_{REout}}{V_{osc1}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$		–	0,8	–	
Transconductance factor					
$\frac{I_{Coffset}}{V_{Cosc2}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0,48	–	
at $I_{HPF} = 0\ \mu A$		–	0	–	
at $I_{HPF} = -30\ \mu A$		–	–0,48	–	
with radial off; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0	–	
Transconductance factor					
$\frac{I_{Coffset}}{V_{Cosc1}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0	–	
with radial off; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0,08	–	
Transconductance factor					
$\frac{I_{agc}}{V_{Cosc1}} \cdot R_{osc}$					
with radial on; $V_{agc} = 0,5$ V; $V_{Coffset} = V_{Cosc2} = 0$ V					
at $I_{Re1} = -150\ \mu A$; $I_{Re2} = 0$		–	–0,48	–	
at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	note 6	–	
at $I_{Re1} = 0$; $I_{Re2} = -150\ \mu A$		–	+ 0,48	–	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transconductance factor					
$\frac{I_{agc}}{V_{Cosc2}} \cdot R_{osc}$					
with radial on; $V_{agc} = 0,5$ V; $V_{offset} = V_{Cosc1} = 0$ V					
at $I_{Re1} = -150\ \mu A$; $I_{Re2} = 0$		–	–0,48	–	
at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	0	–	
at $I_{Re1} = 0$; $I_{Re2} = -150\ \mu A$		–	+0,48	–	
Transfer $C_{lag} \rightarrow$ RElag					
$\frac{V_{RElag}}{V_{Clag}}$; at frequencies < 10 kHz					
with lag short-circuit off; RElag output on		–	1	–	
Slew rate					
RElag amplifier with lag short-circuit off; RElag output on	SR	–	0,4	–	V/μs
Switch lag short-circuit					
Impedance $\frac{\Delta V_{Clag}}{\Delta I_{Clag}}$					
with lag short-circuit on; $\lvert I_{Clag}\rvert < 10\ \mu A$	$\lvert Z_{lag\ sc}\rvert$	–	–	1	kΩ
Offset $\lvert V_{Clag} - V_{ref}\rvert$					
with lag short-circuit on; $I_{Clag} = 0\ \mu A$	$\lvert V_{RElag}\rvert$	–	–	10	mV
Transfer resistance (Re1, Re2 to C_{HPF})					
$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1} + I_{Re2})}$		–	2,5	–	kΩ
Gain (Re1, Re2 to REout)					
$\frac{\Delta I_{REout}}{\Delta(I_{Re1} - I_{Re2})}$					
with lag short-circuit on; radial on; $V_{Coffset} = V_{osc1} = V_{osc2} = 0$ V; $V_{agc} = 0,5$ V		–	5	–	times

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Offset current RE					
Offset current with lag short-circuit on; radial on; $V_{Coffset} = V_{osc1} = V_{osc2} = 0$ V; $V_{agc} = 0,5$ V at $I_{Re1} = I_{Re2} = 100\ \mu A$	I_{RE}	–	0	–	μA
Gain (Re1, Re2 to C_{agc})					
$\frac{\Delta I_{Cagc}}{\Delta(I_{Re1} - I_{Re2})}$ at $I_{Re1} = -104\ \mu A$ with lag short-circuit on; radial on; $V_{Coffset}$ = (see note 7); $V_{agc} = 0,5$ V; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 1,2$ V; $\Delta(I_{Re1} - I_{Re2}) = 8\ \mu A$		–	0,8	–	times
$\frac{\Delta I_{Cagc}}{\Delta(I_{Re1} - I_{Re2})}$ at $I_{Re2} = -104\ \mu A$ with lag short-circuit on; radial on; $V_{Coffset}$ = (note 7); $V_{agc} = 0,5$ V; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 1,2$ V; $\Delta(I_{Re2} - I_{Re1}) = 8\ \mu A$		–	–0,8	–	times
Offset current I_{Cagc}					
Offset current with lag short-circuit on; radial on; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 0$ V; $V_{agc} = 0,5$ V at $I_{Re1} = I_{Re2} = -100\ \mu A$	I_{Cagc}	–	0	–	μA
Transconductance factor					
$\frac{\Delta I_{RE} \cdot V_{RANGE}}{I_{tot} \cdot V_{Coffset}}$ with $V_{Cosc1} = V_{Cosc2} = 0$ V; radial on; $V_{agc} = -3$ V; $V_{RANGE} = 1$ V (internal); $I_{tot} = I_{Re1} + I_{Re2}$ at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	2,5	–	
$\frac{\Delta I_{RE} \cdot V_{RANGE}}{I_{tot} \cdot V_{Coffset}}$ with $V_{Cosc1} = V_{Cosc2} = 0$ V; radial on; $V_{agc} = V_{BB}$; $V_{RANGE} = 1$ V (internal); $I_{tot} = I_{Re1} + I_{Re2}$ at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	0	–	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain control current I_{agc}					
I_{agc} with $V_{Cosc1} = V_{Cosc2} = 0$ V; $V_{agc} = 0{,}5$ V; radial off; $V_{Coffset} = 0$ V					
at $I_{REtot} = 200$ μA; $I_{Re1} - I_{Re2} = 35$ μA	I_{agc}	–	0	–	μA
at $I_{REtot} = 200$ μA; $I_{Re1} - I_{Re2} = 65$ μA	I_{agc}	–	50	–	μA

Notes to the characteristics

1. REdig output conditions:
   A: $I_{Re1} > I_{Re2} + 5$ μA; $V_{Coffset} = V_{ref}$; B0 and B1 and B2 and B3 $> V_{BB} + 2{,}0$ V.
   B: $I_{Re1} > I_{Re2} + 5$ μA; $V_{Coffset} = V_{ref}$; B0 or B1 or B2 or B3 $< V_{BB} + 0{,}8$ V.
   C: $I_{Re2} > I_{Re1} + 5$ μA; $V_{Coffset} = V_{ref}$; don't cares for B0, B1, B2 and B3.
2. In the 'home' application all logical inputs B0, B1, B2 and B3 must be $> V_{BB} + 2$ V.

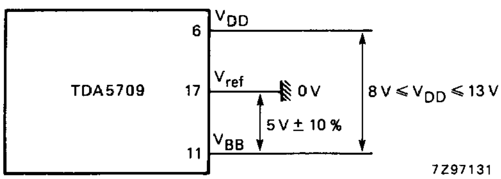

Fig. 4 TDA5709 'home' application.

3. In the 'car' application one or more of the logical inputs B0, B1, B2, B3 must be $< V_{BB} + 0{,}8$ V.

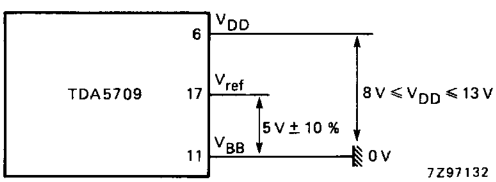

Fig. 5 TDA5709 'car' application.

4. M_2 is the measured value of I_{osc1} at $V_{osc1} = 0$ V.
5. M_3 is the measured value of I_{osc2} at $V_{osc2} = 0$ V.
6. Parabolic curve.
7. $V_{Coffset}$ must be adjusted so that $I_{Clag} = 4$ μA.

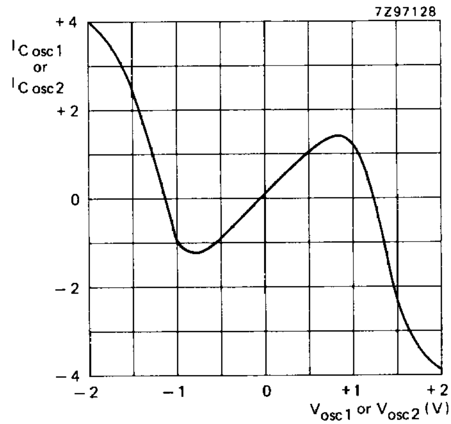

Fig. 6 Amplitude stabilization (typical curve).

Table 1 Truth table for DAC output current

type names	DAC output (μA)*	logical inputs				internal switches				
		B0	B1	B2	B3	lag	lag s/c	rad	test	output RElag
OFF	0	0	0	0	0	off	on	off	off	off
CATCH	0	0	0	0	1	off	on	on	off	off
PUSH	−200	0	0	1	0	off	on	off	off	off
(kick)	−200	0	0	1	1	off	off	off	off	on
PULL	50	0	1	0	0	off	on	off	off	off
PULL	37,5	0	1	0	1	off	on	off	off	off
PULL	25	0	1	1	0	off	on	off	off	off
PULL	12,5	0	1	1	1	off	on	off	off	off
PUSH	−50	1	0	0	0	off	on	off	off	off
PUSH	−37,5	1	0	0	1	off	on	off	off	off
PUSH	−25	1	0	1	0	off	on	off	off	off
PUSH	−12,5	1	0	1	1	off	on	off	off	off
PULL	200	1	1	0	0	off	on	off	off	off
(kick)	200	1	1	0	1	off	off	off	off	on
play	0	1	1	1	0	on	off	on	off	on
test**	0	1	1	1	1	off	off	off	on	on

Where:
0 = input voltage LOW; 1 = input voltage HIGH.
* With R_{OSC} = 24 kΩ.
** Non-proper operating of output REdig if the logical zero is close to V_{BB}.