DATA SHEET

TDA6508; TDA6508A; TDA6509; TDA6509A

3-band mixer/oscillator and PLL for terrestrial tuners

Product specification
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3-band mixer/oscillator and PLL for terrestrial tuners

TDA6508; TDA6508A; TDA6509; TDA6509A

CONTENTS

3-band mixer/oscillator and PLL for terrestrial tuners

TDA6508; TDA6508A; TDA6509; TDA6509A

1 FEATURES

- Single-chip 5 V mixer / oscillator and synthesizer for TV, VCR tuners, DVD-R and PC TV.
- I²C bus protocol compatible with 3.3 V and 5 V microcontrollers
  - Address with 4 data bytes transmission (I²C-bus 'write' mode)
  - Address with 1 status byte (I²C-bus 'read' mode)
  - 4 independent I²C-bus addresses.
- 5 Positive-channel Metal Oxide Semiconductor (PMOS) output ports
  - 3 buffers for band selection (20 mA)
  - 2 buffers for general purpose, e.g. FM sound trap (5 mA).
- 33 V tuning voltage output
- In-lock flag
- 5-step analog-to-digital converter (3 bits in I²C-bus mode)
- 15-bit programmable divider
- Programmable reference divider ratio (64, 80 or 128)
- Programmable charge-pump current (20 or 100 μA)
- Balanced mixer with a common emitter input for LOW band (single input)
- Balanced mixer with a common emitter input for MID band (balanced input)
- Balanced mixer with a common base input for HIGH band (balanced input)
- 2-pin asymmetrical oscillator for LOW band
- 2-pin symmetrical oscillator for MID band
- 2-pin symmetrical oscillator for HIGH band
- External 4-pin IF filter between mixer output (medium impedance) and IF amplifier input (high impedance)
- Weak signal booster (I²C controlled switchable gain amplifier)
- Low power
- Low radiation
- Small size
- TDA6508; TDA6509: symmetrical IF amplifier output to drive a SAW filter (1.25 kΩ)
- TDA6508A; TDA6509A: single-ended IF amplifier to drive low ohmic load (75 Ω).

2 APPLICATIONS

- 3-band tuner for terrestrial TV, DVD-R, VCR and PC TV.

3 GENERAL DESCRIPTION

This device is a programmable 3-band mixer oscillator and synthesizer intended for LOW, MID and HIGH band TV and VCR tuners. It has three double balanced mixers and three oscillators for the LOW, MID and HIGH band respectively, a PLL synthesizer, and an IF amplifier. There are four package variants: TDA6508, TDA6509, TDA6508A and TDA6509A. Versions TDA6508; TDA6509 have a symmetrical IF amplifier; versions TDA6508A; TDA6509A have an asymmetrical IF amplifier, (see Fig.1).

The common output of all three mixers can be connected, via two output pins, to an external IF filter to enable shunted IF bandpass and/or serial filtering for improved signal handling. Two input pins are available for connecting the output of the external filter to the input of the IF amplifier. The mixer output has an impedance of 300 Ω. The IF amplifier input has an impedance of 2.5 kΩ (5 pF).

The overall gain of the tuner can be increased at low signal amplitude conditions to improve TV reception by activating a weak signal booster via the I²C-bus.

There are five open-drain PMOS output ports; each port has a different drive capability. I²C-bus bit P0 enables port P0 (20 mA drain current) and the LOW band mixer oscillator. Bit P1 enables port P1 (20 mA drain current) and the MID band mixer oscillator. When ports P0 and P1 are both disabled, the HIGH band mixer oscillator is enabled. Bit P2 enables port P2 (20 mA drain current). Bit P3 enables port P3 (5 mA drain current) for general use, and bit P4 enables port P4 (5 mA drain current) for general use, and is also combined with the ADC input. When the ports are used, the sum of the drain currents must be limited to 30 mA.

The PLL synthesizer comprises a 15-bit programmable divider, a crystal oscillator, programmable reference divider, phase comparator (phase/frequency detector) combined with a charge-pump which drives an internal tuning amplifier and an output at pin CP. The CP signal current can be integrated by connecting an external RC

loop filter between pin CP and pin VTUNE as shown in Fig.27. The tuning amplifier can supply up to 33 V (max.) at pin VT for controlling any of the internal oscillators via external tank circuits. The phase comparator can operate at 62.5, 50 or 31.25 kHz with a 4 MHz crystal, depending on the reference divider ratio of either 64, 80 or 128; see Table 4. An externally sourced signal having a frequency between 3.58 MHz and 4.43 MHz can be used as a reference frequency for the internal crystal oscillator at any of the reference divider ratios.

In test mode, port P3 will output either half the crystal reference frequency ($\frac{1}{2}f_{ref}$) or half the reference divider frequency ($\frac{1}{2}f_{div}$); see Table 5.

The device can be controlled according to the I^2C-bus format; see Table 1. The in-lock flag bit FL is set to logic 1 when the PLL is locked. This flag is read from the status byte on pin SDA during a READ operation; see Table 6 and Table 7.

Automatic frequency control is provided using an internal Analog-to-Digital Converter controlled by the voltage on pin ADC. The ADC code is read during a READ operation; see Table 8.

The device requires to be addressed by five sequential serial bytes (including the address byte) via the I^2C-bus to set the crystal oscillator frequency, program the five ports and to set the charge-pump current; see Table 1. The address byte can have one of four possible device addresses which are selected by applying a specific voltage to pin AS; see Table 3.

4 QUICK REFERENCE DATA

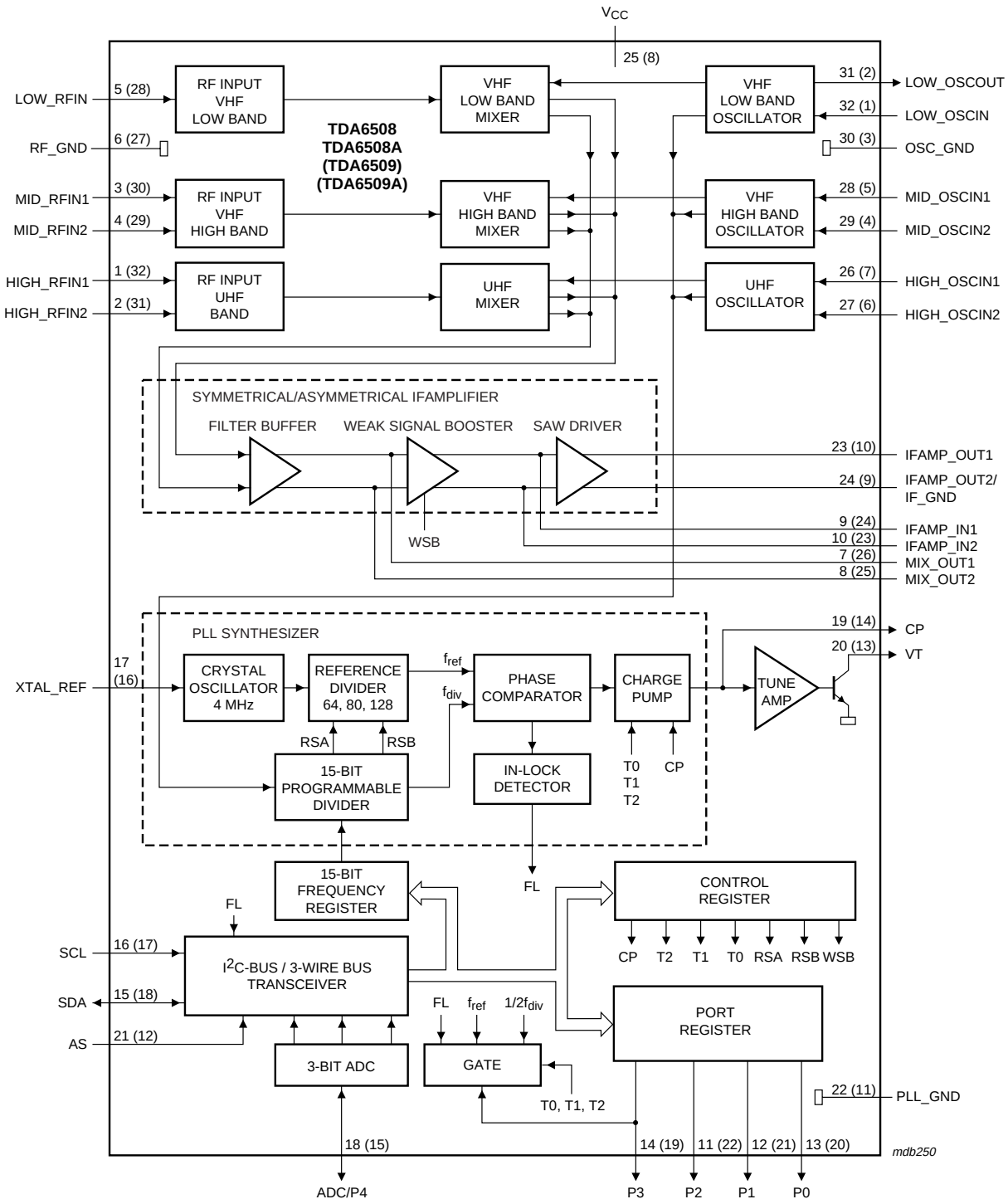
Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5	5.5	V
I_{CC}	supply current	V_{CC} = 5 V; all ports off	43	58	74	mA
f_{xtal}	crystal oscillator frequency	R_{xtal} = 25 Ω to 300 Ω	3.58	4.0	4.43	MHz
P_{tot}	total power dissipation		–	290	385	mW
T_{stg}	IC storage temperature		−40	–	+150	°C
T_{amb}	ambient temperature		−20	–	+85	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6508TT	TSSOP32	plastic thin shrink small outline package; 32 leads body width 6.1 mm	SOT487-1
TDA6508ATT			
TDA6509TT	TSSOP32	plastic thin shrink small outline package; 32 leads body width 6.1 mm	SOT487-1
TDA6509ATT			
TDA6509HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1
TDA6509AHN			

6 BLOCK DIAGRAM



(1) 'A' versions only.

The pin numbers in parenthesis refer to versions TDA6509 and TDA6509A.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6508; TDA6508A	TDA6509; TDA6509A	
HIGH_RFIN1	1	32	HIGH band RF input 1
HIGH_RFIN2	2	31	HIGH band RF input 2
MID_RFIN1	3	30	MID band RF input 1
MID_RFIN2	4	29	MID band RF input 2
LOW_RFIN	5	28	LOW band RF input
RF_GND	6	27	RF ground
MIX_OUT1	7	26	mixer output 1 (to external IF filter)
MIX_OUT2	8	25	mixer IF output 2 (to external IF filter)
IFAMP_IN1	9	24	IF amplifier input 1 (from external IF filter)
IFAMP_IN2	10	23	IF amplifier input 2 (from external IF filter)
P2	11	22	HIGH band port output
P1	12	21	MID band port output
P0	13	20	LOW band port output
P3	14	19	general purpose port - test mode output
SDA	15	18	serial data input/output
SCL	16	17	serial clock input
XTAL_REF	17	16	crystal oscillator reference signal input
ADC/P4	18	15	ADC input/general purpose port output
CP	19	14	charge-pump output
VT	20	13	tuning voltage output
AS	21	12	address selection input
PLL_GND	22	11	PLL ground
IFAMP_OUT1	23	10	IF amplifier output 1
IFAMP_OUT2	24	9	IF amplifier output 2 (TDA6508 and TDA6509 only)
IF_GND	24	9	IF ground (TDA6508A and TDA6509A only)
V_{CC}	25	8	supply voltage
HIGH_OSCIN1	26	7	HIGH band oscillator input 1
HIGH_OSCIN2	27	6	HIGH band oscillator input 2
MID_OSCIN1	28	5	MID band oscillator input 1
MID_OSCIN2	29	4	MID band oscillator input 2
OSC_GND	30	3	oscillator ground
LOW_OSCOUT	31	2	LOW band oscillator output
LOW_OSCIN	32	1	LOW band oscillator input

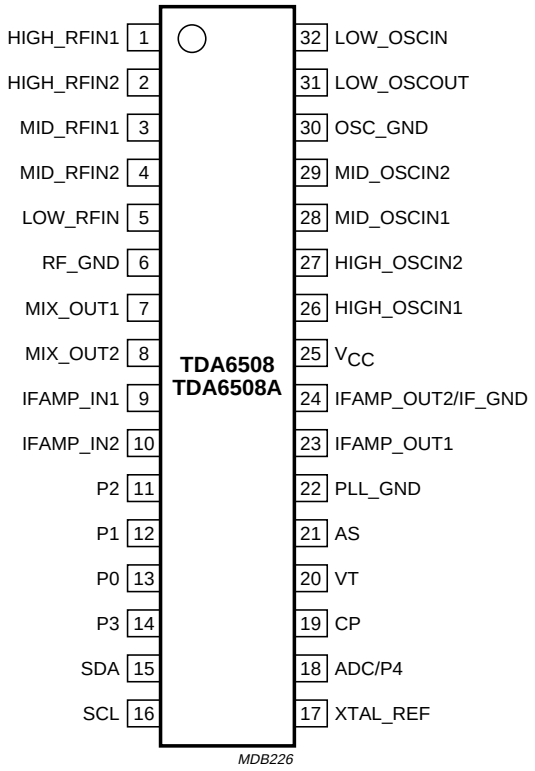


Fig.2 Pin configuration for TDA6508 and TDA6508A (TSSOP32).

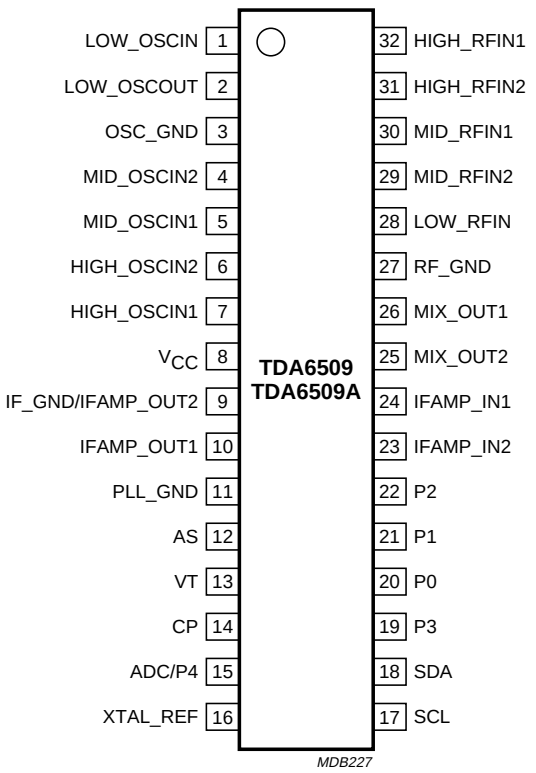


Fig.3 Pin configuration for TDA6509 and TDA6509A (TSSOP32).

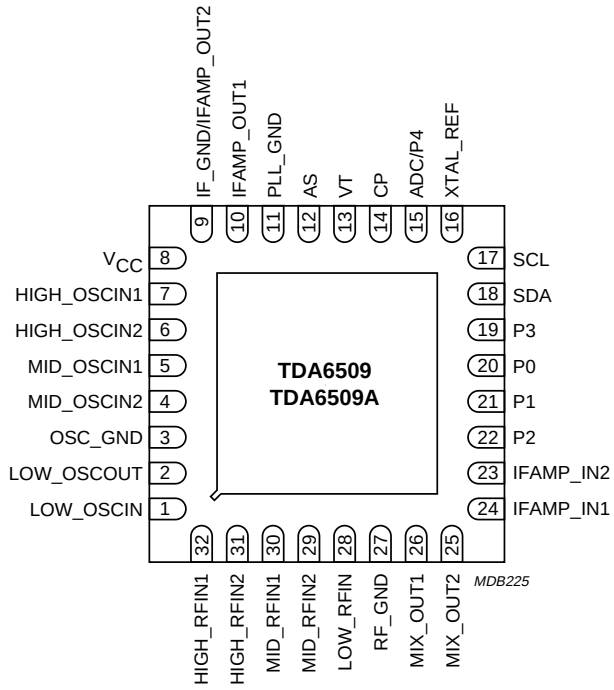


Fig.4 Pin configuration for TDA6509 and TDA6509A (HVQFN32).

8 I²C-BUS DATA FORMAT

8.1 I²C-bus address selection

The address byte ADB contains programmable module address bits MA1 and MA0 which allow up to four synthesizers to be used in the same system, and are configured by applying one of four possible voltages on pin AS; see Tables 1 and 2. For each voltage on pin AS, the resultant values of bits MA1 and MA0 are shown in Table 3.

8.2 Write mode

The write mode is defined by setting bit R/$\overline{W}$ to logic 0 in address byte ADB; see Table 1.

Data bytes can be sent to the device after sending the first address byte. Four data bytes are required to fully program the device.

The bus transceiver has an auto-increment facility which allows the device to be programmed by one transmission (address byte with 4 data bytes). The device can be partially programmed provided that the first data byte following the address byte is divider byte DB1 or control byte CB.

The MSB of the first data byte DB1 indicates whether frequency data (MSB = 0) or control and band switch data will follow. Additional data bytes can be entered without the need to re-address the device until an I²C-bus STOP command is sent by the controller.

The frequency divider register is loaded after the 8th clock pulse of byte DB2. The control register is loaded after the 8th clock pulse of byte CB, and the band switch register is loaded after the 8th clock pulse of byte BB.

Table 1 I^2C-bus data format for write mode

NAME	BYTE	BITS(1)							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	WSB
Band switch byte	BB	X	X	X	P4	P3	P2	P1	P0

Note

1. X = don't care.

Table 2 Function of write mode bits used in Table 1

BIT	FUNCTION
MA1 and MA0	module address; see Table 3
R/$\overline{W}$	read/write mode; 0 = write mode
N14 to N0	programmable divider bits: $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$
CP	charge-pump current control: 0: charge-pump current is 20 μA 1: charge-pump current is 100 μA
T2, T1 and T0	test mode; see Table 5
RSA and RSB	reference divider ratio; see Table 4
WSB	Weak Signal Booster control: 0: normal mode - no gain increase: external IF filter used 1: Weak Signal Booster activated: IF filter by-passed
P0, P1, P2, P3, P4	port P0 to P4 control: 0: corresponding port is off; high impedance state (default) 1: corresponding port is on.

Table 3 Module address selection bits

MA1	MA0	VOLTAGE APPLIED TO PIN AS
0	0	0 V to $0.1V_{CC}$
0	1	$0.2V_{CC}$ to $0.3V_{CC}$ or open-circuit
1	0	$0.4V_{CC}$ to $0.6V_{CC}$
1	1	$0.9V_{CC}$ to $1.0V_{CC}$

Table 4 Reference divider ratio selection bits

RSA	RSB	REFERENCE DIVIDER RATIO	FREQUENCY STEP (kHz)(1)
X	0	80	50
0	1	128	31.25
1	1	64	62.5

Note

1. Crystal oscillator frequency or externally sourced reference frequency of 4 MHz at pin XTAL_REF.

Table 5 Test mode selection bits

T2	T1	T0	TEST MODE
0	0	0	normal mode (read and write mode bytes allowed)
0	0	1	normal mode (read and write mode bytes allowed)(1)
0	1	0	charge-pump is off(2)
0	1	1	byte BB ignored
1	1	0	charge-pump sinks current
1	1	1	charge-pump sources current
1	0	0	$\frac{1}{2}f_{ref}$ is output from port P3(3)
1	0	1	$\frac{1}{2}f_{div}$ is output from port P3(3)

Notes

1. This is the default mode at power-on reset.
2. $\frac{1}{2}f_{div}$ is output from port P3 when the charge-pump is off.
3. Port P3 cannot be used when these test modes are active.

8.3 Read mode

The read mode is defined by setting bit R/$\overline{W}$ to logic 1 in address byte ADB; see Table 6.

After the slave address has been recognized, the device generates an acknowledge pulse, and status byte SB is transferred on the SDA line (MSB first). Data is valid on the SDA line when pin SCL is HIGH. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge).

End of transmission will occur if no master acknowledge is asserted. The device will then release the data line to allow the microcontroller to generate a STOP condition.

Bit POR is set to logic 1 at power-on. This bit is reset when an end-of-data is detected by the device at the end of a read sequence. Bit FL controls the PLL by indicating when the loop is locked (bit FL = 1).

The internal ADC can be used to apply AFC information to a microcontroller in the IF section of the television via status byte bits A0, A1 and A2. Up to five voltage levels can be applied to the ADC input pin ADC; the resultant values of bits A2, A1 and A0 are shown in Table 8.

Table 6 Read data format

NAME	BYTE	BIT							
		MSB(1)							**LSB**
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1
Status byte	SB	POR	FL	1	1	1	A2	A1	A0

Note

1. MSB is transmitted first.

Table 7 Description of the bits used in Table 6

BIT	DESCRIPTION
MA1 and MA0	programmable address bits; see Table 3
R/$\overline{W}$	read/write mode selection; 1 = read mode
POR	Power-on reset flag: 0: after end of the first read sequence 1: at Power-on
FL	in-lock flag: 0: loop is not locked 1: loop is locked
A2, A1 and A0	digital outputs of the 5-level ADC; see Table 8

Table 8 Digital outputs for analog to digital converter (note 1)

A2	A1	A0	VOLTAGE APPLIED TO PIN ADC
0	0	0	0 V_{CC} to 0.15 V_{CC}
0	0	1	0.15 V_{CC} to 0.3 V_{CC}
0	1	0	0.3 V_{CC} to 0.45 V_{CC}
0	1	1	0.45 V_{CC} to 0.6 V_{CC}
1	0	0	0.6 V_{CC} to 1 V_{CC}

Note

1. Accuracy is $\pm 0.03 \times V_{CC}$.

8.4 Power-on reset

The threshold level for the power-on reset supply voltage V_{POR} is set to 3.2 V at room temperature. Below this threshold, the device is reset to the power-on state.

The following actions take place In the power-on state:

- The charge-pump current is set to 100 μA
- Test bits T2, T1 and T0 are set to logic 001; the charge-pump can either sink or source current
- The Weak signal booster is disabled
- All ports are off and the HIGH band is selected by default.

Table 9 Default setting of the bits at power-on reset

NAME	BYTE	BITS[1]							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	X
Divider byte 1	DB1	0	X	X	X	X	X	X	X
Divider byte 2	DB2	X	X	X	X	X	X	X	X
Control byte	CB	1	1	0	0	1	X	X	0
Band switch byte	BB	X	X	X	0	0	0	0	0

Note

1. X = don't care.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PIN		PARAMETER	MIN.	MAX.	UNIT
	TDA6508; TDA6508A	TDA6509; TDA6509A				
V_{CC}	25	8	DC supply voltage	–0.3	+6	V
			operating supply	4.5	5.5	V
V_{Pn}	11, 12, 13, 14, 18	22, 21, 20, 19, 15	PMOS port output voltage	–0.3	V_{CC} + 0.3	V
I_{Pn}	11, 12, 13	22, 21, 20	PMOS port output current	–20	0	mA
	14, 18	19, 15		–5	0	mA
V_{VT}	20	13	tuning voltage output	–0.3	+35	V
V_{SCL}	16	17	serial clock input voltage	–0.3	+6	V
V_{SDA}	15	18	serial data input or output voltage	–0.3	+6	V
I_{SDA}	15	18	serial data output current	0	+10	mA
V_{AS}	21	12	address selection input voltage	–0.3	+6	V
V_{xtal}	17	16	crystal input voltage	–0.3	V_{CC} + 0.3	V
$t_{sc(max)}$	–	–	maximum short-circuit time (all pins to V_{CC} and all pins to all grounds)	–	10	s
T_{stg}	–	–	storage temperature	–40	+150	°C
T_{amb}	–	–	ambient temperature	–20	+85	°C
T_j	–	–	junction temperature	–	+150	°C

Note

1. Maximum ratings can not be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings can not be accumulated.

10 HANDLING

Human Body Model: C = 100 pF and R = 1500 Ω. All pins withstand 2000 V in accordance with specification *EIA/JESD22-A114-A*.

Machine model: C = 200 pF and R = 0 Ω. All pins withstand 200 V in accordance with specification *EIA/JESD22-A115-A*.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air - SOT487-5[1]	115	K/W
		in free air - SOT487-4[1]	125	K/W
		in free air - SOT617-1	31	K/W

Note

1. JEDEC conditions apply to single layer PCB.

12 CHARACTERISTICS

V_{CC} = 5 V, T_{amb} = 25 °C; TDA6508 and TDA6509 values measured with R_L = 1.25 kΩ and TDA6508A and TDA6509A values measured with R_L = 75 Ω; Weak signal booster off; measured using the PAL application circuit shown in Figure 27; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	at V_{CC} = 5 V; all ports off	43	58	74	mA
FUNCTIONAL RANGE						
V_{POR}	power-on reset supply voltage	power-on reset activates below this voltage	–	3.2	–	V
N	divider ratio	15-bit frequency word	64	–	32767	–
f_{xtal}	crystal oscillator frequency	R_{xtal} = 25 Ω to 300 Ω	3.58	4.0	4.43	MHz
$\lvert Z_{xtal} \rvert$	input impedance (absolute value)	f_{xtal} = 4 MHz	1000	1200	–	Ω
PMOS PORTS: PINS P0, P1, P2, P3, P4						
$I_{L(Pn)}$	leakage current	V_{CC} = 5.5 V; V_{Pn} = 0 V or 5.5 V	–10	–	+120	µA
$V_{Pn(sat)}$	output saturation voltage	$V_{Pn(sat)} = V_{CC} - V_{Pn}$				
		one buffer output is on and sourcing 5 mA	–	0.25	0.4	V
		one buffer output is on and sourcing 20 mA	–	0.25	0.4	V
ADC INPUT: PIN ADC (IN I^2C BUS MODE)						
V_{ADC}	ADC input voltage	see Table 8	0	–	V_{CC}	V
$I_{ADC(H)}$	HIGH level input current	$V_{ADC} = V_{CC}$	–	–	100	µA
$I_{ADC(L)}$	LOW level input current	V_{ADC} = 0 V	–10	–	–	µA
ADDRESS SELECTION INPUT: PIN AS						
$I_{AS(H)}$	HIGH level input current	V_{AS} = 5 V	–	–	10	µA
$I_{AS(L)}$	LOW level input current	V_{AS} = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLOCK AND DATA INPUTS: PINS SCL AND SDA						
$V_{SCL(L)}$, $V_{SDA(L)}$	LOW level input voltage		0	–	1.5	V
$V_{SCL(H)}$, $V_{SDA(H)}$	HIGH level input voltage		2.3	–	5.5	V
$I_{SCL(H)}$, $I_{SDA(H)}$	HIGH level input current	V_{bus} = 5.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{bus} = 5.5 V; V_{CC} = 5.5 V	–	–	10	µA
$I_{SCL(L)}$, $I_{SDA(L)}$	LOW level input current	V_{bus} = 1.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{bus} = 0 V; V_{CC} = 5.5 V	–10	–	–	µA
DATA OUTPUT: PIN SDA						
$I_{L(SDA)}$	leakage current	V_{SDA} = 5.5 V	–	–	10	µA
$V_{SDA(H)}$	HIGH level output voltage	I_{SDA} = 3 mA (sink current)	–	–	0.4	V
CLOCK FREQUENCY (I^2C-BUS MODE)						
f_{clk}	clock frequency		–	–	400	kHz
CHARGE-PUMP OUTPUT: PIN CP						
$\|I_{CP(H)}\|$	HIGH level input current (absolute value)	CP = 1	–	100	115	µA
$\|I_{CP(L)}\|$	LOW level input current (absolute value)	CP = 0	15	20	–	µA
$I_{L(CP)}$	off-state leakage current	T2 = 0; T1 = 1; T0 = 0	–15	0	+15	nA
TUNING VOLTAGE OUTPUT: PIN VT						
$I_{tune(off)}$	leakage current when switched-off	T2 = 1; T1 = 1; T0 = 0; tuning supply is 33 V	–	–	10	µA
$V_{o(tune)}$	output voltage when loop is closed	T2 = 0; T1 = 0; T0 = 1; R_L = 33 kΩ; tuning supply is 33 V	0.3	–	32.7	V
LOW MIXER (INCLUDING IF PREAMPLIFIER)						
$f_{RF(o)}$	RF operational frequency		40	–	800	MHz
f_{RF}	RF frequency	f_{pc}; note 1	43.25	–	161.25	MHz
G_v	voltage gain	TDA6508; TDA6509; IF output loaded with 1.25 kΩ				
		f_{RF} = 46 MHz; see Fig.10	22	25	28	dB
		f_{RF} = 164 MHz; see Fig.10	22	25	28	dB
		TDA6508A; TDA6509A; IF output loaded with 75 Ω				
		f_{RF} = 46 MHz; see Fig.11	18	21	24	dB
		f_{RF} = 164 MHz; see Fig.11	18	21	24	dB
NF	noise figure	f_{RF} = 50 MHz; see Figs 12 and 13	–	8	10	dB
		f_{RF} = 150 MHz; see Fig.13	–	8	10	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_o	output voltage (causing 1% cross-modulation in channel)	TDA6508; TDA6509				
		f_{RF} = 43.25 MHz; see Fig.15	114	117	–	dBμV
		f_{RF} = 161.25 MHz; see Fig.15	114	117	–	dBμV
		TDA6508A; TDA6509A				
		f_{RF} = 43.25 MHz; see Fig.16	106	109	–	dBμV
		f_{RF} = 161.25 MHz; see Fig.16	106	109	–	dBμV
V_i	input voltage (causing pulling in channel at 750 Hz)	f_{RF} = 161.25 MHz; note 2	–	90	–	dBμV
g_{os}	optimum source conductance for noise figure	f_{RF} = 50 MHz	–	0.7	–	mS
g_i	input conductance	f_{RF} = 43.25 MHz; see Fig.5	–	0.3	–	mS
		f_{RF} = 161.25 MHz; see Fig.5	–	0.3	–	mS
C_i	input capacitance	f_{RF} = 43.25 to 161.25 MHz; see Fig.5	–	1	–	pF
LOW OSCILLATOR						
$f_{osc(o)}$	oscillator operational frequency		60	–	600	MHz
f_{osc}	oscillator frequency	note 3	82.15	–	200.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency variation with supply voltage	ΔV_{CC} = 5%; note 4	–	20	–	kHz
		ΔV_{CC} = 10%; note 4	–	50	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency variation with temperature	ΔT = ±25 °C; with compensation; note 5	–	900	–	kHz
		ΔT = 35 °C; without compensation; note 5	–	1700	–	kHz
Φ_{osc}	phase noise, carrier-to-noise sideband	worst case in the frequency range				
		±100 kHz frequency offset	–	–110	–107	dBc/Hz
		±10 kHz frequency offset	–	–90	–87	dBc/Hz
$RSC_{(p-p)}$	ripple susceptibility of V_{CC} (peak-to-peak value)	4.75 V < V_{CC} < 5.25 V; worst case in the frequency range; ripple frequency 500 kHz; note 6	15	90	–	mV
FM_{mod}	FM modulation caused by I^2C communication	worst case; note 7	–	–	2.12	kHz
MID MIXER (INCLUDING IF PREAMPLIFIER)						
$f_{O(RF)}$	RF operational frequency		40	–	800	MHz
f_{RF}	RF frequency	f_{pc}; note 1	154.25	–	447.25	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_v	voltage gain	TDA6508; TDA6509; IF output loaded with 1.25 kΩ				
		f_{RF} = 157 MHz; see Fig.17	22	25	28	dB
		f_{RF} = 450 MHz; see Fig.17	22	25	28	dB
		TDA6508A; TDA6509A; IF output loaded with 75 Ω				
		f_{RF} = 157 MHz; see Fig.18	18	21	24	dB
		f_{RF} = 450 MHz; see Fig.18	18	21	24	dB
NF	noise figure	f_{RF} = 150 MHz; see Figs 12 and 13	–	8	10	dB
		f_{RF} = 300 MHz; see Figs 12 and 13	–	8	10	dB
V_o	output voltage (causing 1% cross-modulation in channel)	TDA6508; TDA6509				
		f_{RF} = 154.25 MHz; see Fig.19	114	117	–	dBμV
		f_{RF} = 447.25 MHz; see Fig.19	114	117	–	dBμV
		TDA6508; TDA6509A				
		f_{RF} = 154.25 MHz; see Fig.20	106	109	–	dBμV
		f_{RF} = 447.25 MHz; see Fig.20	106	109	–	dBμV
V_i	input voltage (causing pulling in channel at 750 Hz)	f_{RF} = 447.25 MHz; note 2	–	90	–	dBμV
g_{os}	optimum source conductance for noise figure	f_{RF} = 150 MHz	–	0.9	–	mS
		f_{RF} = 300 MHz	–	1.5	–	mS
g_i	input conductance	f_{RF} = 154.25 MHz	–	0.21	–	mS
		f_{RF} = 447.25 MHz	–	1.8	–	mS
C_i	input capacitance	f_{RF} = 154.25 to 447.25 MHz	–	0.6	–	pF
MID OSCILLATOR						
$f_{osc(o)}$	oscillator operational frequency		60		600	MHz
f_{osc}	oscillator frequency	note 3	193.15	–	486.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency variation with supply voltage	ΔV_{CC} = 5%; note 4	–	15	–	kHz
		ΔV_{CC} = 10%; note 4	–	40	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency variation with temperature	ΔT = ±25 °C; with compensation; note 5	–	1200	–	kHz
		ΔT = 35 °C; without compensation; note 5	–	2000	–	kHz
Φ_{osc}	phase noise, carrier-to-noise sideband	worst case in the frequency range				
		±100 kHz frequency offset	–	–109	–106	dBc/Hz
		±10 kHz frequency offset	–	–87	–86	dBc/Hz
$RSC_{(p-p)}$	ripple susceptibility of V_{CC} (peak-to-peak value)	4.75 V < V_{CC} < 5.25 V; worst case in the frequency range; ripple frequency 500 kHz; note 6	15	70	–	mV
FM_{mod}	FM modulation caused by I^2C communication	worst case; note 7	–	–	2.12	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HIGH MIXER (INCLUDING IF PREAMPLIFIER)						
$f_{O(RF)}$	RF operational frequency		200		900	MHz
f_{RF}	RF frequency	f_{pc}; note 1	439.25	–	863.25	MHz
G_v	voltage gain	TDA6508; TDA6509; IF output loaded with 1.25 kΩ				
		f_{RF} = 442 MHz; see Fig.21	33	36	39	dB
		f_{RF} = 866 MHz; see Fig.21	33	36	39	dB
		TDA6508A; TDA6509A; IF output loaded with 75 Ω				
		f_{RF} = 442 MHz; see Fig.22	29	32	35	dB
		f_{RF} = 866 MHz; see Fig.22	29	32	35	dB
NF	noise figure (not corrected for image)	f_{RF} = 439.25 MHz; see Fig.23	–	7	9	dB
		f_{RF} = 863.25 MHz; see Fig.23	–	7	9	dB
V_o	output voltage (causing 1% cross-modulation in channel)	TDA6508; TDA6509				
		f_{RF} = 439.25 MHz; Fig.25	114	117	–	dBμV
		f_{RF} = 863.25 MHz; Fig.25	114	117	–	dBμV
		TDA6508A; TDA6509A				
		f_{RF} = 439.25 MHz; Fig.26	106	109	–	dBμV
		f_{RF} = 863.25 MHz; Fig.26	106	109	–	dBμV
V_i	input voltage (causing pulling in channel at 750 Hz)	f_{RF} = 863.25 MHz; note 2	–	75	–	dBμV
Z_i	input impedance ($R_S + j\omega L_S$)	R_S at f_{RF} = 439.25 MHz	–	28	–	Ω
		R_S at f_{RF} = 863.25 MHz	–	34	–	Ω
		L_S at f_{RF} = 439.25 MHz	–	8	–	nH
		L_S at f_{RF} = 863.25 MHz	–	8	–	nH
HIGH OSCILLATOR						
$f_{osc(o)}$	oscillator operational frequency		300		1000	MHz
f_{osc}	oscillator frequency	note 3	478.15	–	902.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency variation with supply voltage	ΔV_{CC} = 5%; note 4	–	40	–	kHz
		ΔV_{CC} = 10%; note 4	–	80	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency variation with temperature	ΔT = ±25 °C; with compensation; note 5	–	2700	–	kHz
		ΔT = 35 °C; without compensation; note 5	–	4100	–	kHz
Φ_{osc}	phase noise, carrier-to-noise sideband	worst case in the frequency range				
		±100 kHz frequency offset	–	–105	–102	dBc/Hz
		±10 kHz frequency offset	–	–85	–82	dBc/Hz
$RSC_{(p-p)}$	ripple susceptibility of V_{CC} (peak-to-peak value)	4.75 V < V_{CC} < 5.25 V; worst case in the frequency range; ripple frequency 500 kHz; note 6	15	50	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM_{mod}	FM modulation caused by I^2C communication	worst case; note 7	–	–	3.0	kHz
WEAK SIGNAL BOOSTER						
$\Delta G_{v(WSB)}$	gain increase when the weak signal booster mode is activated	TDA6508; TDA6509; IF = 36.15 MHz	13	16	–	dB
		TDA6508A; TDA6509A; IF = 36.15 MHz	7	10	–	dB
IF PREAMPLIFIER						
$f_{O(IF)}$	IF operational frequency		5		60	MHz
Z_o	output impedance ($R_S + j\omega L_S$)	TDA6508; TDA6509				
		R_S at 36.15 MHz	–	100	–	Ω
		L_S at 36.15 MHz	–	52	–	nH
		TDA6508A; TDA6509A				
		R_S at 36.15 MHz	–	40	–	Ω
		L_S at 36.15 MHz	–	12	–	nH
REJECTION AT THE IF OUTPUT						
INT_{div}	level of divider interferences in the IF signal	worst case; note 8	–	24	–	dBμV
IR_{xtal}	crystal oscillator interferences rejection	worst case in the frequency range; note 9	60	80	–	dBc
R_{ref}	reference frequency rejection	worst case in the frequency range; f_{ref} = 62.5 kHz; note 10	60	66	–	dBc
INT_{SO2}	channel SO2 beat	V_{pc} = 80 dBμV; note 11	60	66	–	dBc

Notes

1. The range of f_{RF} is defined by the range of f_{osc} and I; f_{pc} = picture carrier frequency.
2. V_i is the level of f_{RF} (100% amplitude modulated with 11.89 kHz) that causes the frequency of the oscillator signal to deviate by 750 Hz; it produces sidebands 30 dB below the level of the oscillator signal.
3. Limits are related to the tank circuits used in Fig.27; frequency bands may be adjusted by the choice of external components.
4. The oscillator frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 V to 4.75 V (or 5 V to 4.5 V) or from V_{CC} = 5 V to 5.25 V (or 5 V to 5.5 V). The oscillator is free running during this measurement.
5. The oscillator frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from T_{amb} = 25 °C to 50 °C (60 °C max.) or from T_{amb} = 25 °C to 0 °C. The oscillator is free running during this measurement. For $\Delta T = \pm 25$ °C measurements, the tank circuit has temperature compensated values; for ΔT = 35 °C measurements, the tank circuit has non-temperature compensated values.
6. The ripple susceptibility is measured with a 500 kHz ripple signal applied to the supply voltage. The level of the ripple signal is increased until a difference of 53.5 dB occurs between the level of the IF carrier, fixed at 110 dBμV for TDA6508; TDA6509 or 100 dBμV for TDA6508A; TDA6509A, and the sideband components.
7. FM modulation of the local oscillator resulting from I^2C-bus communication is measured at the IF output using a modulation analyzer with a peak-to-peak detector and a post detection filter of 20 Hz to 100 kHz. I^2C-bus messages sent to the tuner address the tuner without changing the contents of the PLL registers. The maximum I^2C-bus clock rate is 400 kHz. The I^2C-bus pull-up resistor values are 1.5 kΩ.

8. This is the level of signals close to the IF frequency which can interfere with the dividers. Typical interference signals are channel S3: f_{osc} = 256.15 MHz, $^{5}/_{32}$ f_{osc} = 40.02 MHz. The LOW and MID RF inputs must not be connected to any load or cable; the HIGH RF inputs are connected to a hybrid (balun).
9. Crystal oscillator interference is the 4 MHz sidebands produced by the crystal oscillator. The rejection must be greater than 60 dB for an IF output signal of 110 dBµV for versions TDA6508; TDA6509 or 100 dBµV for versions TDA6508A; TDA6509A.
10. Reference frequency rejection measures the level of reference frequency sidebands with respect to the sound sub-carrier f_{ssc}.
11. Channel SO2 beat is the interfering product of the picture carrier frequency f_{pc}, f_{IF} and f_{OSC} in channel SO2: $f_{BEAT} = f_{osc} - 2 \times f_{IF}$ = 37.35 MHz. Another possible mechanism is: $2 \times f_{pc} - f_{osc}$. For the measurement, V_{RF} = 80 dBµV.

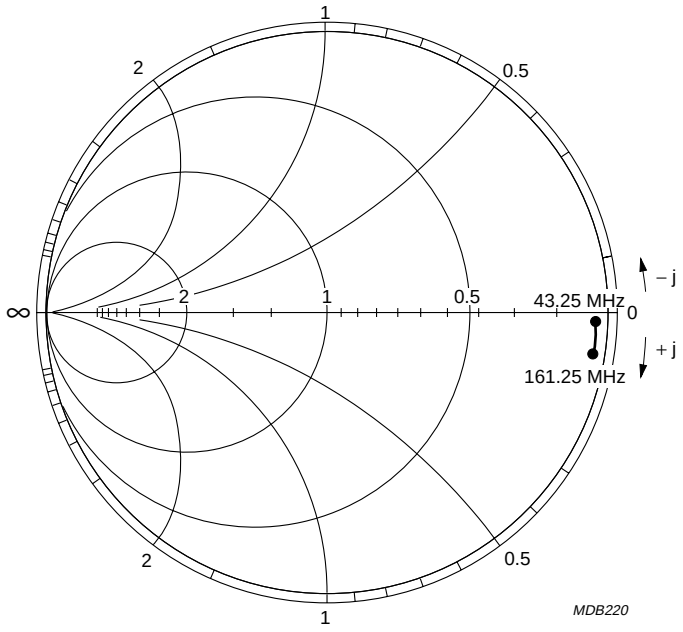


Fig.5 Input admittance (S_{11}) of the LOW band mixer (43.25 to 161.25 MHz); Y_O = 20 mS.

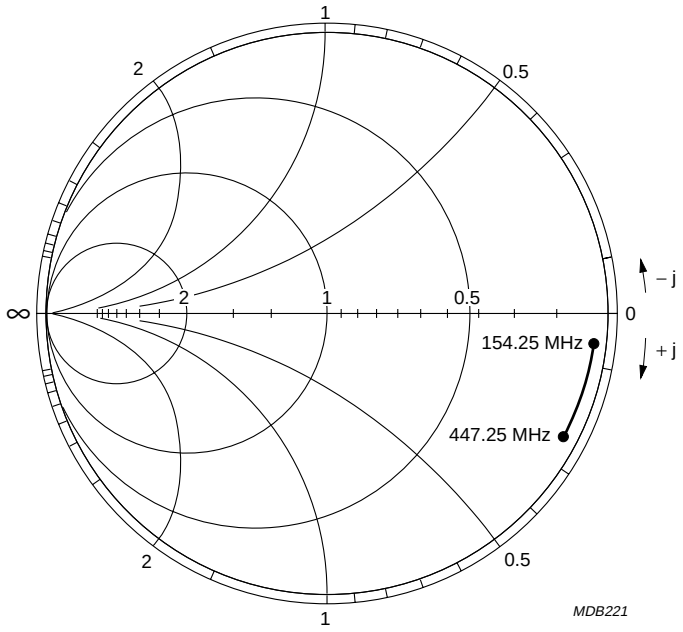


Fig.6 Input admittance (S_{11}) of the MID band mixer (154.25 to 447.25 MHz); Y_O = 10 mS.

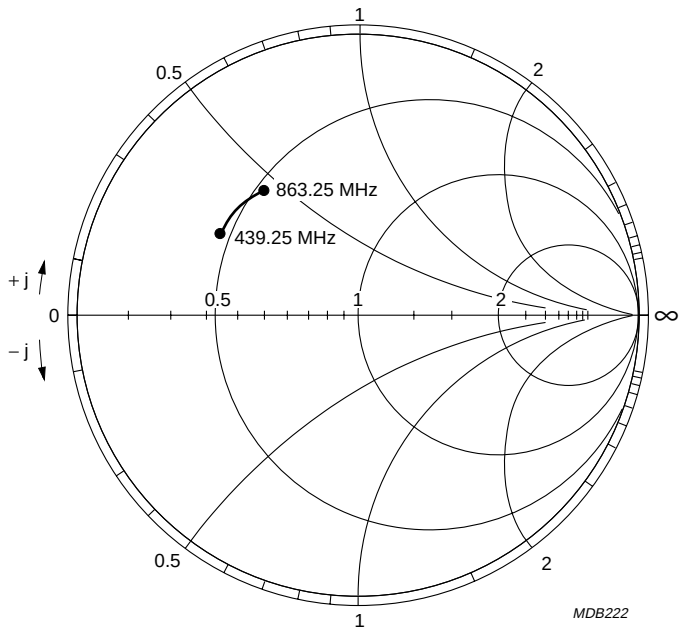


Fig.7 Input impedance (S_{11}) of the HIGH band mixer (439.25 to 863.25 MHz); Z_O = 100 Ω.

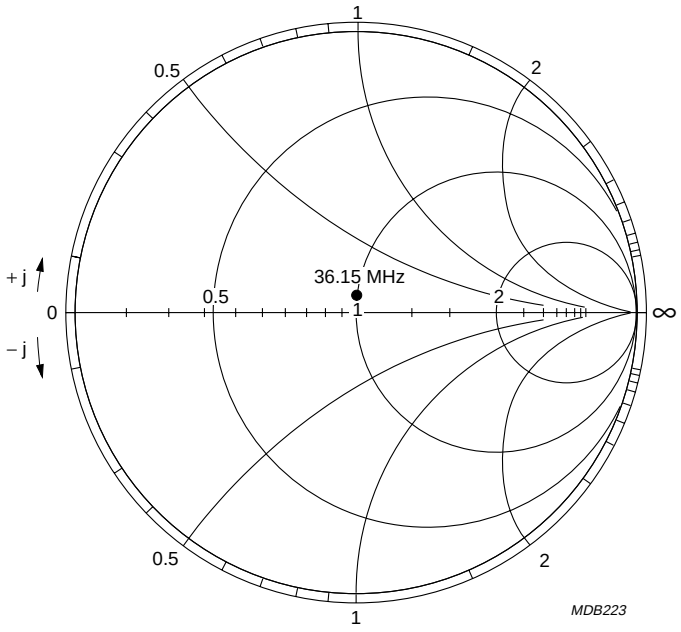


Fig.8 Output impedance of TDA6508; TDA6509; Z_O = 100 Ω.

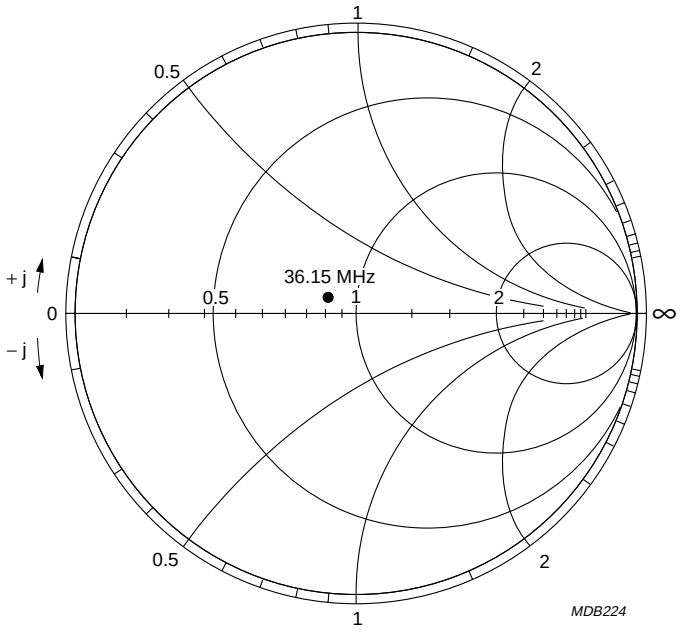
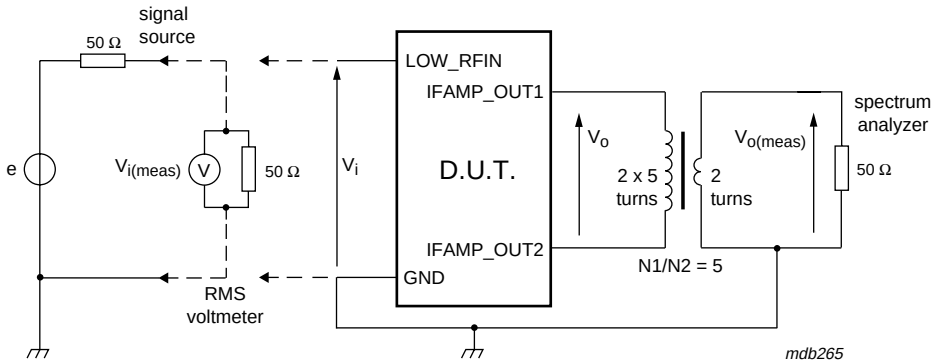


Fig.9 Output impedance of TDA6508A; TDA6509A; Z_O = 50 Ω.

13 TEST AND APPLICATION INFORMATION

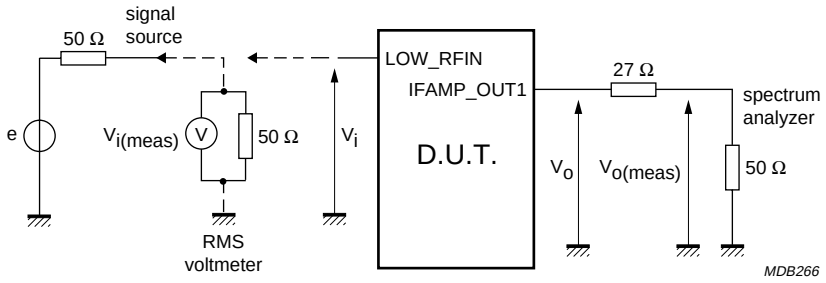


$Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{i(meas)} = 80\ dB\mu V$.
$V_i = V_{i(meas)} + 6\ dB = 80\ dB\mu V$.
$V_o = V_{o(meas)} + 15\ dB$ (transformer ratio N1/N2 and transformer loss).

$$G_v = 20 \log \frac{V_o}{V_i}$$

PAL $f_{IF} = 36.15$ MHz.

Fig.10 Gain measurement in the LOW-band of the TDA6508; TDA6509.

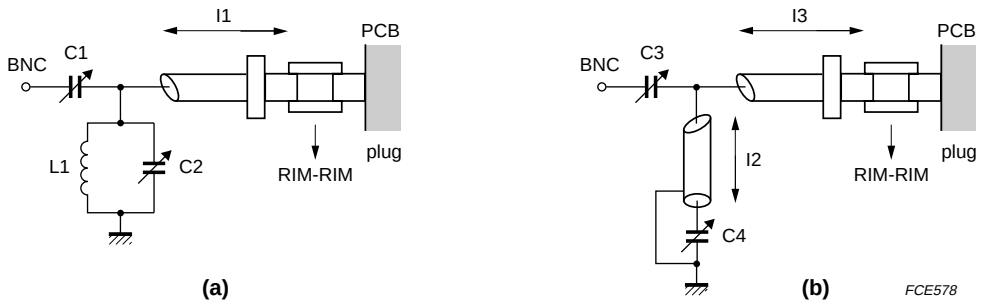


$Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{i(meas)} = 80\ dB\mu V$.
$V_i = V_{i(meas)} + 6\ dB = 80\ dB\mu V$.
$V_o = V_{o(meas)} + 3.75\ dB$.

$$G_v = 20 \log \frac{V_o}{V_i}$$

PAL $f_{IF} = 36.15$ MHz.

Fig.11 Gain measurement in the LOW-band of the TDA6508A; TDA6509A.



(a) f_{RF} = 50 MHz:

LOW band mixer frequency response measured = 57 MHz, loss = 0 dB.

image suppression = 16 dB.

C1 = 9 pF.

C2 = 15 pF.

L1 = 7 turns (∅ 5.5 mm, wire ∅ = 0.5 mm).

l1 = semi-rigid (RIM) cable, length = 5 cm (33 dB/100 m, 50 Ω and 96 pF/m).

(b) For f_{RF} = 150 MHz:

MID band mixer frequency response measured = 150.3 MHz, loss = 0 dB.

image suppression = 13 dB.

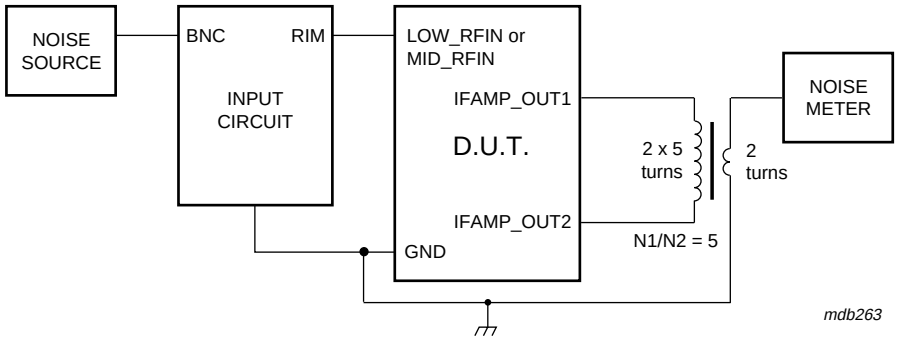
C3 = 5 pF.

C4 = 25 pF.

l2 = semi-rigid (RIM) cable, length = 30 cm.

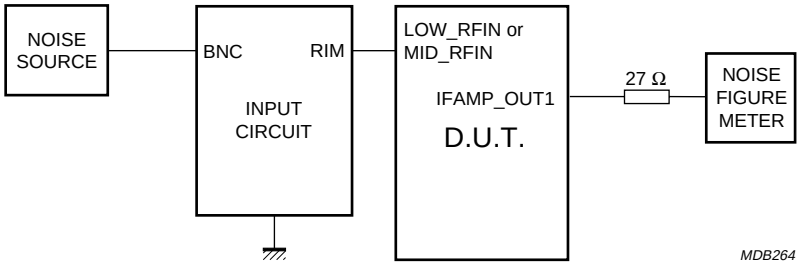
l3 = semi-rigid (RIM) cable, length = 5 cm (33 dB/100 m, 50 Ω and 96 pF/m).

Fig.12 Input circuit for optimum noise figure in LOW and MID-bands.



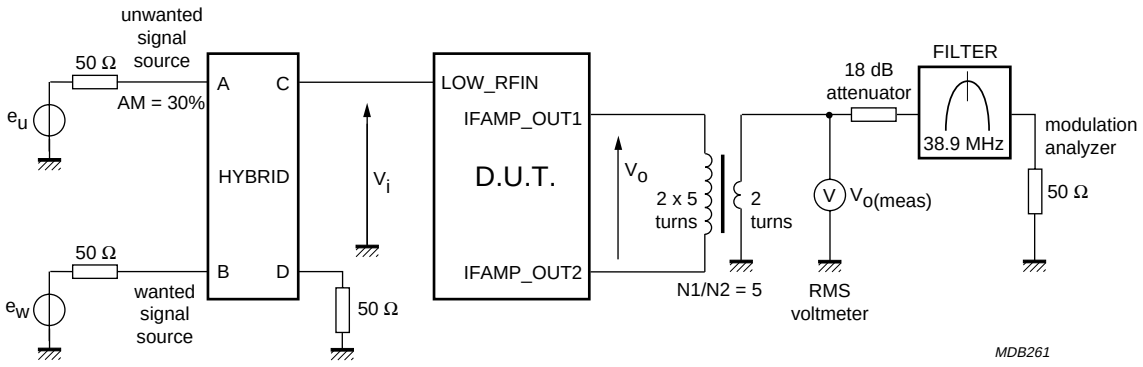
NF = NF_{meas} – input circuit loss (dB).

Fig.13 Noise figure measurement in the LOW and MID-bands of the TDA6508; TDA6509.



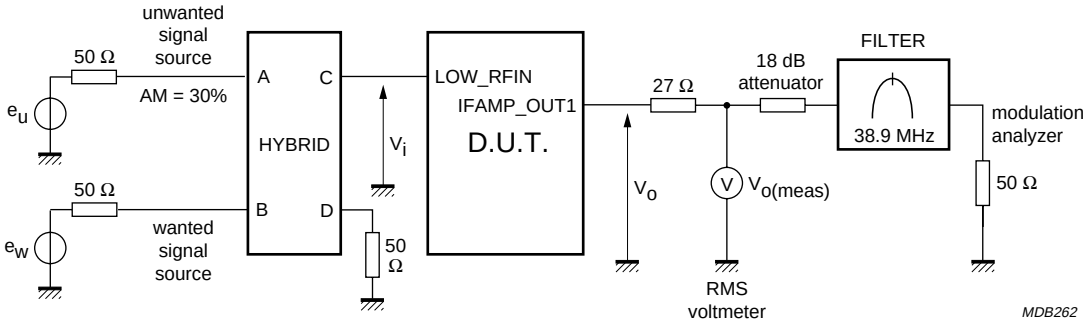
NF = f_{meas} – input circuit loss (dB).

Fig.14 Noise figure measurement in the LOW and MID-bands of the TDA6508A; TDA6509A.



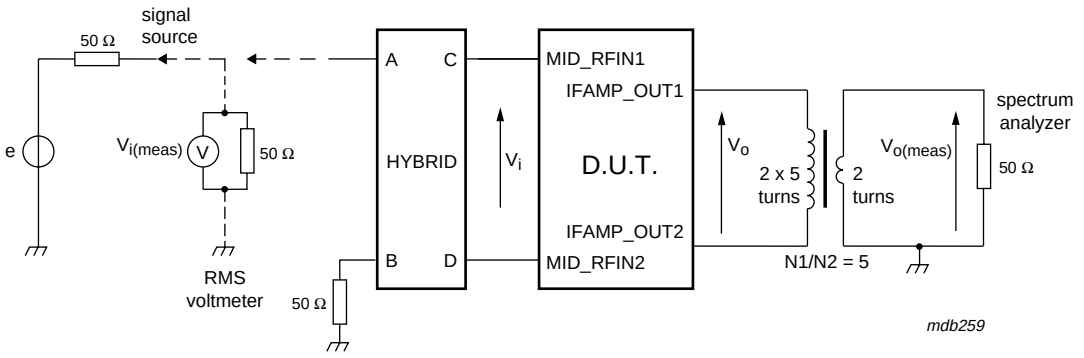
$V_o = V_{o(meas)}$ + 15 dB (transformer ratio N1/N2 and transformer loss).
Wanted output signal at picture carrier frequency $f_{RF(w)}$; $V_{o(w)}$ = 110 dBμV.
Unwanted output signal at sound sub-carrier frequency $f_{RF(u)}$; AM = 30%; AF = 2 kHz.
Measuring the level of unwanted signal causing 0.3% AM in the wanted signal.
$f_{RF(w)}$ = 43.25 MHz (min); 161.25 MHz (max).
$f_{RF(u)}$ = 48.75 MHz (min); 166.75 MHz (max).
f_{osc} = 82.15 MHz (min); 200.15 MHz (max.).

Fig.15 Cross-modulation measurement in the LOW-band of the TDA6508; TDA6509.



$V_o = V_{o(meas)}$ + 3.75 dB (transformer ratio N1/N2 and transformer loss).
Wanted output signal at picture carrier frequency $f_{RF(w)}$; $V_{o(w)}$ = 100 dBμV.
Unwanted output signal at sound sub-carrier frequency $f_{RF(u)}$; AM = 30%; AF = 2 kHz.
Measuring the level of unwanted signal causing 0.3% AM in the wanted signal.
$f_{RF(w)}$ = 43.25 MHz (min.); 161.25 MHz (max.).
$f_{RF(u)}$ = 48.75 MHz (min.); 166.75 MHz (max.).
f_{osc} = 82.15 MHz (min.); 200.15 MHz (max.).

Fig.16 Cross-modulation measurement in the LOW-band of the TDA6508A; TDA6509A.

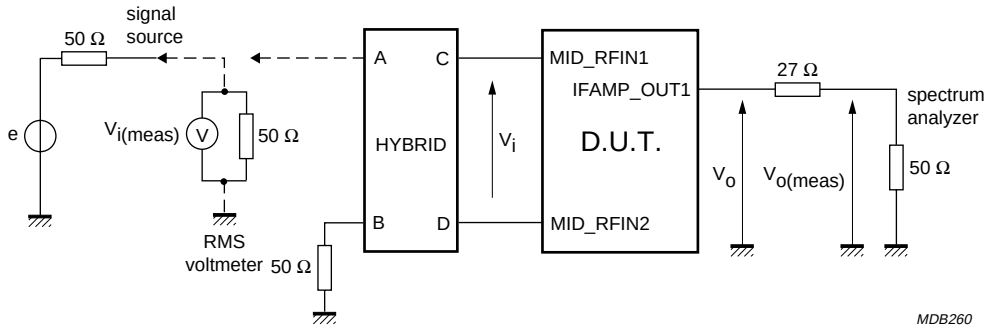


Z_i >> 50 Ω, symmetrical input.
Hybrid loss = 1 dB.
$V_i = V_{i(meas)}$ – loss + 6 + 3 = 80 dBμV.
$V_o = V_{o(meas)}$ + 15 dB (transformer ratio N1/N2 and transformer loss).

$$G_v = 20 \log \frac{V_o}{V_i}$$

PAL f_{IF} = 36.15 MHz.

Fig.17 Gain measurement in the MID-band of the TDA6508; TDA6509.

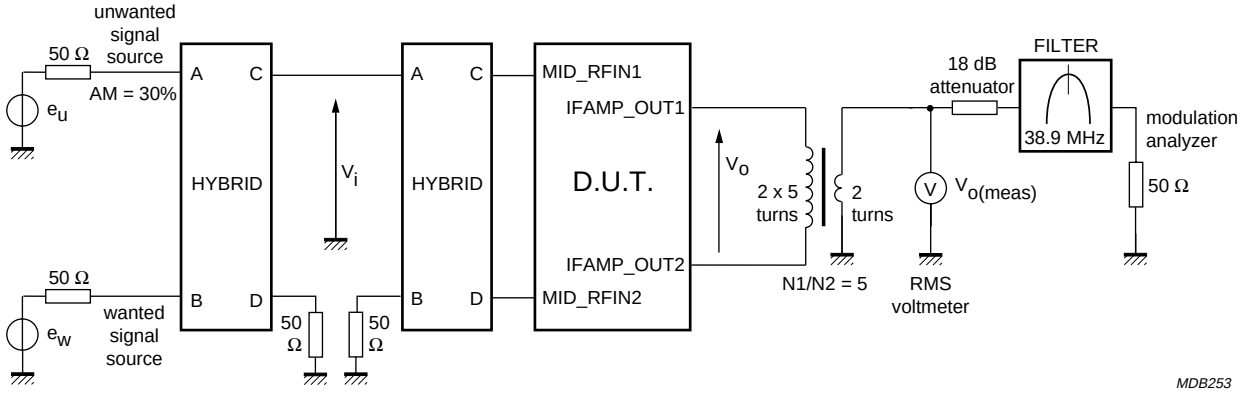


Z_i >> 50 Ω symmetrical input.
Hybrid loss = 1 dB.
$V_i = V_{i(meas)}$ – loss + 6 + 3 = 80 dBμV.
$V_o = V_{o(meas)}$ + 3.75 dB.

$$G_v = 20 \log \frac{V_o}{V_i}$$

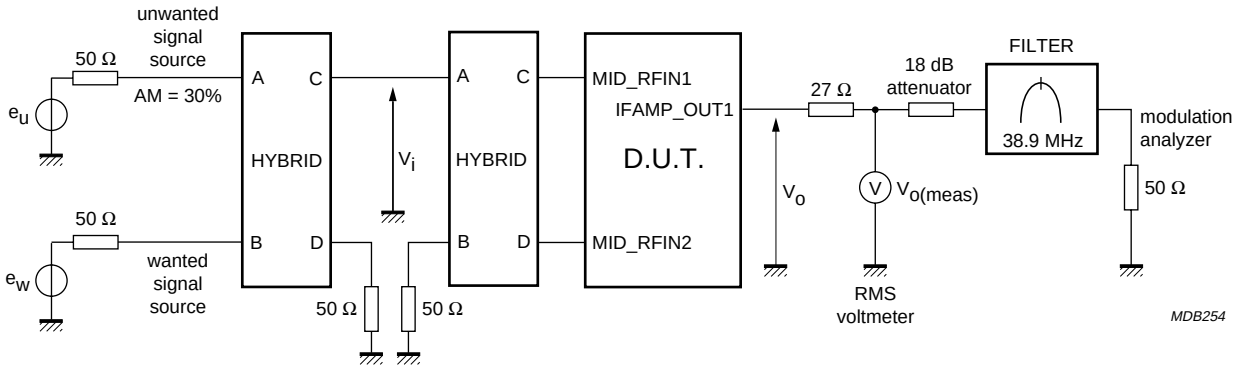
PAL f_{IF} = 36.15 MHz.

Fig.18 Gain measurement in the MID-band of the TDA6508A; TDA6509A.



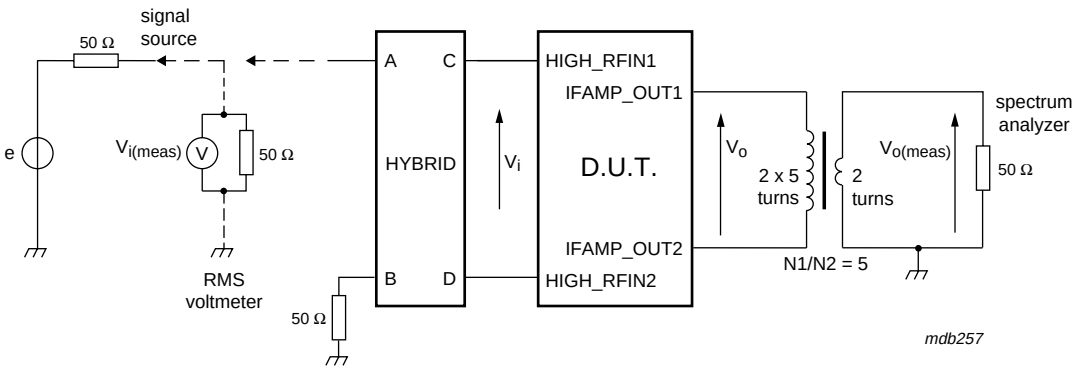
$V_o = V_{o(meas)}$ + 15 dB (transformer ratio N1/N2 and transformer loss).
Wanted output signal at picture carrier frequency $f_{RF(w)}$; $V_{o(w)}$ = 110 dBμV.
Unwanted output signal at sound sub-carrier frequency $f_{RF(u)}$; AM = 30%; AF = 2 kHz.
Measuring the level of unwanted signal causing 0.3% AM in the wanted signal.
$f_{RF(w)}$ = 154.25 MHz (min.); 447.25 MHz (max.).
$f_{RF(u)}$ = 159.75 MHz (min.); 452.75 MHz (max.).
f_{osc} = 193.15 MHz (min.); 486.15 MHz (max.).

Fig.19 Cross-modulation measurement in the MID-band of the TDA6508; TDA6509.



$V_o = V_{o(meas)} + 3.75$ dB.
Wanted output signal at fpix; $V_{o(w)} = 100$ dBµV.
Unwanted output signal at fsnd; AM = 30%; AF = 2 kHz.
Measuring the level of unwanted signal causing 0.3% AM in the wanted signal.
$f_{RF(w)} = 154.25$ MHz (min.); 447.25 MHz (max.).
$f_{RF(u)} = 159.75$ MHz (min.); 452.75 MHz (max.).
$f_{osc} = 193.15$ MHz (min.); 486.15 MHz (max.).

Fig.20 Cross-modulation measurement in the MID-band of the TDA6508A; TDA6509A.

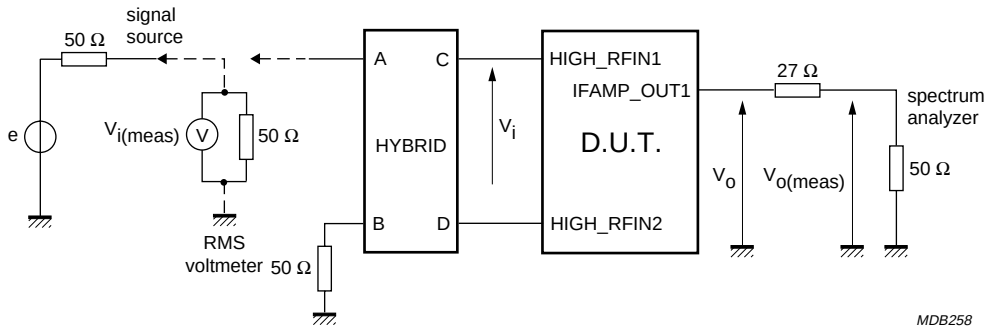


Hybrid loss = 1 dB.
$V_i = V_{i(meas)}$ – loss = 70 dBµV.
$V_o = V_{o(meas)}$ + 15 dB (transformer ratio N1/N2 and transformer loss).

$$G_v = 20 \log \frac{V_o}{V_i}$$

PAL $f_{IF} = 36.15$ MHz.

Fig.21 Gain measurement in the HIGH-band of the TDA6508; TDA6509.



Hybrid loss = 1 dB.

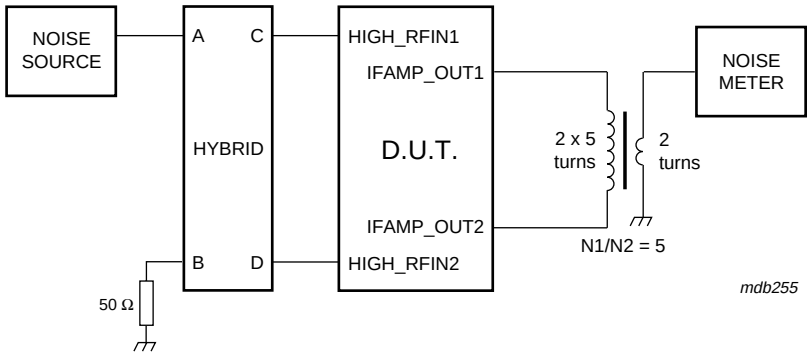
$V_i = V_{i(meas)}$ – loss = 70 dBµV.

$V_o = V_{o(meas)}$ + 3.75 dB.

$G_v = 20 \log \frac{V_o}{V_i}$

PAL f_{IF} = 36.15 MHz.

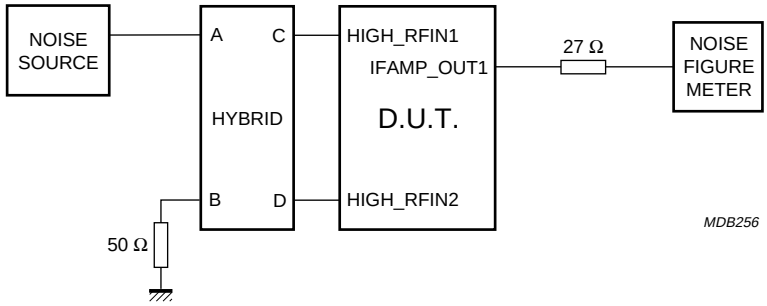
Fig.22 Gain measurement in the HIGH-band of the TDA6508A; TDA6509A.



Hybrid loss = 1 dB.

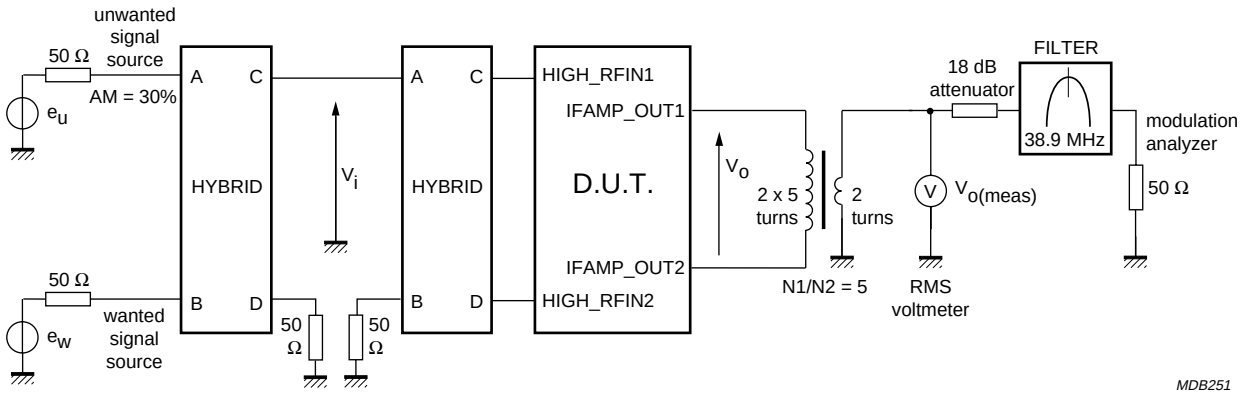
$NF = NF_{meas}$ – hybrid loss.

Fig.23 Noise figure measurement in the HIGH-band of the TDA6508; TDA6509.



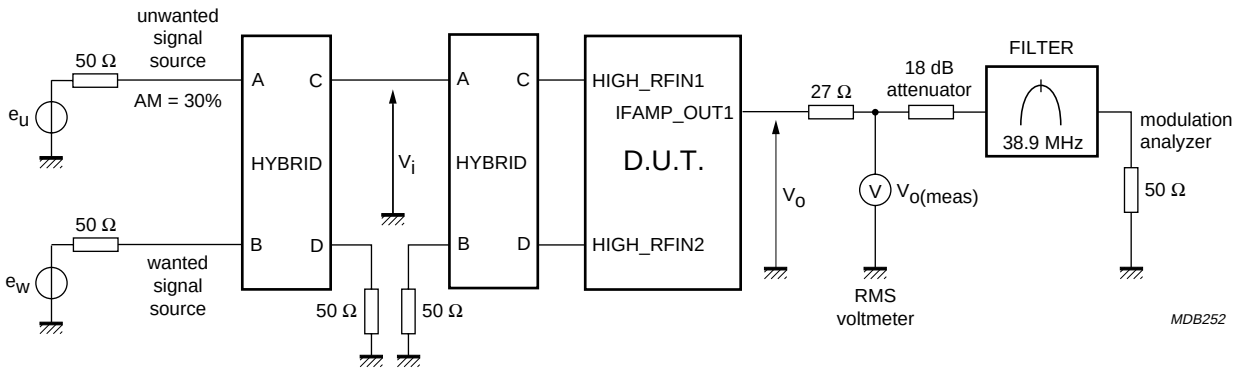
Hybrid loss = 1 dB.
NF = NF_{meas} − hybrid loss.

Fig.24 Noise figure measurement in the HIGH-band of the TDA6508A; 6509A.



$V_o = V_{o(meas)}$ + 15 dB (transformer ratio N1/N2 and transformer loss).
Wanted output signal at picture carrier frequency $f_{RF(w)}$; $V_{o(w)}$ = 110 dBμV.
Unwanted output signal at sound sub-carrier frequency $f_{RF(u)}$; AM = 30%; AF = 2 kHz.
Measuring the level of unwanted signal causing 0.3% AM in the wanted signal.
$f_{RF(w)}$ = 439.25 MHz (min.); 863.25 MHz (max.).
$f_{RF(u)}$ = 444.75 MHz (min.); 868.75 MHz (max.).
f_{osc} = 478.15 MHz (min.); 902.15 MHz (max.).

Fig.25 Cross-modulation measurement in the HIGH-band of the TDA6508; TDA6509.



$V_o = V_{o(meas)} + 3.75$ dB.
Wanted output signal at picture carrier frequency $f_{RF(w)}$; $V_{o(w)}$ = 100 dBμV.
Unwanted output signal at sound sub-carrier frequency $f_{RF(u)}$; AM = 30%; AF = 2 kHz.
We measure the level of unwanted signal causing 0.3% AM modulation in the wanted signal
$f_{RF(w)}$ = 439.25 MHz (min.); 863.25 MHz (max.).
$f_{RF(u)}$ = 444.75 MHz (min.); 868.75 MHz (max.).
f_{osc} = 478.15 MHz (min.); 902.15 MHz (max.).

Fig.26 Cross-modulation measurement in the HIGH-band of the TDA6508A; TDA6509A.

13.1 Measurement circuit

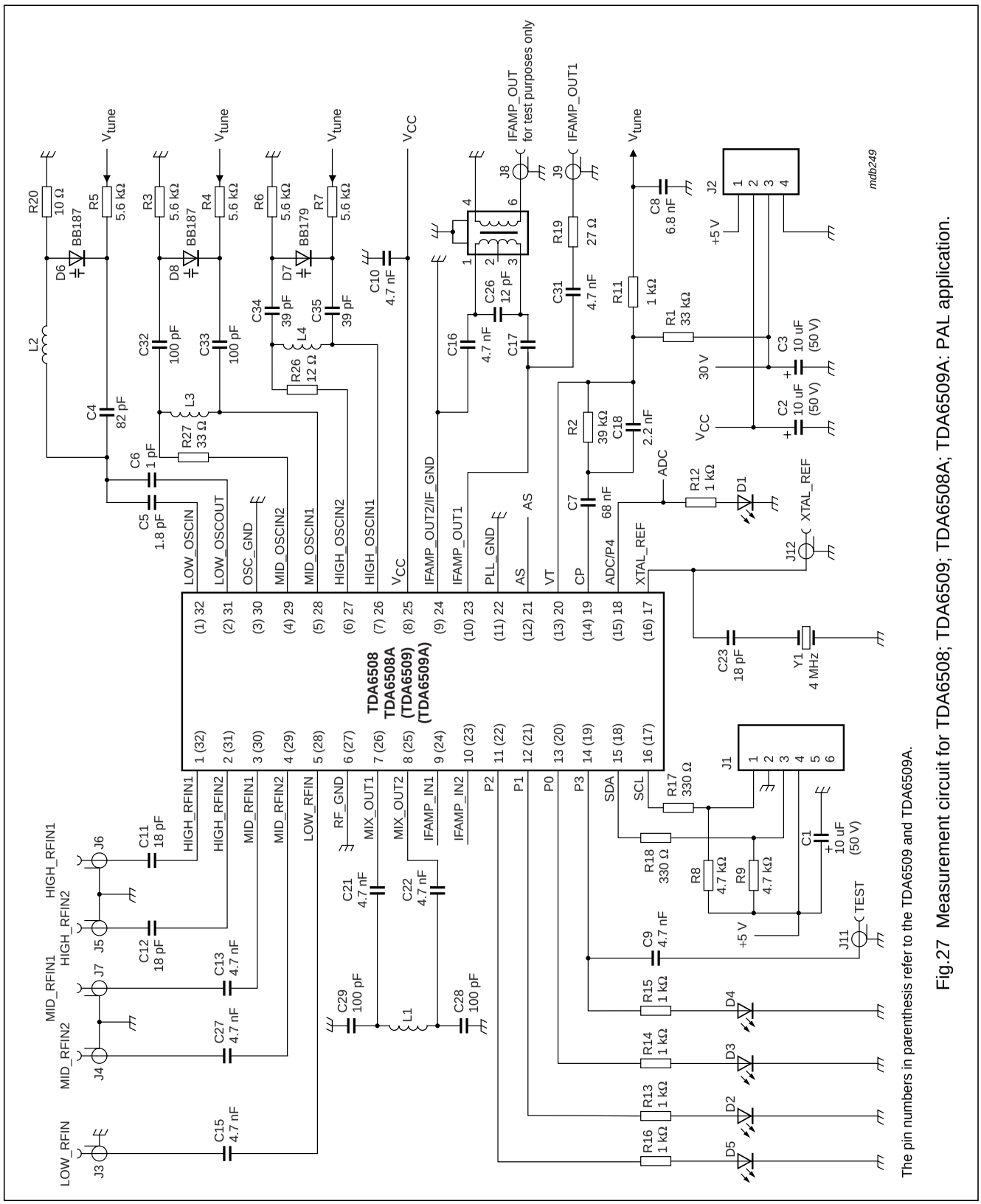
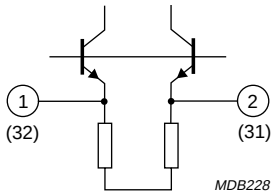
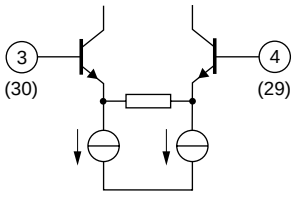
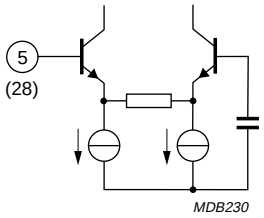
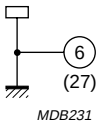
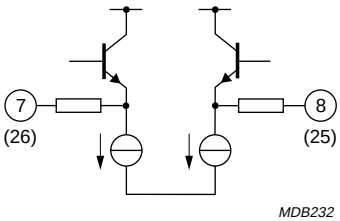
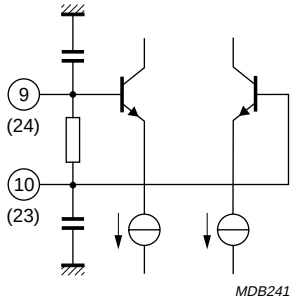
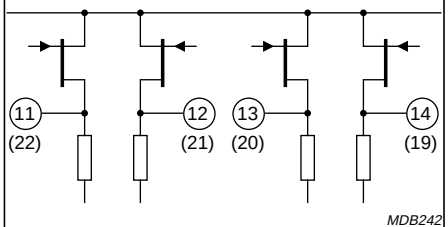
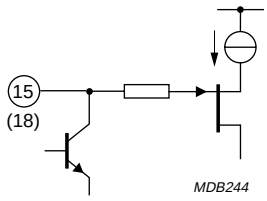
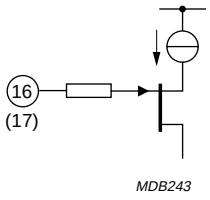
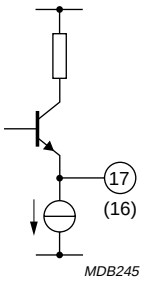


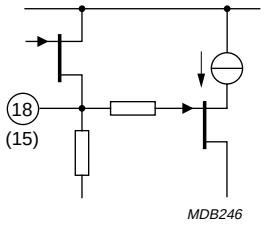
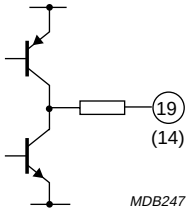
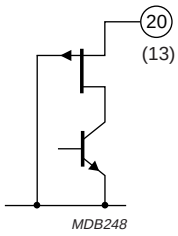
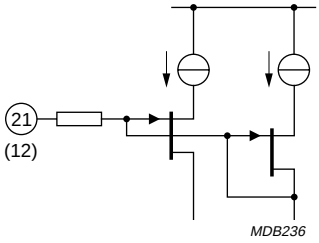
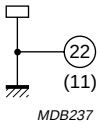
Fig.27 Measurement circuit for TDA6508; TDA6509; TDA6508A; TDA6509A: PAL application.

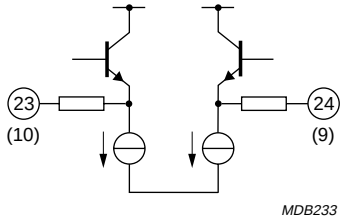
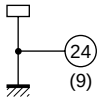
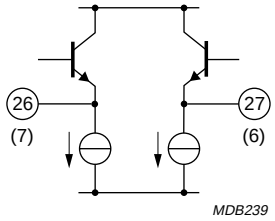
The pin numbers in parenthesis refer to the TDA6509 and TDA6509A.

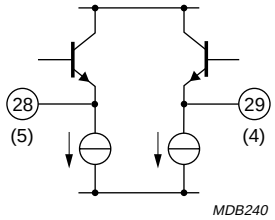
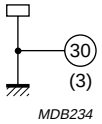
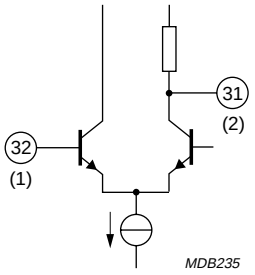
14 INTERNAL PIN CONFIGURATION

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V)		
	TDA6508	TDA6509		LOW	MID	HIGH
HIGH_RFIN1, HIGH_RFIN2	1, 2	32, 31		–	–	1.0
MID_RFIN1, MID_RFIN2	3, 4	30, 29		–	1.0	–
LOW_RFIN	5	28		1.8	–	–
RF_GND	6	27		–	–	–
MIX_OUT1, MIX_OUT2	7, 8	26, 25		2.9	2.9	2.9

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V)		
	TDA6508	TDA6509		LOW	MID	HIGH
IFAMP_IN1, IFAMP_IN2	9, 10	24, 23		3.0	3.0	3.0
P0, P1, P2, P3	13, 12, 11, 14	20, 21, 22, 19		high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$
SDA	15	18		high-Z	high-Z	high-Z
SCL	16	17		high-Z	high-Z	high-Z
XTAL_REF	17	16		1.6	1.6	1.6

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V)		
	TDA6508	TDA6509		LOW	MID	HIGH
ADC/P4	18	15		high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$
CP	19	14		1.0	1.0	1.0
VT	20	13		V_{VT}	V_{VT}	V_{VT}
AS	21	12		1.25	1.25	1.25
PLL_GND	22	11		0	0	0

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V)		
	TDA6508	TDA6509		LOW	MID	HIGH
IFAMP_OUT1, IFAMP_OUT2	23, 24	10, 9		2.0	2.0	2.0
IF_GND	24	9		0	0	0
V_{CC}	25	8	supply voltage	5	5	5
HIGH_OSCIN1	26, 27	7, 6		2.3	2.3	1.3

SYMBOL	PIN		DESCRIPTION(1)	AVERAGE DC VOLTAGE (V)		
	TDA6508	TDA6509		LOW	MID	HIGH
MID_OSCIN1	28, 29	5, 4		2.3	1.3	2.3
OSC_GND	30	3		0	0	0
LOW_OSCOUT, LOW_OSCIN	31, 32	2, 1		1.7, 2.9	1.4, 3.5	1.4, 3.5

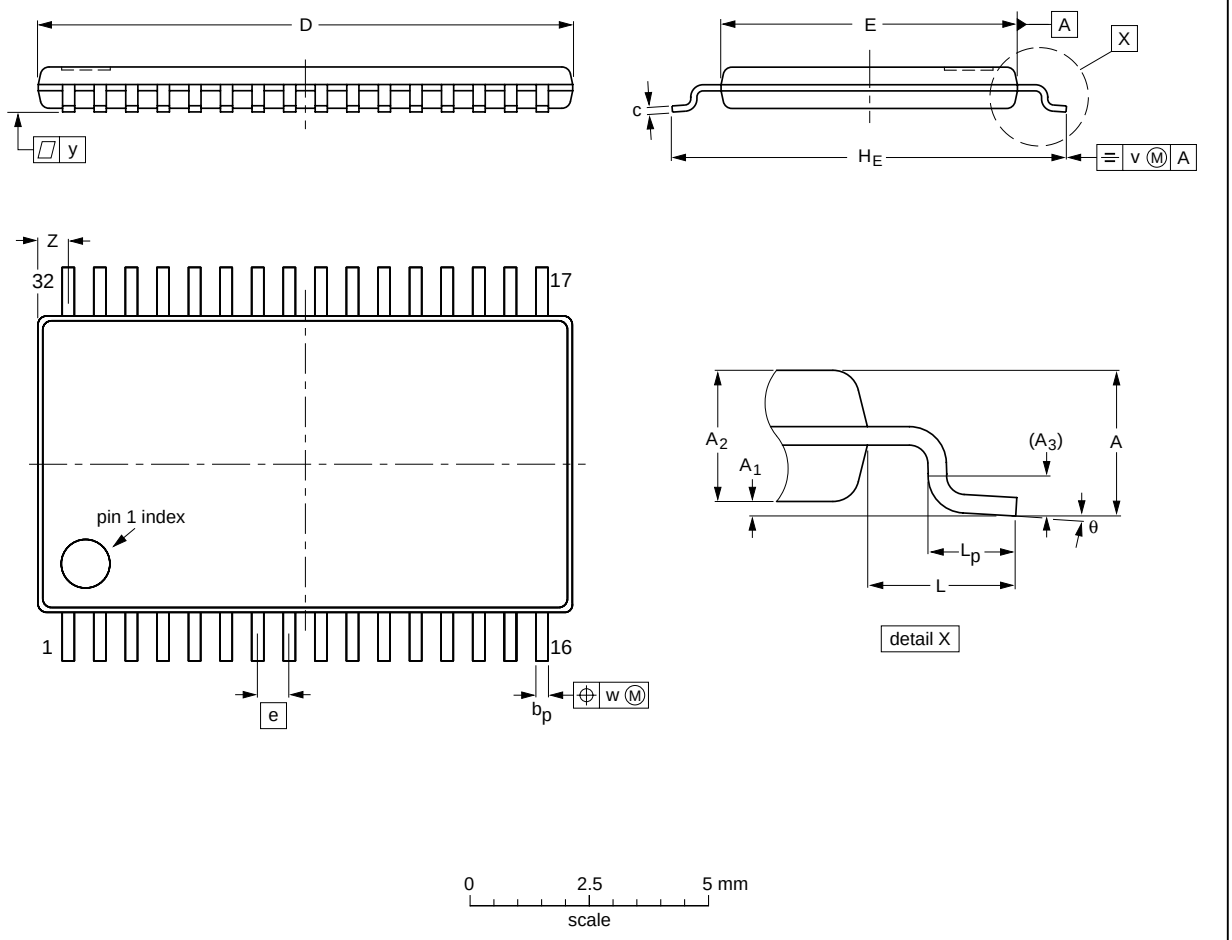
Note

1. The pin numbers in parenthesis apply to the TDA6508TT.

15 PACKAGE OUTLINES

TSSOP32: plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm

SOT487-1



DIMENSIONS (mm are the original dimensions)

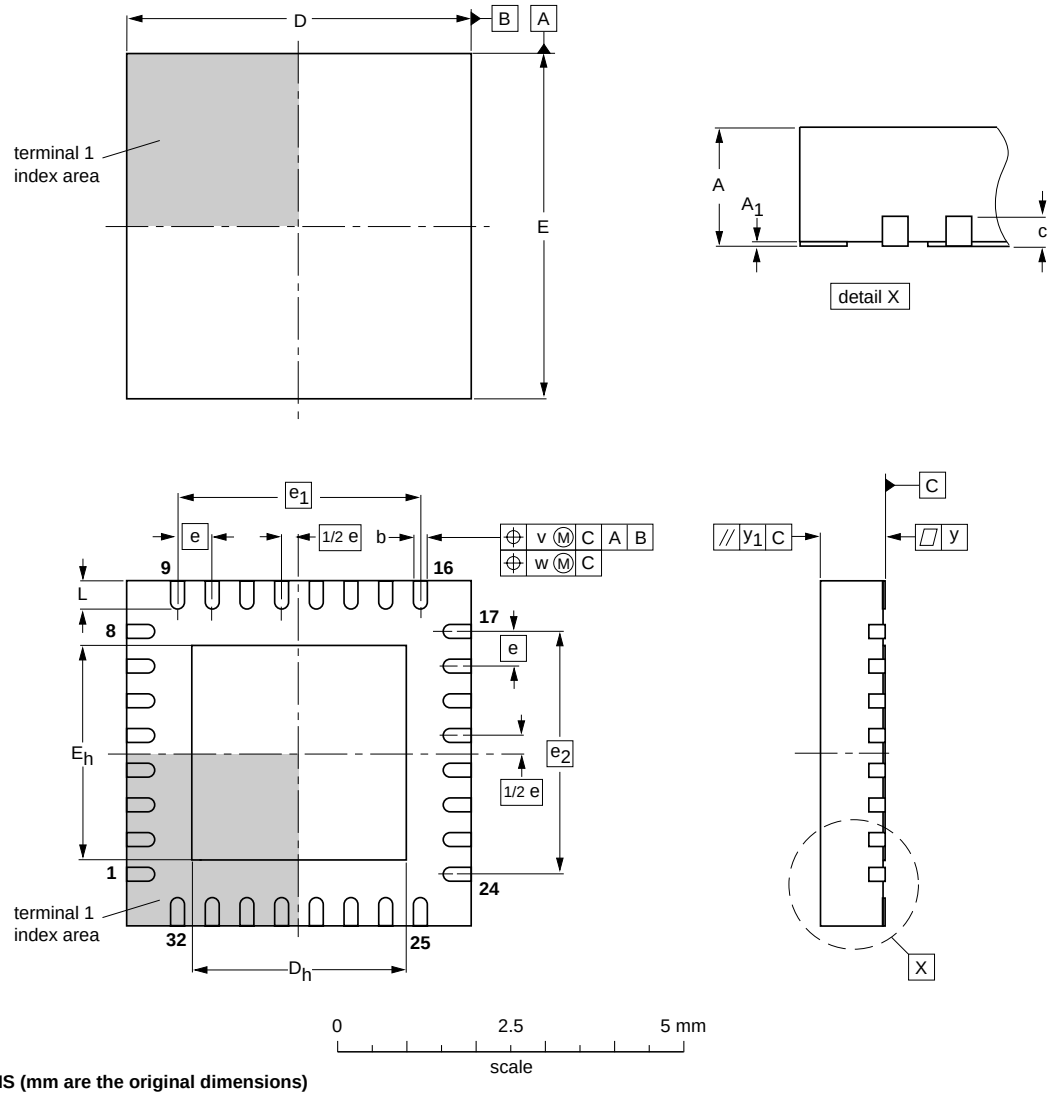
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	6.2 6.0	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT487-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar soldering or manual soldering is suitable for PMFP packages.

17 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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