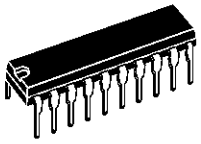
SGS-THOMSON MICROELECTRONICS

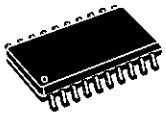
TDA7319

3 BAND DIGITAL CONTROLLED AUDIO PROCESSOR

- ONE STEREO INPUT
- ONE STEREO OUTPUT
- TWO INDEPENDENT VOLUME CONTROL IN 1.0dB STEPS
- TREBLE, MIDDLE AND BASS CONTROL IN 1.0dB STEPS
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2 CBUS



DIP20



SO20

ORDERING NUMBERS: TDA7319 (DIP20)
TDA7319D (SO20)

DESCRIPTION

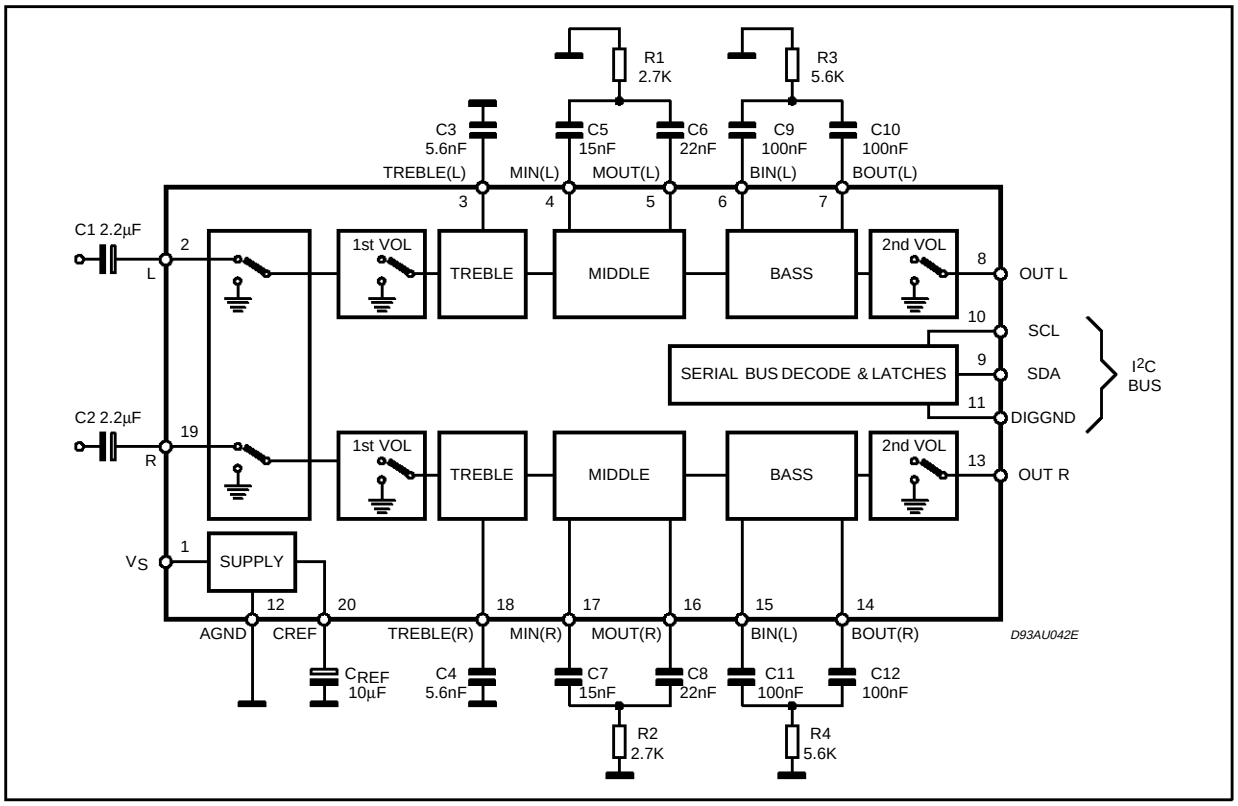
The TDA7319 is a volume and tone (bass , middle and treble) processor for quality audio application in car radio and Hi-Fi system.

Control is accomplished by serial I^2C bus microprocessor interface.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/MOS Technology, Low Distortion, Low Noise and Low Dc stepping are obtained.

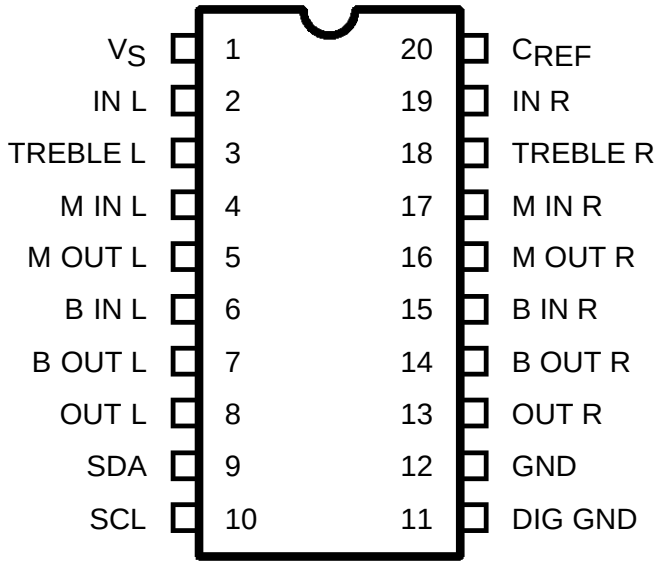
BLOCK DIAGRAM AND APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



D93AU041A

THERMAL DATA

Symbol	Parameter	DIP20	SO20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins	150	150	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10.5	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		100		dB
	1st and 2nd Volume Control 1dB step	-47		0	dB
	Bass, Middle and Treble Control 1dB step	-14		+14	dB
	Mute Attenuation		100		dB

ELECTRICAL CHARACTERISTICS (V_S = 9V; R_L = 10KΩ; f = 1KHz; all control = flat (G = 0); T_{amb} = 25°C Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT						
R_{in}	Input Resistance		35	50	65	KΩ
1st VOLUME CONTROL						
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Maximum Attenuation		45	47	49	dB
A_{step}	Step Resolution		0.5	1.0	1.5	dB
E_A	Attenuation Set Error	G = 0 to -24dB	-1.0		1.0	dB
		G = -24 to -47dB	-1.5		1.5	dB
E_t	Tracking Error	G = 0 to -24dB			1	dB
		G = 24 to -47dB			2	dB
A_{mute}	Mute Attenuation		80	100		dB
V_{DC}	DC Steps	Adiacent Attenuation Steps		0	3	mV
		From 0dB to A_{VMAX}		0.5	5	mV
2nd VOLUME CONTROL						
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Maximum Attenuation		45	47	49	dB
A_{step}	Step Resolution		0.5	1.0	1.5	dB
E_A	Attenuation Set Error	G = 0 to -24dB	-1.0		1.0	dB
		G = -24 to -47dB	-1.5		1.5	dB
E_t	Tracking Error	G = 0 to -24dB			1	dB
		G = 24 to -47dB			2	dB
A_{MUTE}	Mute Attenuation		80	100		dB
V_{DC}	DC Steps	Adiacent Attenuation Steps		0	3	mV
		From 0dB to A_{VMAX}		0.5	5	mV
BASS						
R_b	Internal Feedback Resistance		32	44	56	KΩ
C_{RANGE}	Control Range		±11.5	±14	±16	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
MIDDLE						
R_b	Internal Feedback Resistance		18	25	32	KΩ
C_{RANGE}	Control Range		±11.5	±14	±16	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
TREBLE						
C_{RANGE}	Control Range		±13	±14	±15	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
SUPPLY						
V_S	Supply Voltage (note1)		6	9	10.5	V
I_S	Supply Current		4	7	10	mA
SVR	Ripple Rejection		60	90		dB
AUDIO OUTPUT						
V_{clip}	Clipping Level	d = 0.3%	2	2.6		Vrms
R_{Ol}	Output Load Resistance		2			KΩ
R_O	Output Impedance		100	180	300	Ω
V_{DC}	DC Voltage Level			3.8		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL						
e_{NO}	Output Noise	All Gains 0dB (B = 20 to 20kHz flat)		5	15	µV
E_t	Total Tracking Error	A_V = 0 to -24dB		0	1	dB
		A_V = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All Gains = 0dB; V_O = $1V_{rms}$		106		dB
S_C	Channel Separation		80	100		dB
d	Distortion	A_V = 0; V_{in} = $1V_{rms}$		0.01	0.08	%
BUS INPUTS						
V_{il}	Input Low Voltage				1	V
V_{ih}	Input High Voltage		3			V
I_{in}	Input Current	V_{in} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

Note 1: the device is functionally good at Vs = 5V. A step down, on V_S, to 4V does't reset the device.

APPLICATION SUGGESTIONS

The first and the last stages are volume control blocks. The control range is 0 to -47dB (mute) with a 1dB step.
The very high resolution allows the implementation of systems free from any noisy acoustical effect.
The TDA7319 audioprocessor provides 3 bands tones control.

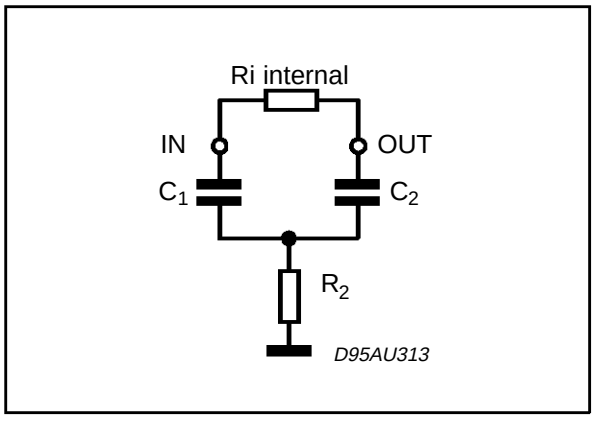
Bass, Middle Stages

The Bass and the middle cells have the same structure.

The Bass cell has an internal resistor Ri = 44KΩ typical.
The Middle cell has an internal resistor Ri = 25KΩ typical.

Several filter types can be implemented, connecting external components to the Bass/Middle IN and OUT pins.

Figure 1.



The fig.1 refers to basic T Type Bandpass Filter starting from the filter component values (R1 internal and R2,C1,C2 external) the centre frequency Fc, the gain Av at max. boost and the filter Q factor are computed as follows:

$$F_C = \frac{1}{2 \cdot \pi \cdot \sqrt{Ri, R2, C1, C2}}$$

$$A_V = \frac{R2\ C2 + R2\ C1 + Ri\ C1}{R2\ C1 + R2\ C2}$$

$$Q = \frac{\sqrt{Ri\ R2 + C1\ C2}}{R2\ C1 + R2\ C2}$$

Viceversa, once Fc, Av, and Ri internal value are fixed, the external components values will be:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot R_i \cdot Q} \qquad C2 = \frac{Q^2 \cdot C1}{A_V - 1\ Q^2}$$

$$R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot F_C \cdot (A_V - 1) \cdot Q}$$

Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25KΩ typical) and an external capacitor connected between treble pins and ground

Typical responses are reported in Figg. 10 to 13.

CREF

The suggested 10µF reference capacitor (CREF) value can be reduced to 4.7µF if the application requires faster power ON.

Figure 2: Noise vs. volume setting

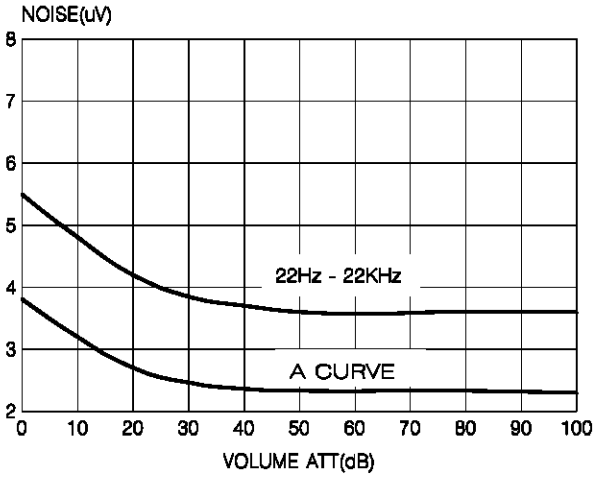


Figure 3: SVRR vs. frequency

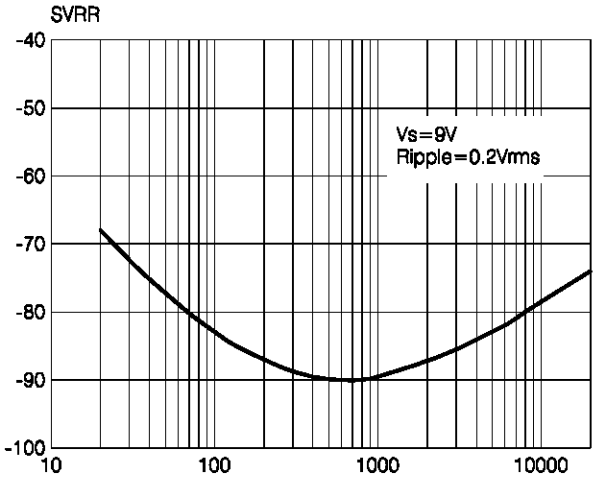


Figure 4: THD vs. frequency

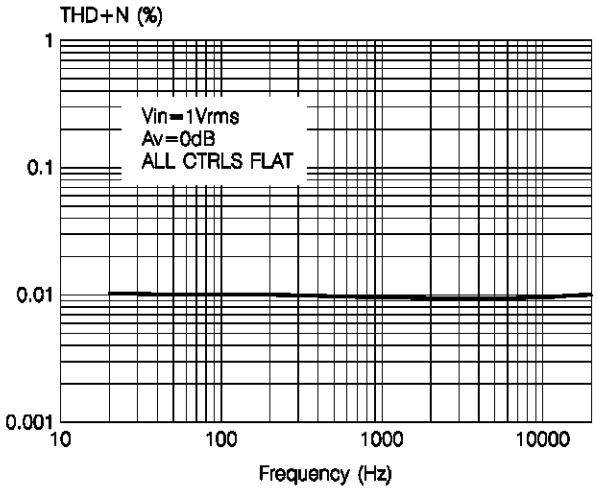


Figure 5: THD vs. R_{LOAD}

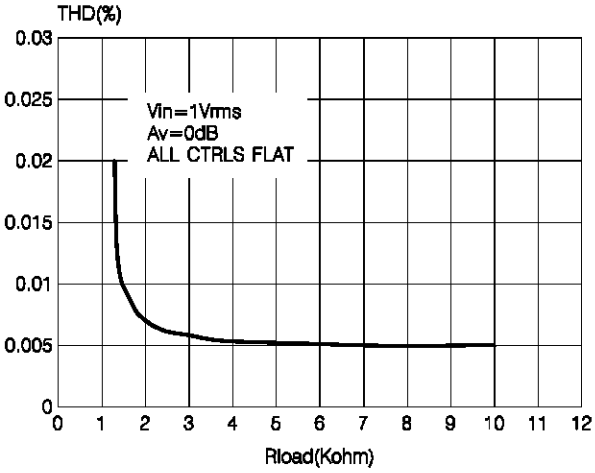


Figure 6: Channel separation vs. frequency

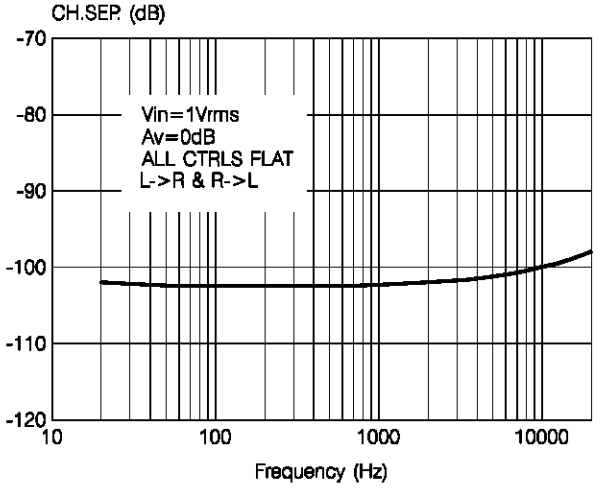


Figure 7: Output clip level vs. Supply voltage

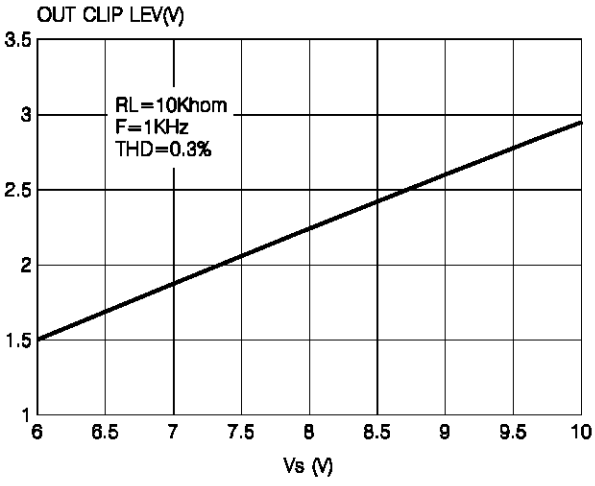


Figure 8: Quiescent current vs. supply voltage

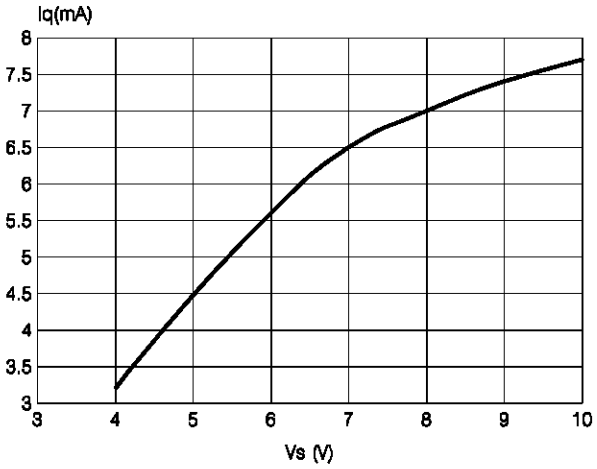


Figure 9: Quiescent current vs. temperature

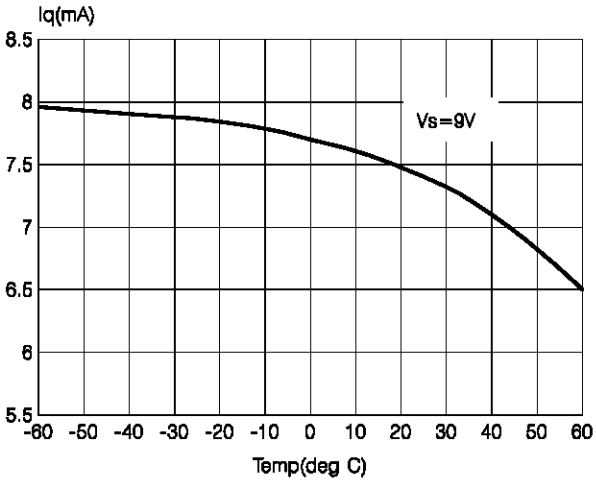


Figure 10: Bass response

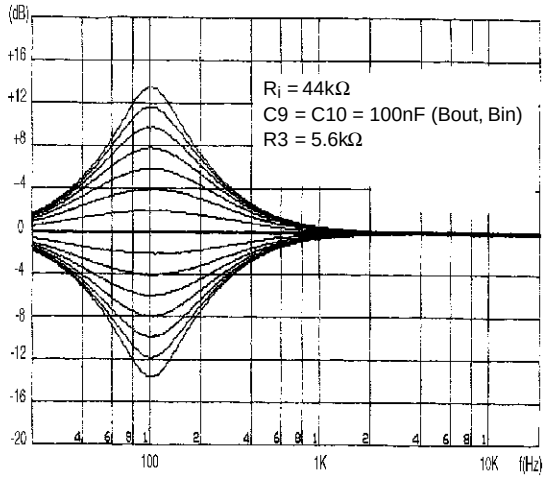


Figure 11: Middle response

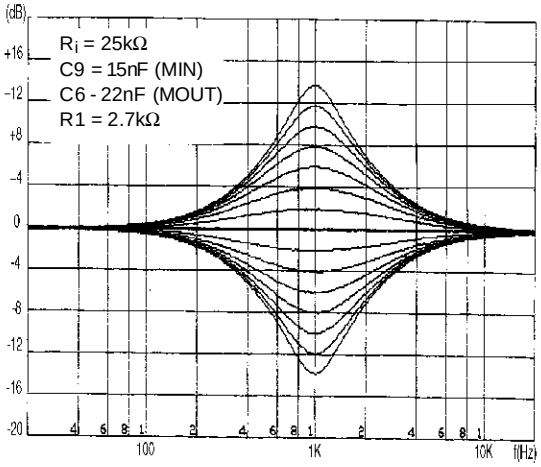


Figure 12: Treble response

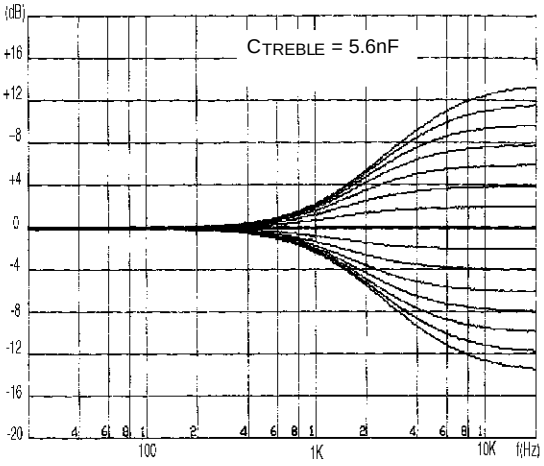
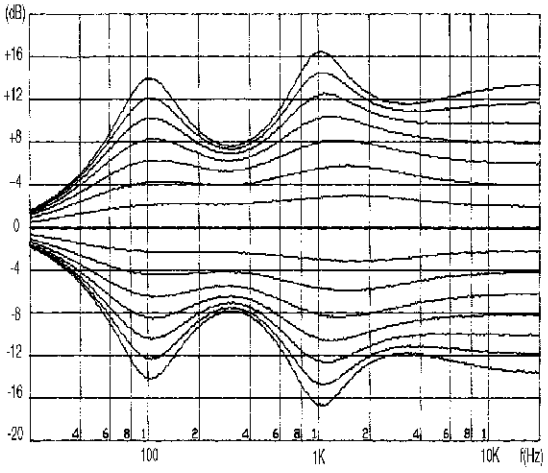


Figure 13: Typical tone response



I^2C BUS INTERFACE

Data transmission from microprocessor to the TDA7319 and viceversa takes place thru the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

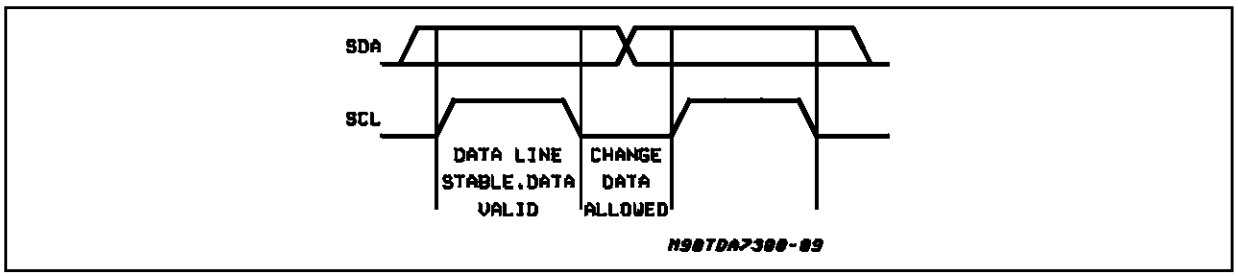
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

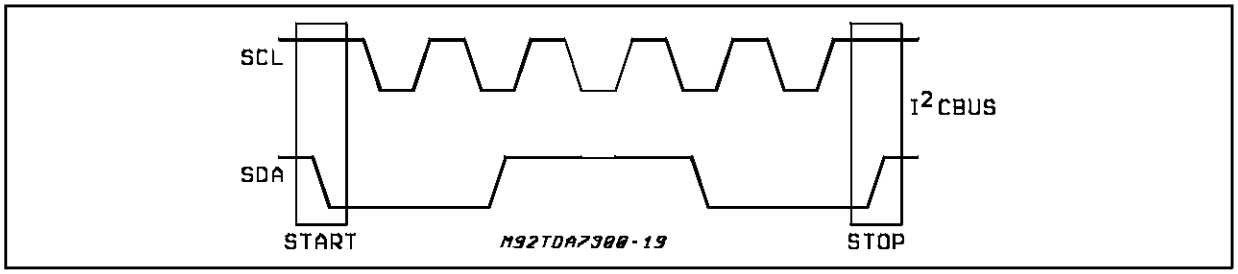
Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it generates the 9th clock pulse without checking the slave acknowledging, and then sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

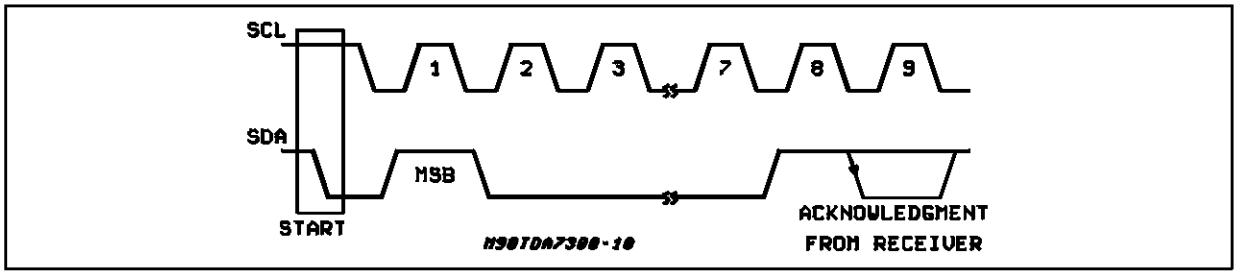
Data Validity on the I^2CBUS



Timing Diagram of I^2CBUS



Acknowledge on the I^2CBUS

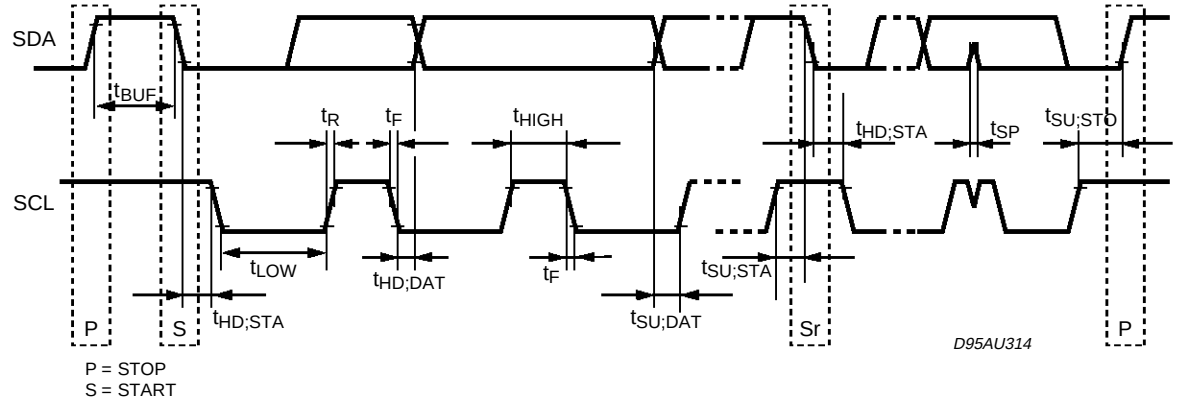


SDA, SCL I²CBUS TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	0		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU:STA}$	Set-up time for a repeated START condition	0.6			µs
$t_{HD:DA}$	Data hold time	0.300			µs
$t_{SU:DAT}$	Data set-up time	100			ns
t_R	Rise time of both SDA and SCL signals	20		300	ns (*)
t_F	Fall time of both SDA and SCL signals	20		300	ns (*)
$t_{SU:STO}$	Set-up time for STOP condition	0.6			µs

All values referred to $V_{IH\ min.}$ and $V_{IL\ max.}$ levels
(*) Must be guaranteed by the I²C BUS master.

Definition of timing on the I²C-bus

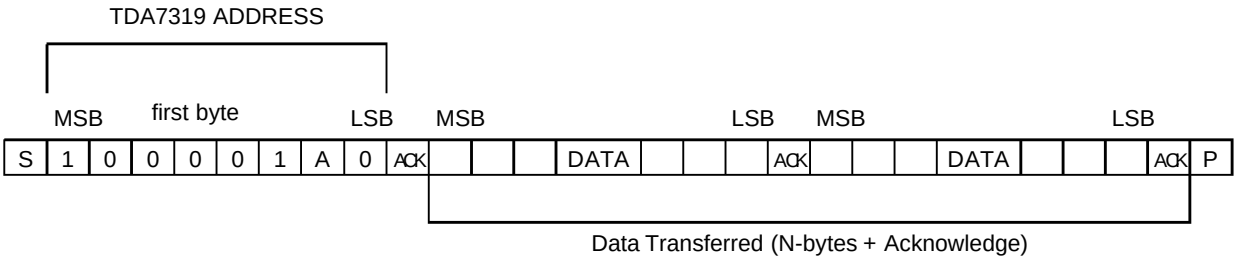


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7319 address (the 8th bit of the byte must be 0). The TDA7319 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 400kbits/s

SOFTWARE SPECIFICATION

Chip address

1 MSB	0	0	0	0	1	1	0 LSB

FUNCTION CODES

	MSB	F6	F5	F4	F3	F2	F1	LSB
1st VOLUME	0	F6	F5	F4	F3	F2	F1	0
2nd VOLUME	0	F6	F5	F4	F3	F2	F1	1
TREBLE	1	0	0	F4	F3	F2	F1	F0
MIDDLE	1	0	1	F4	F3	F2	F1	F0
BASS	1	1	0	F4	F3	F2	F1	F0
MUTMUX	1	1	1	F4	F3	F2	F1	F0

POWER ON RESET:
1st volume = 2nd volume = Mute
Treble = Middle = Bass = -14dB
Mutmux = Active Input

1st VOLUME CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
0							0	step 1dB
				0	0	0		0dB
				0	0	1		-1dB
				0	1	0		-2dB
				0	1	1		-3dB
				1	0	0		-4dB
				1	0	1		-5dB
				1	1	0		-6dB
				1	1	1		-7dB
0							0	step 8dB
	0	0	0					0dB
	0	0	1					-8dB
	0	1	0					-16dB
	0	1	1					-24dB
	1	0	0					-32dB
	1	0	1					-40dB
	1	1	1					MUTE

2nd VOLUME CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
0							1	step 1dB
				0	0	0		0dB
				0	0	1		-1dB
				0	1	0		-2dB
				0	1	1		-3dB
				1	0	0		-4dB
				1	0	1		-5dB
				1	1	0		-6dB
				1	1	1		-7dB
0							1	step 8dB
	0	0	0					0dB
	0	0	1					-8dB
	0	1	0					-16dB
	0	1	1					-24dB
	1	0	0					-32dB
	1	0	1					-40dB
	1	1	1					MUTE

TREBLE CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	0						TREBLE BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	0	0						TREBLE CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

MIDDLE CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	1						MIDDLE BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	0	1						MIDDLE CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

BASS CODES

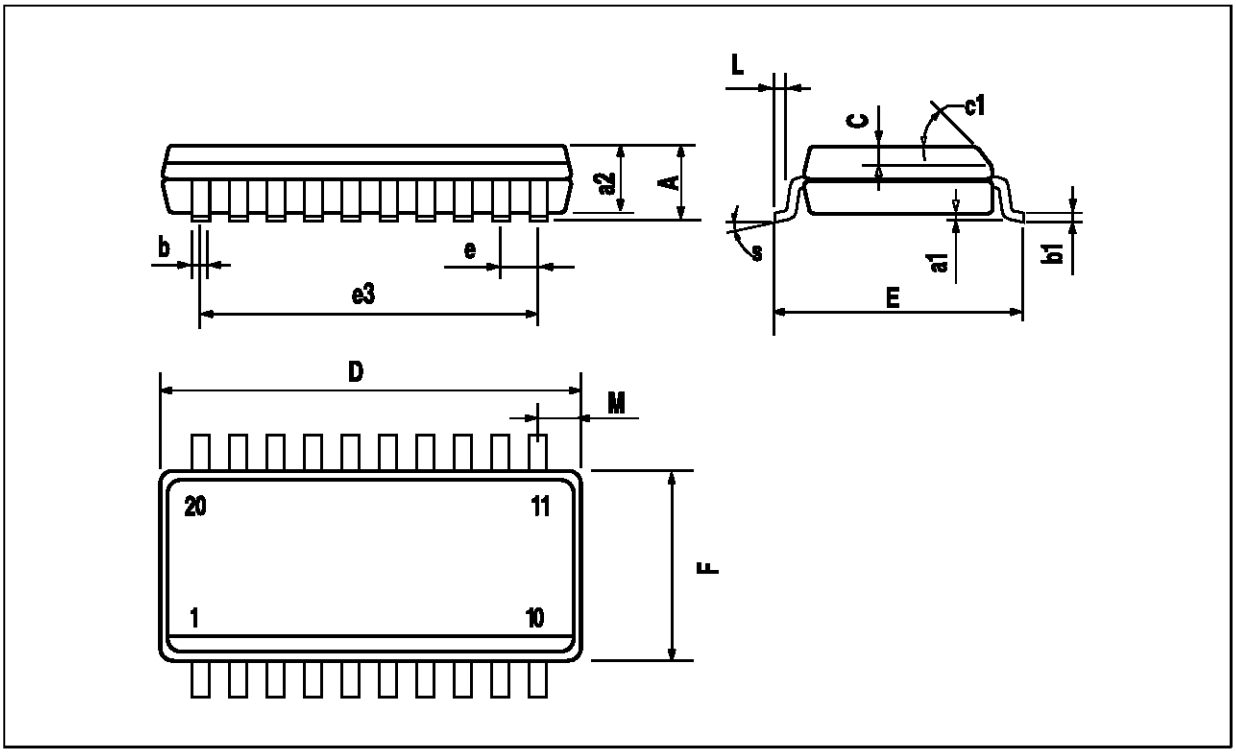
MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	1	0						BASS BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	1	0						BASS CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

MUTMUX CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	1	1						INPUTS
			X	X	X	0	0	NOT ALLOWED
			X	X	X	0	1	NOT ALLOWED
			X	X	X	1	0	NOT ALLOWED
			X	1	1	1	1	IN

SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053