TDA7430
TDA7431

DIGITALLY CONTROLLED AUDIO PROCESSOR WITH SURROUND SOUND MATRIX AND VOICE CANCELLER

1 FEATURES

- 1 STEREO (4STEREO) INPUT + 1 MIXER INPUT
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- VOICE CANCELLER IS AVAILABLE
- TREBLE MIDDLE AND BASS CONTROL
- THREE SURROUND MODES ARE AVAILABLE
  - MUSIC: 4 SELECTABLE RESPONSES
  - MOVIE AND SIMULATED: 256 SELECTABLE RESPONSES
- 2 SPEAKERS AND 2 RECORD ATTENUATORS:
  - 2 INDEPENDENT SPEAKERS AND 2 INDEPENDENT RECORD CONTROL IN 1dB STEP FOR BALANCE FACILITY
  - AVAILABILITY OF LOUDSPEAKER EQUALIZATION FIXED BY EXTERNAL COMPONENTS
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS

Figure 1. Package

SDIP42 TQFP44

Table 1. Order Codes

Part Number	Package
TDA7431S	SDIP42
TDA7430	TQFP44
TDA7430TR	Tape & Reel

2 DESCRIPTION

The TDA7430/TDA7431 is volume tone (bass middle and treble) balance (Left/Right) processors voice canceller for quality audio applications in car radio and Hi-Fi systems.

They reproduce surround sound by using programmable phase shifters and a signal matrix.

Control of all the functions is accomplished by serial bus. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers. Thanks to the used BIPOLAR/CMOS Technology,

Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Pin Connection (TDA7430)

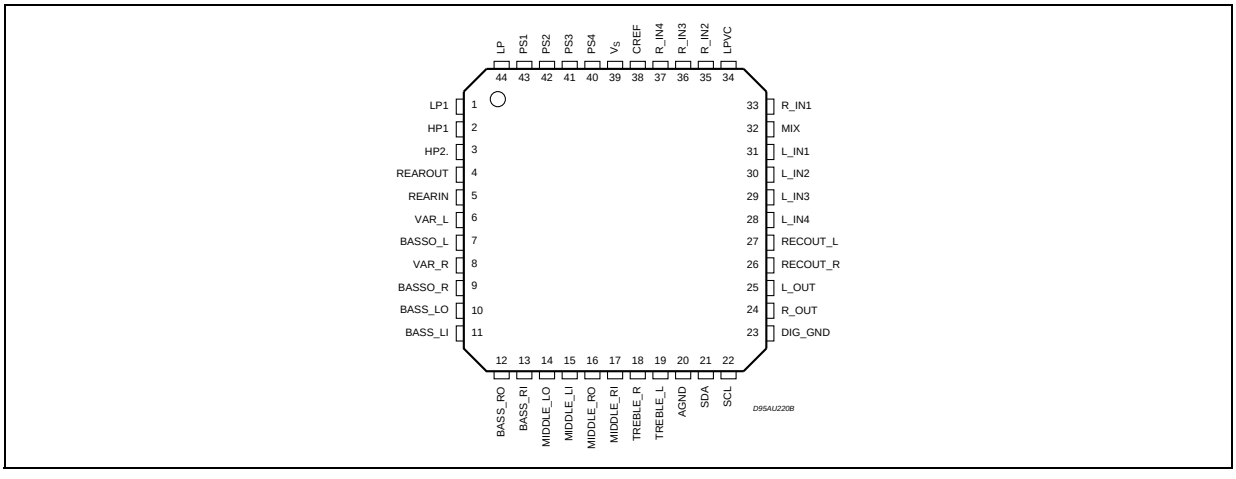


Figure 3. Pin Connection (TDA7431)

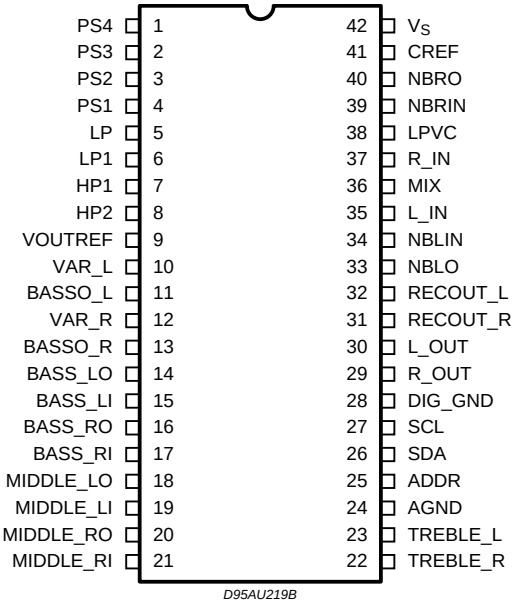


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	11	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Table 3. Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	7	9	10.2	V
V_{CL}	Max Input Signal Handling	2			V_{RMS}
THD	Total Harmonic Distortion V = 0.1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V_{out} = 1Vrms (mode = OFF)		106		dB
S_C	Channel Separation f = 1KHz		90		dB
	Treble Control (2dB step)	-14		14	dB
	Middle Control (2dB step)	-14		14	dB
	Bass Control (2dB step)	-14		14	dB
	Balance Control 1dB step (LCH, RCH)	-79		0	dB
	Mute Attenuation		100		dB

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	85	°C/W

Figure 4. TEST CIRCUIT (TDA7430)

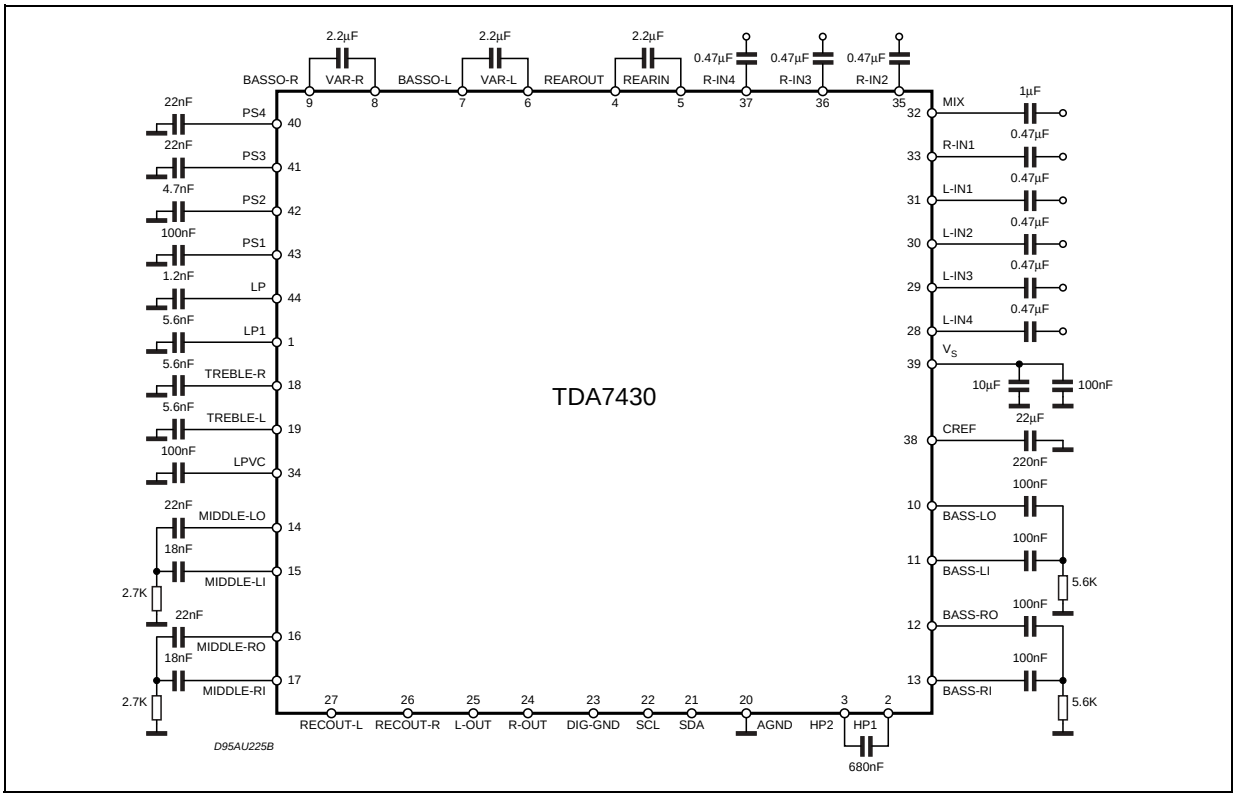


Figure 5. TEST CIRCUIT (TDA7431)

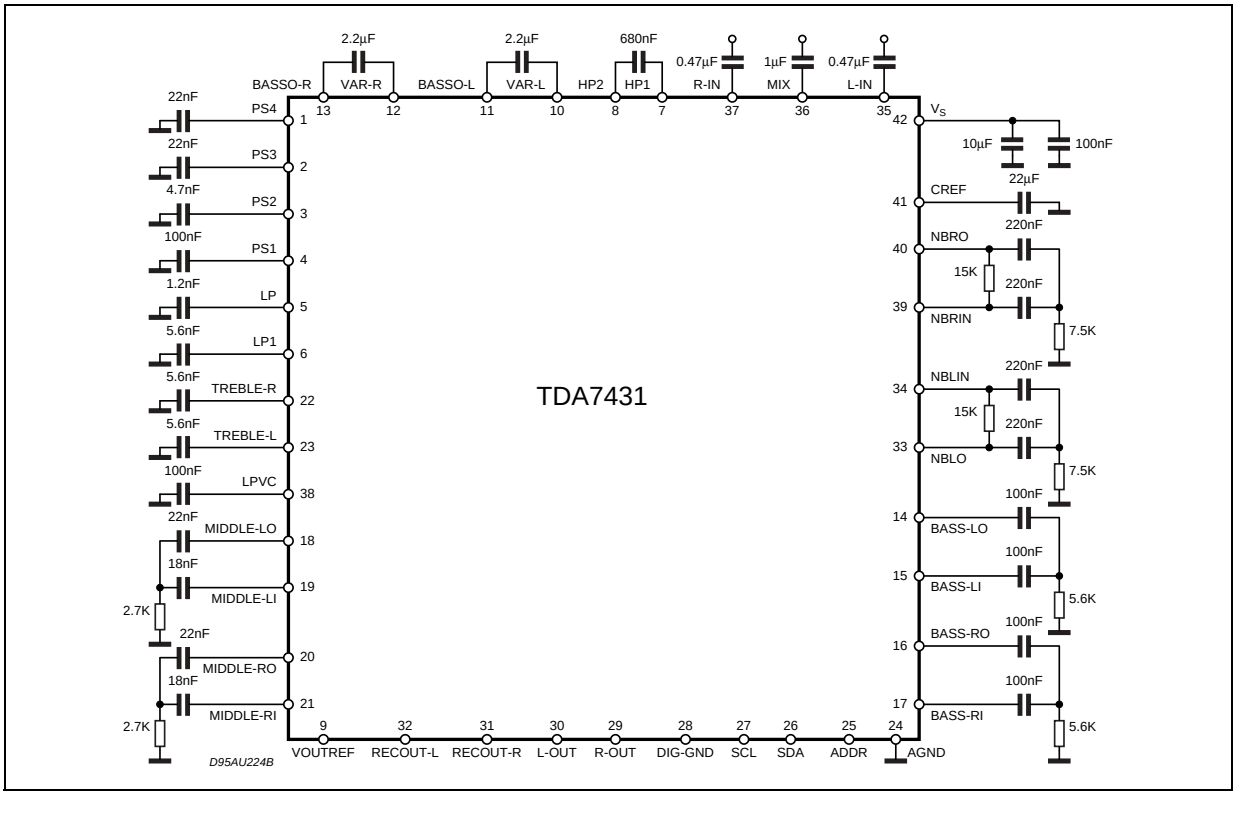


Figure 6. Block Diagram (TDA7430)

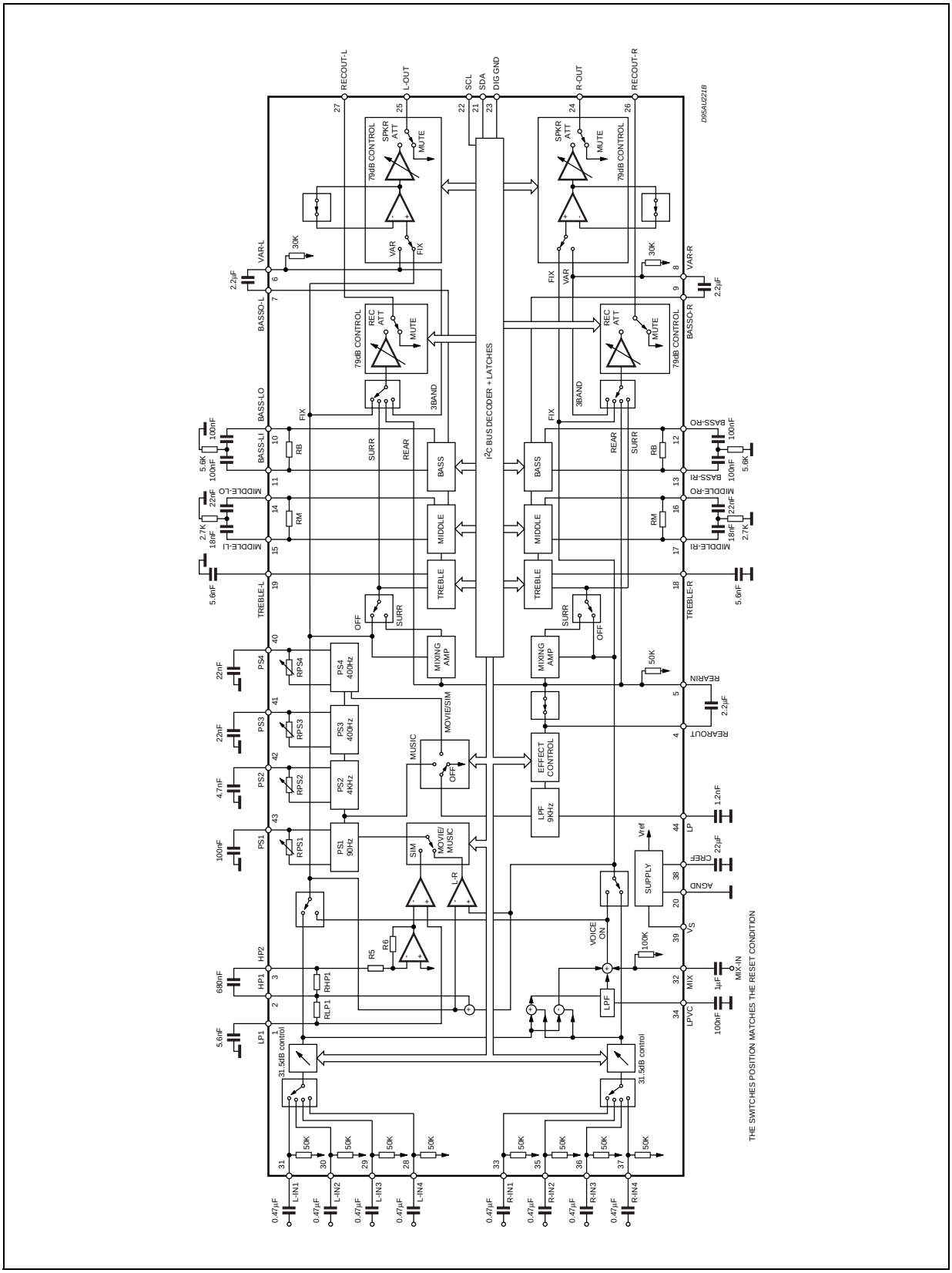


Figure 7. Block Diagram (TDA7431)

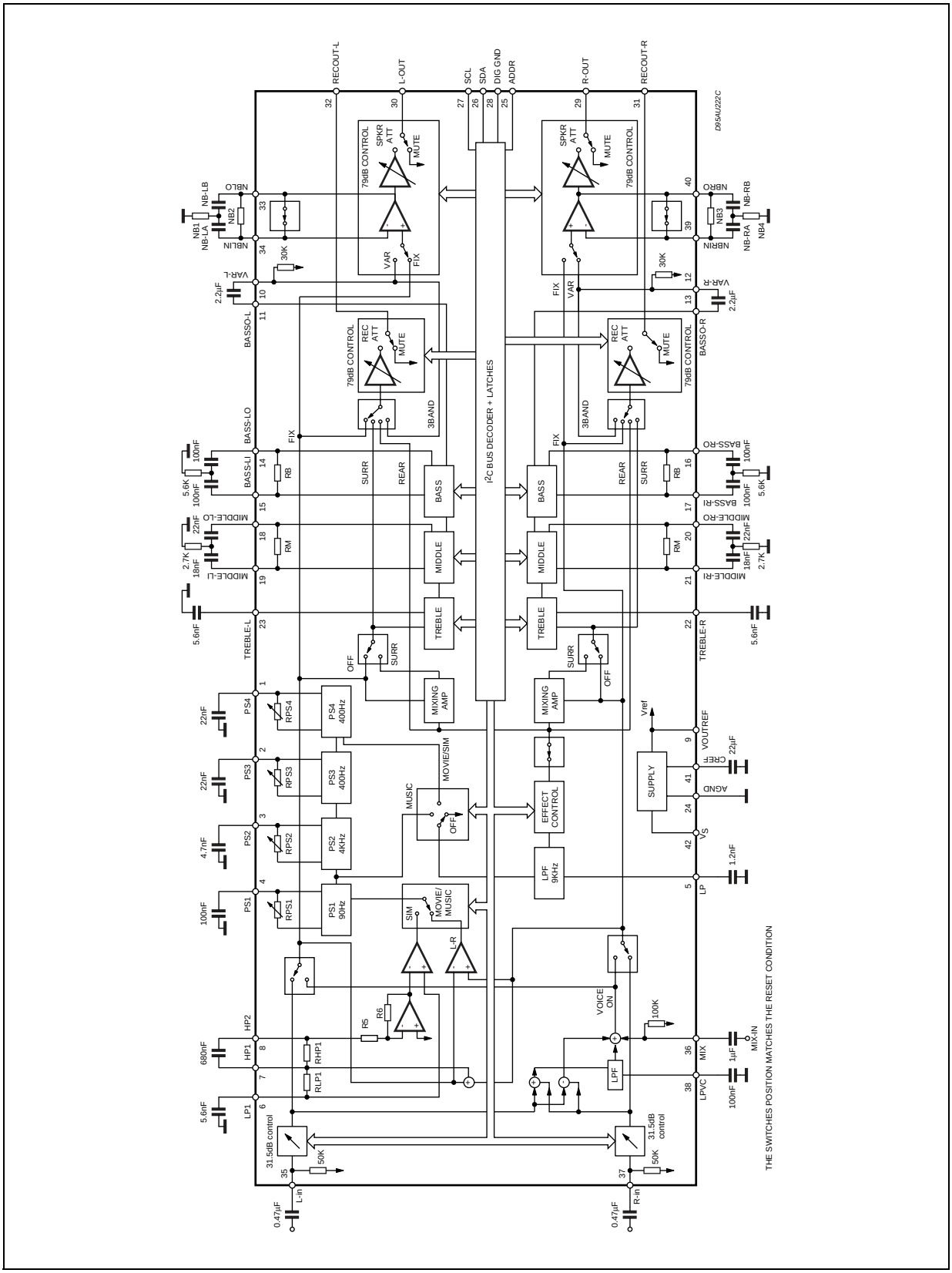


Table 5. Electrical Characteristcs (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, V_{in} = 1Vrms; R_G = 600Ω, all controls flat (G = 0dB), Effect CTRL = -6dB, MODE = OFF; f = 1KHz unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		7	9	10.2	V
I_S	Supply Current		10	18	26	mA
SVR	Ripple Rejection	L_{CH} / $R_{CH\ out}$, Mode = OFF	60	80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V_{rms}
C_{RANGE}	Control Range			31.5		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		31	31.5	32	dB
A_{STEP}	Step Resolution			0.5	1	dB
V_{DC}	DC Steps	adjacent att. step	-3	0	3	mV
A_{VO1}	Voice Canceler Output 1	L_{IN} = R_{IN}, R_{IN} = ON, Vmix = 0V FIX, 0dB attenuation	5	6	7	dB
A_{VO2}	Voice Canceler Output 2	L_{IN} = R_{IN} = 0V, Vmix = 1V_{rms} FIX, 0dB attenuation	-1	0	1	dB
A_{VO3}	Voice Canceler Output 3	L_{IN} = R_{IN}, Vmix = 0V FIX, 0dB attenuation	5	6	7	dB
R_{LPV}	Low Pass Filter Resistance		22.4	32	41.6	KΩ
R_{MIX}	Input Impedance		70	100	130	KΩ
BASS CONTROL						
G_b	Control Range	Max. Boost/cut	±11.5	±14.0	±16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		32	44	56	KΩ
MIDDLE CONTROL						
G_m	Control Range	Max. Boost/cut	±11.5	±14.0	±16.0	dB
M_{STEP}	Step Resolution		1	2	3	dB
R_M	Internal Feedback Resistance		17.5	25	32.5	KΩ
TREBLE CONTROL						
G_t	Control Range	Max. Boost/cut	±13.0	±14.0	±15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB

Table 5. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
EFFECT CONTROL						
C_{RANGE}	Control Range		±13.0		6	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
SURROUND SOUND MATRIX TEST CONDITION (Phase Resistor Selection D0=0, D1=1, D2=0. D3=1, D4=0, D5=1, D6=0, D7=1						
G_{OFF}	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p}, $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$	-1	0	1	dB
D_{GOFF}	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p}, $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$	-1	0	1	dB
G_{MOV}	In-phase Gain (Movie)	Movie mode, Effect Ctrl = -6dB 1kHz, 1.4 V_{p-p}, $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$		8		dB
D_{GMOV}	LR In-phase Gain Difference (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $(R_{in} \rightarrow R_{out})$ - $(L_{in} \rightarrow L_{out})$		0		dB
G_{MUS}	In-phase Gain (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $(R_{in} \rightarrow R_{out})$, $(L_{in} \rightarrow L_{out})$		7		dB
D_{GMUS}	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $(R_{in} \rightarrow R_{out})$, $(L_{in} \rightarrow L_{out})$		0		dB
L_{MON1}	Simulated L Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		4.5		dB
L_{MON2}	Simulated L Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		–4.0		dB
L_{MON3}	Simulated L Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		7.0		dB
R_{MON1}	Simulated R Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		– 4.5		dB
R_{MON2}	Simulated R Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		3.8		dB
R_{MON3}	Simulated R Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		– 20		dB
R_{LP1}	Low Pass Filter Resistance		7	10	13	KΩ
R_{HPI}	High Pass Filter Resistance		42	60	78	KΩ
R_{LPF}	LP Pin Impedance		7	10	13	KΩ

Table 5. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SURROUBND SOUBND MATRIX PHASE						
R_{PS10}	Phase Shifter 1: D1 = 0, D0 = 0		8.3	11.8	15.2	KΩ
R_{PS11}	Phase Shifter 1: D1 = 0, D0 = 1		10	14.1	18.3	KΩ
R_{PS12}	Phase Shifter 1: D1 = 1, D0 = 0		12.6	17.9	23.3	KΩ
R_{PS13}	Phase Shifter 1: D1 = 1, D0 = 1		26.4	37.3	48.85	KΩ
R_{PS20}	Phase Shifter 2: D3 = 0, D2 = 0		4	5.6	7.2	KΩ
R_{PS21}	Phase Shifter 2: D3 = 0, D2 = 1		4.8	6.8	8.7	KΩ
R_{PS22}	Phase Shifter 2: D3 = 1, D2 = 0		6	8.4	10.9	KΩ
R_{PS23}	Phase Shifter 2: D3 = 1, D2 = 1		12.9	18.3	23.7	KΩ
R_{PS30}	Phase Shifter 3: D5 = 0, D4 = 0		8.5	12.1	15.6	KΩ
R_{PS31}	Phase Shifter 3: D5 = 0, D4 = 1		10.2	14.5	18.7	KΩ
R_{PS32}	Phase Shifter 3: D5 = 1, D4 = 0		12.7	18.1	23.3	KΩ
R_{PS33}	Phase Shifter 3: D5 = 1, D4 = 1		27.4	39.1	50.75	KΩ
R_{PS40}	Phase Shifter 4: D7 = 0, D6 = 0		8.5	12.1	15.6	KΩ
R_{PS41}	Phase Shifter 4: D7 = 0, D6 = 1		10.2	14.5	18.7	KΩ
R_{PS42}	Phase Shifter 4: D7 = 1, D6 = 0		12.7	18.1	23.3	KΩ
R_{PS43}	Phase Shifter 4: D7 = 1, D6 = 1		27.4	39.1	50.75	KΩ
SPEAKER & RECORD ATTENUATORS						
C_{RANGE}	Control Range			79		dB
S_{STEP}	Step Resolution		-0.5	1	1.5	dB
E_A	Attenuation set error	A_v = 0 to -20dB	-1.5	0	1.5	dB
		A_v = -20 to -79dB	-3	0	2	dB
V_{DC}	DC Steps	adjacent att. steps	-3	0	3	mV
A_{MUTE}	Output Mute Condition		+70	100		dB
R_{VEA}	Input Impedance		21	30	39	KΩ
AUDIO OUTPUTS						
$N_{O(OFF)}$	Output Noise (OFF)	Output Mute, Flat BW = 20Hz to 20KHz		4 5		μV_{rms} μV_{rms}
$N_{O(MOV)}$	Output Noise (Movie)	Mode = Movie BW = 20Hz to 20KHz		30		μV_{rms}
$N_{O(Mus)}$	Output Noise (Music)	Mode = Music BW = 20Hz to 20KHz		30		μV_{rms}
$N_{O(MON)}$	Output Noise (Simulated)	Mode Simulated BW = 20Hz to 20KHz		30		μV_{rms}

Table 5. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
d	Distorsion	A_V = 0 ; V_{in} = 1V_{rms}		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		10	40	70	Ω
V_{OUT}	DC Voltage Level			3.8		V
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	mA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

3 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7430/TDA7431 and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data Validity

As shown in fig. 8, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and Stop Conditions

As shown in fig.9 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

3.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 10). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 8. Data validity on the I²C bus

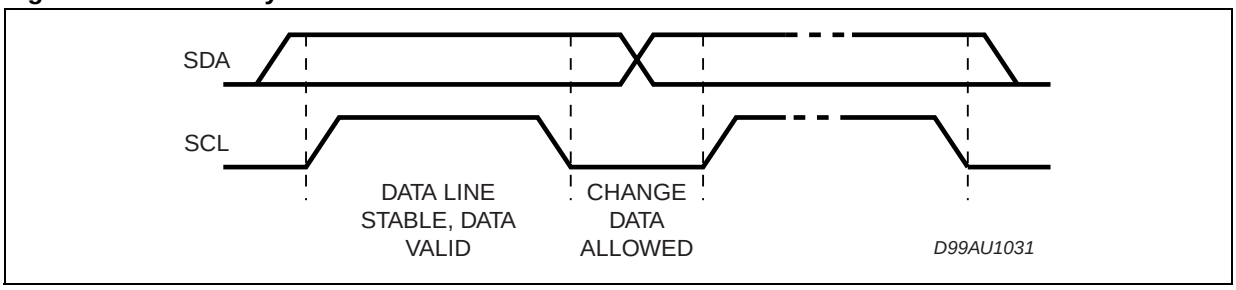


Figure 9. Timing Diagram of I²C bus

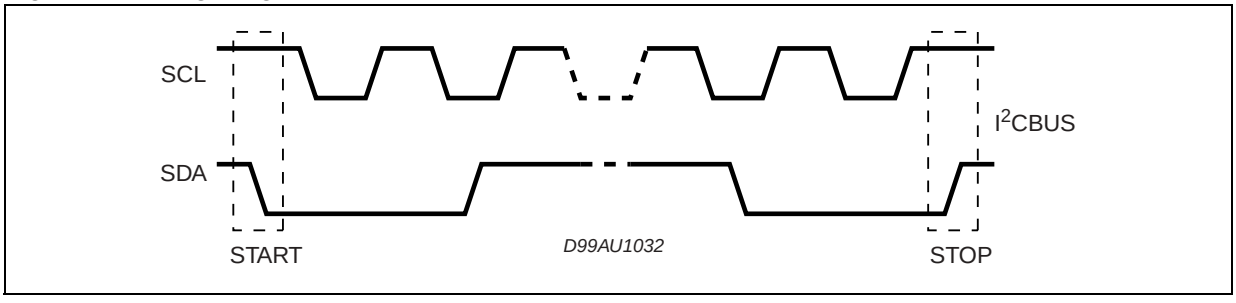
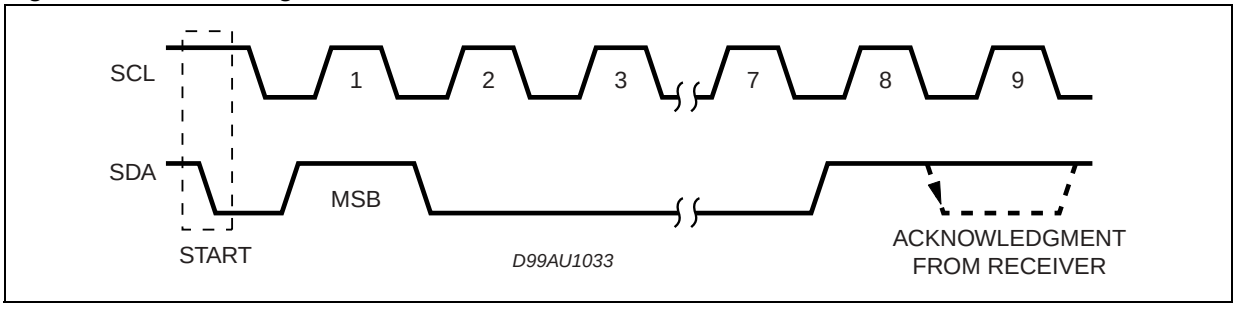


Figure 10. Acknowledge on the I²C bus



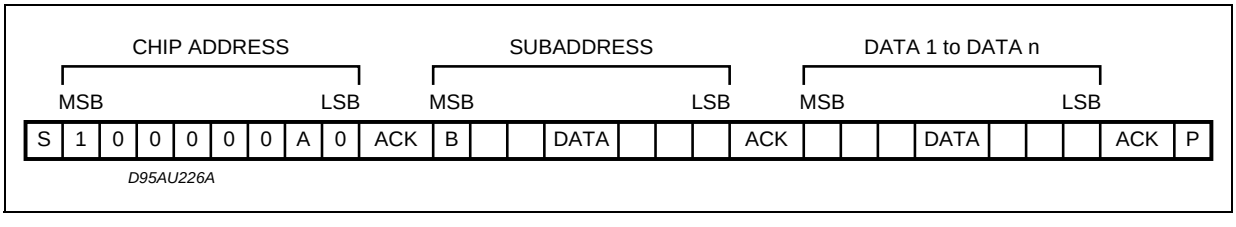
4 SOFTWARE SPECIFICATION

4.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7430/TDA7431 address
- A subaddress bytes
- A sequence of data (N byte + achnowledge)
- A stop condition (P)

Figure 11.

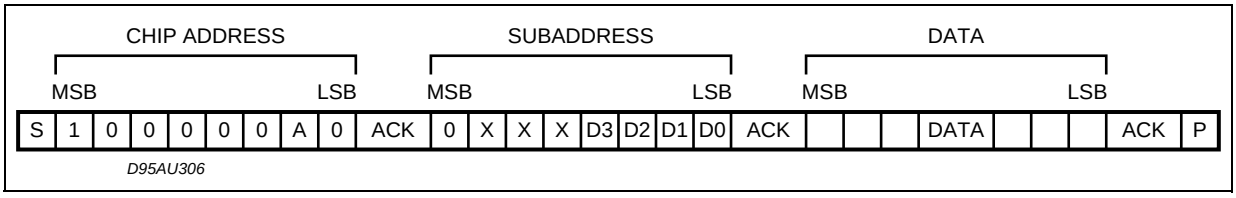


5 EXAMPLES

5.1 No Incremental Bus

The TDA7430/TDA7431 receives a start condition, the correct chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.

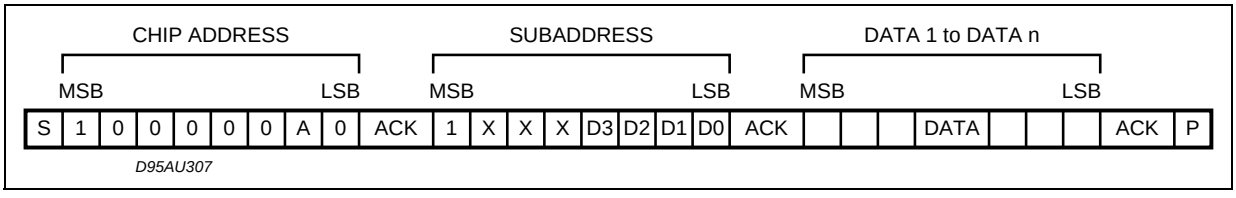
Figure 12.



5.2 Incremental Bus

The TDA7430/TDA7431 receives a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored.The DATA 1 concern thesubaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.

Figure 13.



6 DATA BYTES

Address = 80(HEX) ADDR open; 82 (HEX): need to connect supply

6.1 Function Selection

Table 6. The first byte (Subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
B	X	X	X	0	0	0	0	INPUT ATTENUATION
B	X	X	X	0	0	0	1	SURROUND & OUT & EFFECT CONTROL
B	X	X	X	0	0	1	0	PHASE RESISTOR
B	X	X	X	0	0	1	1	BASS & NATURAL BASE
B	X	X	X	0	1	0	0	MIDDLE & TREBLE
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L"
B	X	X	X	0	1	1	0	SPEAKER ATTENUATION "R"
B	X	X	X	0	1	1	1	AUX ATTENUATION "L"
B	X	X	X	1	0	0	0	AUX ATTENUATION"R"
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER, & AUX OUT

B = 1 incremental bus; active
B = 0 no incremental bus;
X = indifferent 0,1

Table 7. INPUT ATTENUATION SELECTION

MSB							LSB	INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	0.5 dB STEPS
X					0	0	0	0
X					0	0	1	-0.5
X					0	1	0	-1
X					0	1	1	-1.5
X					1	0	0	-2
X					1	0	1	-2.5
X					1	1	0	-3
X					1	1	1	-3.5
								4 dB STEPS
X		0	0	0				0
X		0	0	1				-4
X		0	1	0				-8
X		0	1	1				-12
X		1	0	0				-16
X		1	0	1				-20
X		1	1	0				-24
X		1	1	1				-28

INPUT ATTENUATION = 0 ~ -31.5dB

Table 8.

D7	D6	D5	D4	D3	D2	D1	D0	REAR SWITCH
X	0							REARIN, REAROUT PIN ACTIVE
X	1							NO REARIN, REAROUT PIN

Table 9. SURROUND SELECTION

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**SURROUND MODE**
						0	0	SIMULATED
						0	1	MUSIC
						1	0	OFF
						1	1	MOVIE
								OUT
					0			VAR
					1			FIX
								EFFECT CONTROL
	0	0	0	0				-6
	0	0	0	1				-7
	0	0	1	0				-8
	0	0	1	1				-9
	0	1	0	0				-10
	0	1	0	1				-11
	0	1	1	0				-12
	0	1	1	1				-13
	1	0	0	0				-14
	1	0	0	1				-15
	1	0	1	0				-16
	1	0	1	1				-17
	1	1	0	0				-18
	1	1	0	1				-19
	1	1	1	0				-20
	1	1	1	1				-21

Table 10. PHASE RESISTOR SELECTION

MSB							LSB	SURROUND PHASE RESISTOR
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**PHASE SHIFT 1 (KΩ)**
						0	0	12
						0	1	14
						1	0	18
						1	1	37
								PHASE SHIFT 2 (KΩ)
				0	0			6
				0	1			7
				1	0			8
				1	1			18
								PHASE SHIFT 3 (KΩ)
		0	0					12
		0	1					14
		1	0					18
		1	1					39
								PHASE SHIFT 4 (KΩ)
0	0							12
0	1							14
1	0							18
1	1							39

Table 11. BASS SELECTION

MSB							LSB	BASS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**2 dB STEPS**
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								NATURAL BASE
			0					NBRIN, NBRO, NBLIN, NBLO PIN ACTIVE
			1					NO NBRIN, NBRO, NBLIN, NBLO PIN

Table 12. SPEAKER/AUX ATT. R & L SELECTION

MSB							LSB	SPEAKER/AUX ATT
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**1 dB STEPS**
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								8 dB STEPS
	0	0	0	0				0
	0	0	0	1				-8
	0	0	1	0				-16
	0	0	1	1				-24
	0	1	0	0				-32
	0	1	0	1				-40
	0	1	1	0				-48
	0	1	1	1				-56
	1	0	0	0				-64
	1	0	0	1				-72
								MUTE
	1	0	1	X				
	1	1	X	X				

X = INDIFFERENT 0,1
SPEAKER/AUX ATTENUATION = 0dB ~ -79dB

Table 13. MIDDLE & TREBLE SELECTION

MSB							LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								TREBLE
								2 dB STEPS
0	0	0	0					-14
0	0	0	1					-12
0	0	1	0					-10
0	0	1	1					-8
0	1	0	0					-6
0	1	0	1					-4
0	1	1	0					-2
0	1	1	1					0
1	1	1	1					0
1	1	1	0					2
1	1	0	1					4
1	1	0	0					6
1	0	1	1					8
1	0	1	0					10
1	0	0	1					12
1	0	0	0					14

Table 14. VOICE CANCELLER/INPUT/RECOUT L & R SELECTION

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**VOICE CANCELER**
					0	1	0	OFF
					0	0	1	ON
								INPUT MULTIPLEXER
					0	0		IN2
					0	1		IN3
					1	0		IN4
					1	1		IN1
								REC OUT "L"
			0	0				VER 1 (3BAND)
			0	1				VER 2 (SURR)
			1	0				VER 3 (REAR)
			1	1				FIX
								REC OUT "R"
	0	0					0	VER 1 (3BAND)
	0	1					0	VER 2 (SURR)
	1	0					0	VER 3 (REAR)
	1	1					0	FIX

Table 15.

POWER ON RESET	
BASS & MIDDLE	2dB
TREBLE	0dB
SURROUND & OUT CONTROL+ EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
SPEAKER/AUX ATTENUATION L &R	MUTE
INPUT ATTENUATION + REAR SWITCH	MAX ATTENUATION + ON
NATURAL BASE	OFF
INPUT	IN1

Figure 14. PINS: L-OUT, R-OUT, RECOUT-L, RECOUT-R,

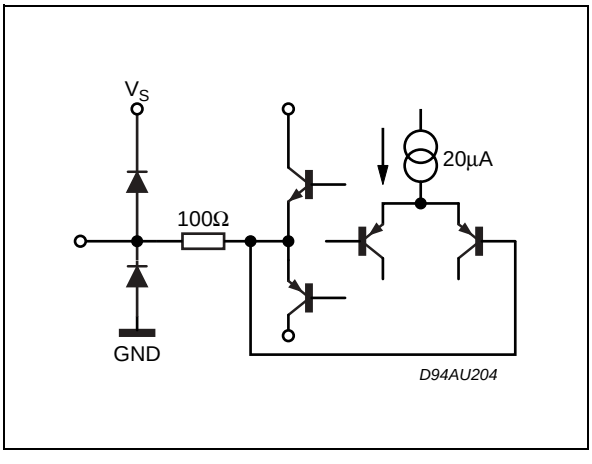


Figure 15. PIN: HP1

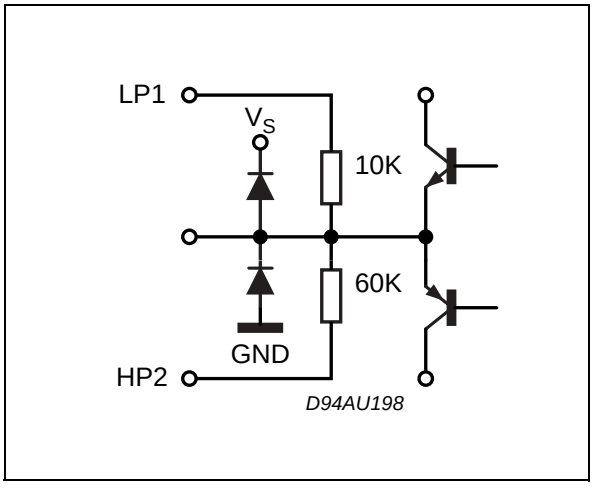


Figure 16. PIN: HP2

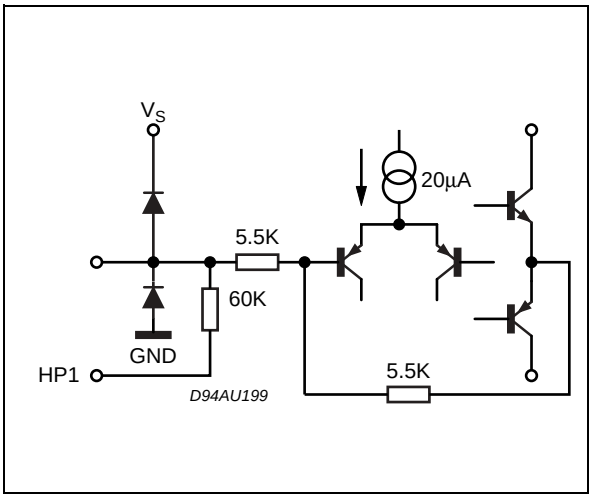


Figure 17. PIN: VAR-L, VAR-R,

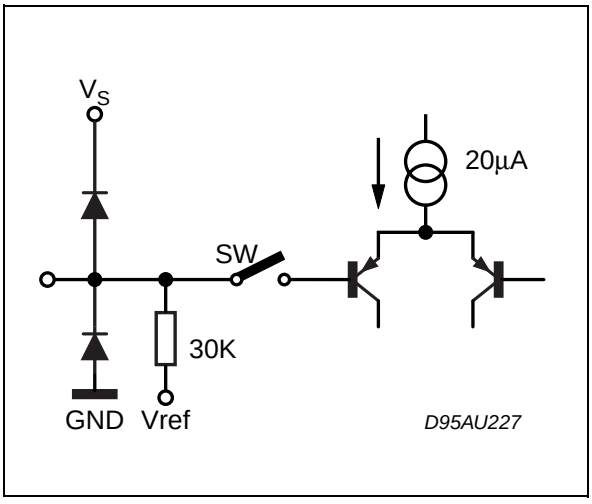


Figure 18. PIN: L-IN, R-IN, L-IN2, R-IN2, L-IN3, R-IN3, L-IN4, R-IN4,

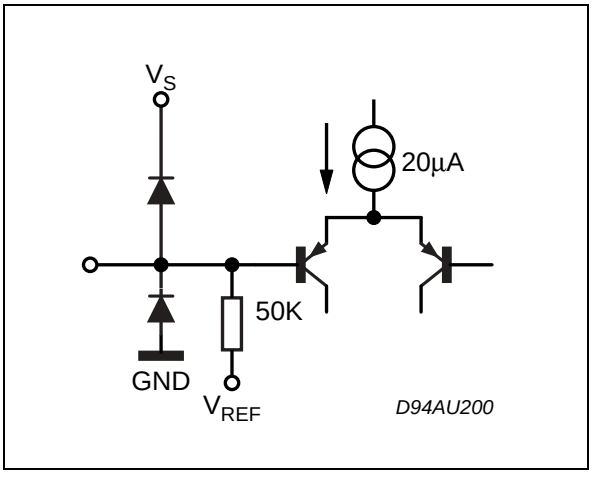


Figure 19. PIN: LP1

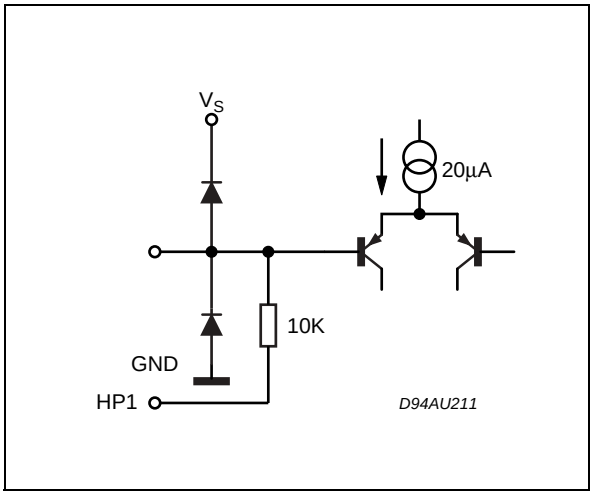


Figure 20. PIN: CREF

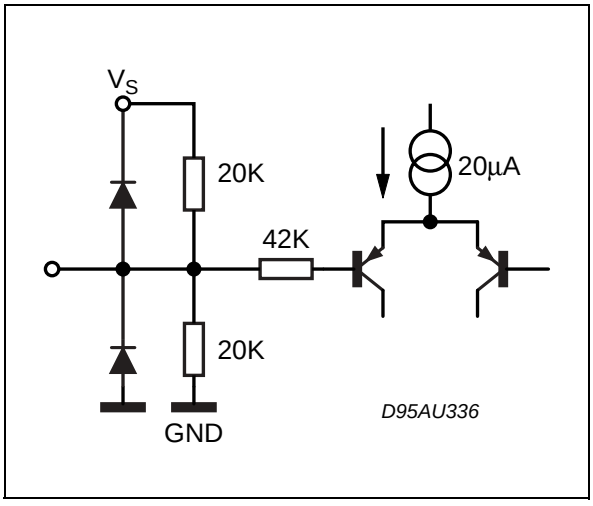


Figure 21. PIN: SCL, SDA

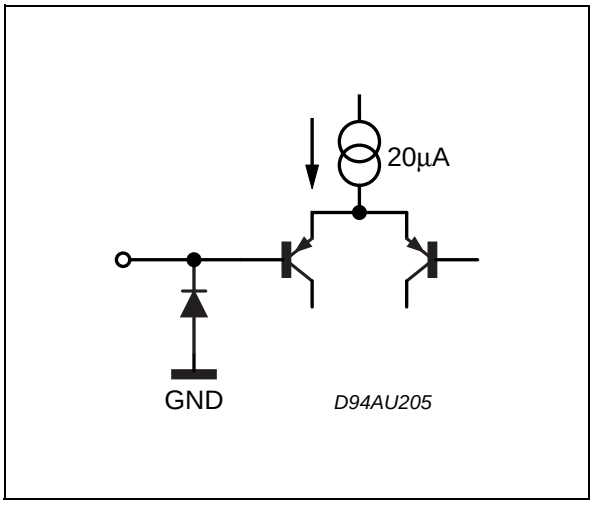


Figure 22. PIN: PS1, PS2, PS3, PS4, LP

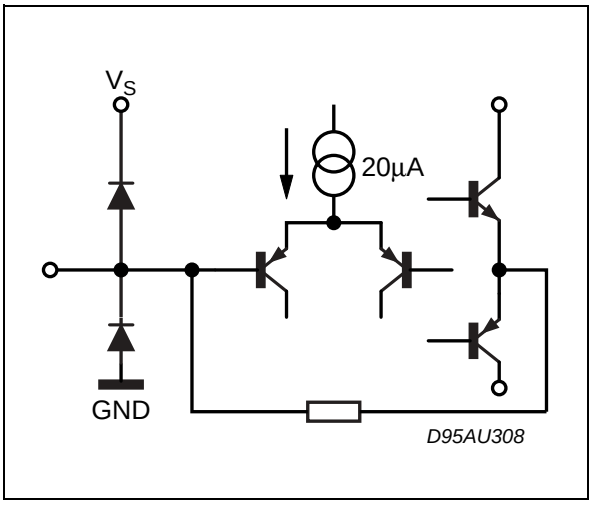


Figure 23. PIN: ADDR

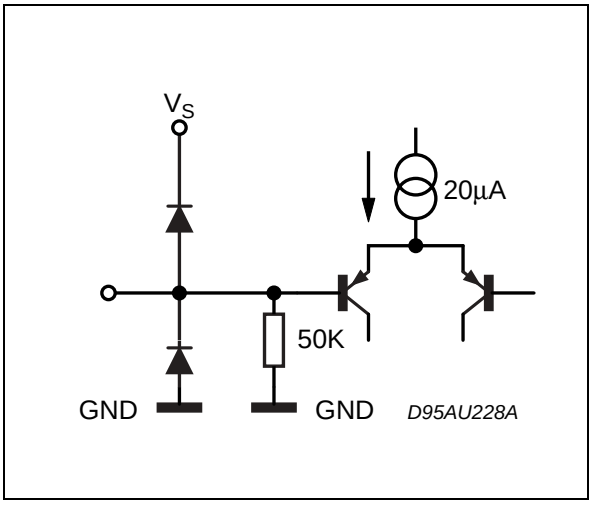


Figure 24. PIN: REARIN

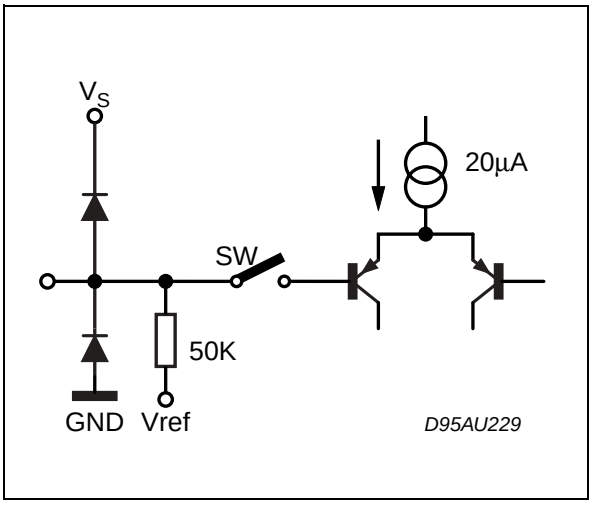


Figure 25. PIN: MIX

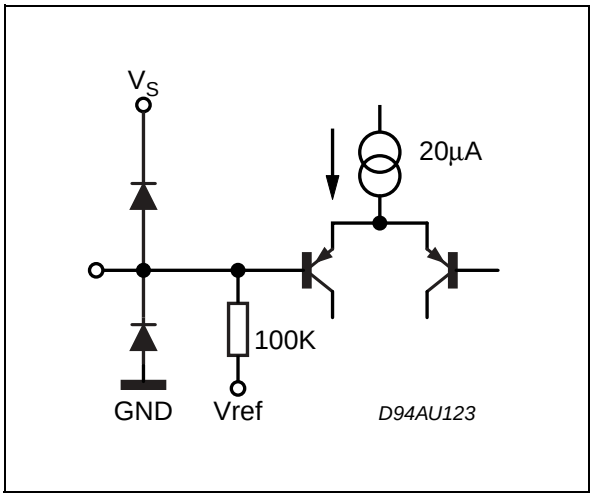


Figure 26. PINS: REAEROUT, BASSO-L, BASSO-R

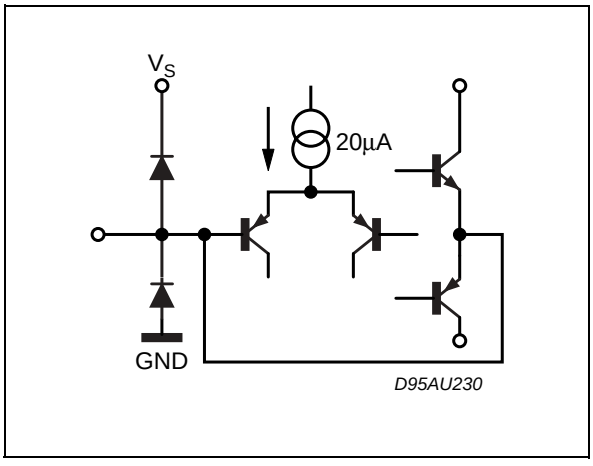


Figure 27. BASS-LI, BASS-RI, MIDDLE-L, MIDDLE-RII

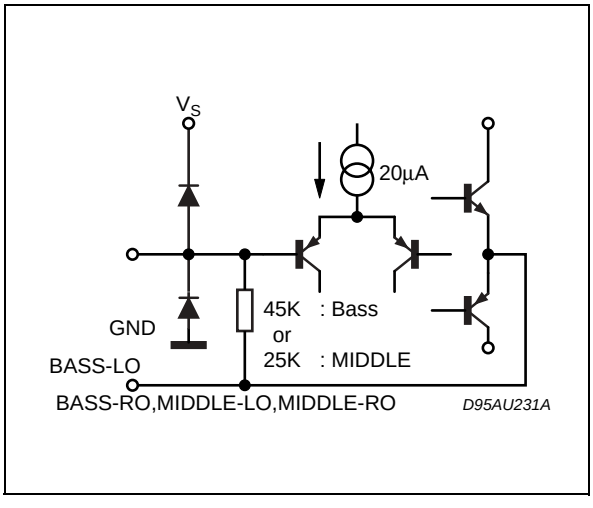


Figure 28. PIN: BASS-LO, BASS-RO, MIDDLE-LO, MIDDLE-RO,

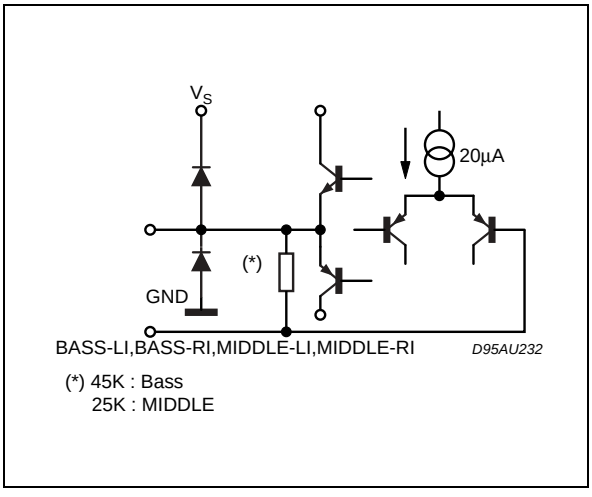


Figure 29. PIN:TREBLE-L, TREBLE-R,

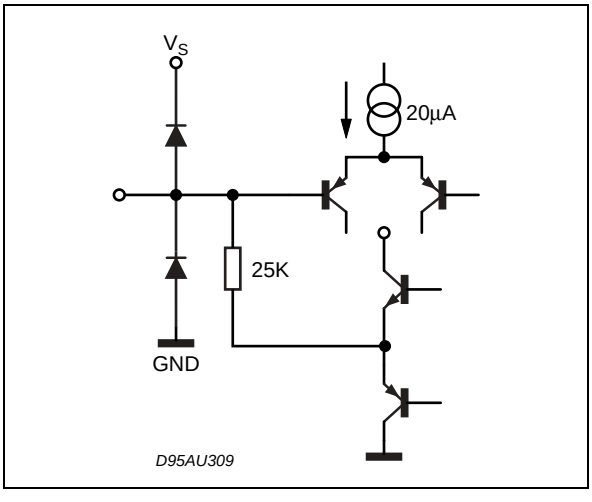


Figure 30. PIN VOUT REF,

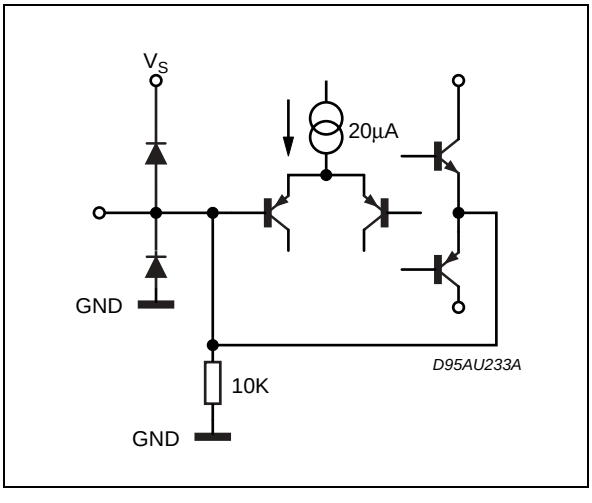


Figure 31. NBLIN, NBRIN

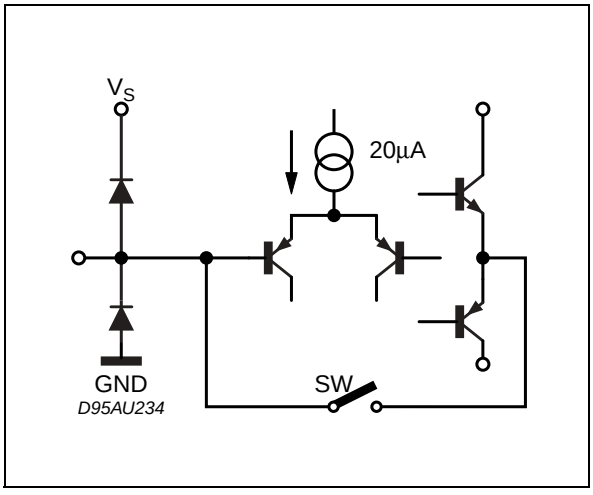


Figure 32. NBLO, NBRO

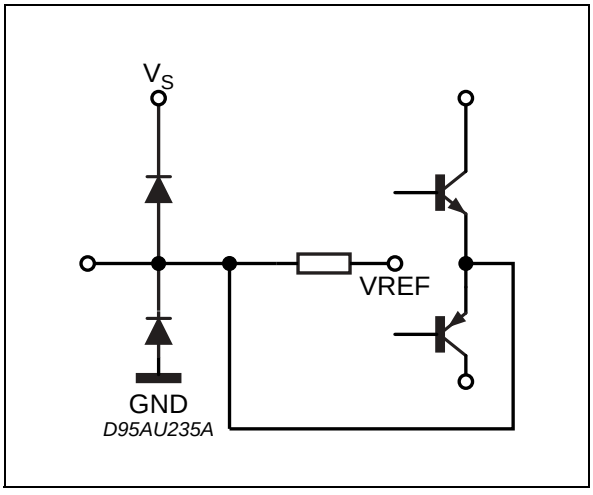
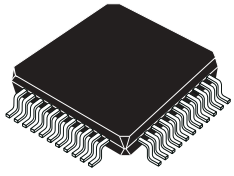


Figure 33. TQFP44 (10 x 10) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0˚(min.), 3.5˚(typ.), 7˚(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)

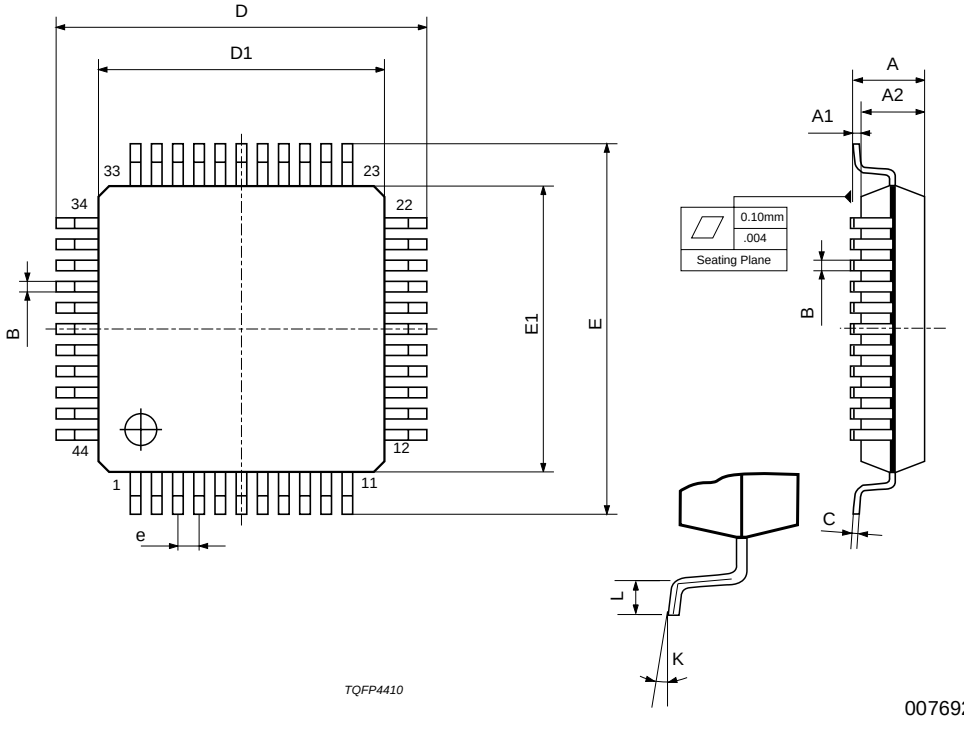
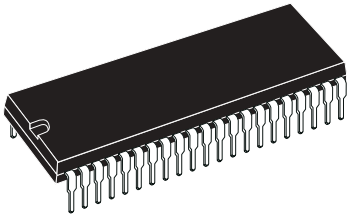


Figure 34. SDIP42 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

OUTLINE AND MECHANICAL DATA



SDIP42 (0.600")

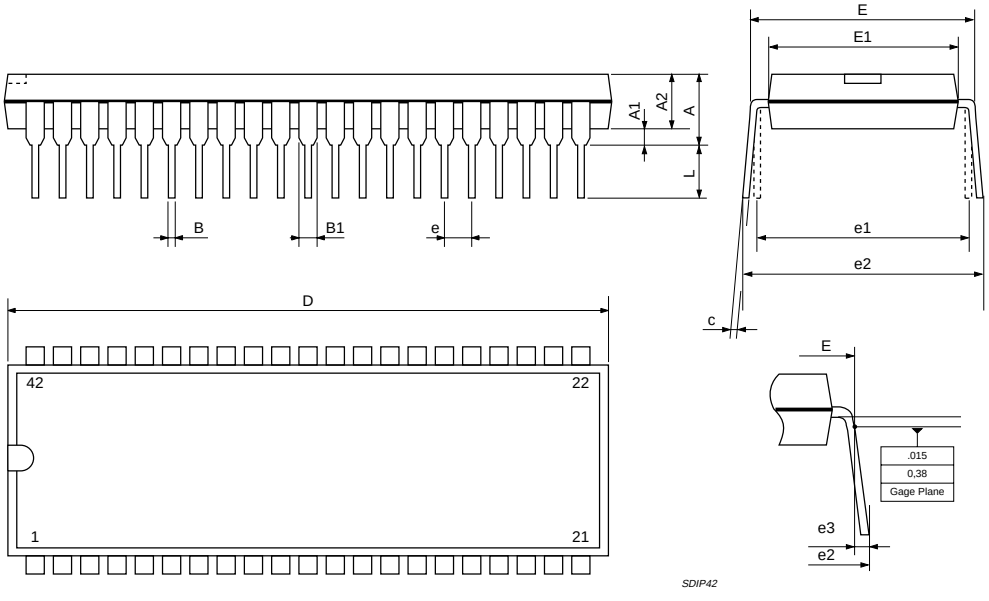


Table 16. Revision History

Date	Revision	Description of Changes
January 2004	9	First Issue in EDOCS DMS
June 2004	10	Changed the Style-sheet in compliance to the new “Corporate Technical Pubblications Design Guide”