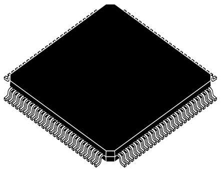
# TDA7505

## Car radio DSP for advanced signal processing

## Features

- Full software flexibility with two 24x24 bit DSP cores
- FM processing
- AM processing
- Dolby B noise reduction
- MP3 and C3 decoding
- Echo AND noise cancellation
- Audio processor
- Special sound effect processor
- Dual media processing
- RDS Filter, Demodulator & Decoder
- 4 + 1 channel ADC, 6 channel DAC CODEC
- IIC/SPI control busses
- SAI 6 channel serial audio interface
- SPDIF interface with sample rate converter
- Dual core external memory interface
- Debug interface
- On-chip PLL
- 5V-tolerant 3V I/O interface
- Multifunction general purpose I/O ports



**LQFP100**
**(14x14x1.4mm)**

## Description

The TDA7505 is an MPX-sampling DSP for car radio applications.

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| TDA7505 | LQFP100 | Tray |

# Contents

# List of tables

# List of figures

# 1 Overview

The TDA7505 integrates two 75 MIPS DSP cores. One core is used for stereo decoding, noise blanking, weak signal processing, Dolby B, music search and MP3 decoding. The second core is used for audio and sound processing and Echo & Noise cancellation. All functions are realized in SW and thus are flexible on customer request.

The device may be controlled by a main micro through either SPI or $I^2C$ interface. Through the same pins, but with separate device address ($I^2C$) respectively separate chip select line (SPI) the main micro may communicate with the DSP or with the RDS block.

An additional SPI is available allowing a separate communication (e.g. to a display micro).

The DSP cores are integrated with their associated data and program memories.

DSP0 is declared as master. Its associated peripherals and interfaces are: $I^2C$, SPI1 (Master SPI), SPI2 (Display SPI), Serial Audio Interface (SAI), PLL Oscillator, External Memory Interface (EMI), General Purpose I/O ports (DSP0 GPIO[0..11]), RDS filter and D/A converters.

DSP1 is declared as Co-DSP. Its associated peripherals and interfaces are: A/D converters, SPDIF, Sample Rate Converter (SRC) and General Purpose I/O ports (DSP1 GPIO[0..11]).

Both DSP´s are identical (ST Orpheus core, 75 MHz clock). Only the peripherals and memory configurations are different. The internal communication takes place through a bi-directional 24/10-word exchange interface (XCHG) with complex flag and interrupts capability.

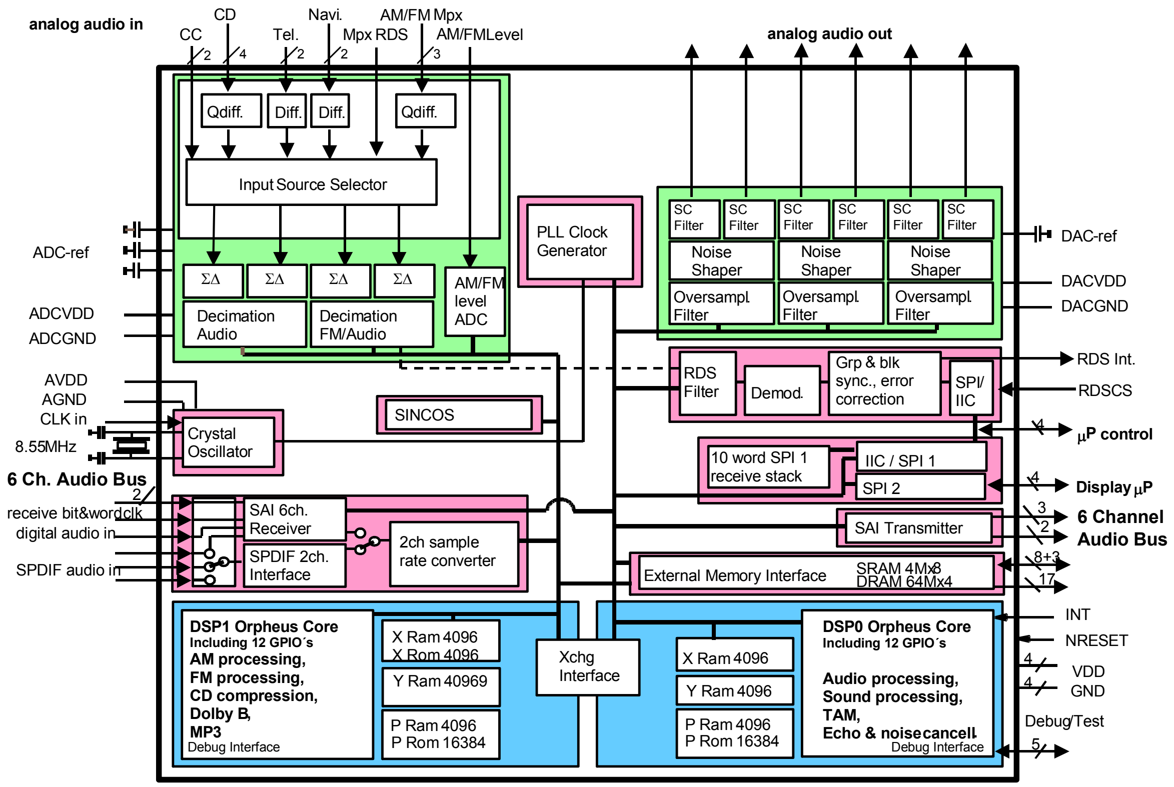
The Radio Data System (RDS, respectively RBDS) function is realized via dedicated hardware. It may run fully autonomous without SW intervention. Thus an efficient background mode as well as a low current standby mode is possible. The RDS input is connected to the A/D converter to receive the FM multiplex signal (MPX) automatically. Its output may be configured to $I^2C$ or SPI format. The pins are shared with the $I^2C$ and SPI1 of DSP0.

The device is equipped with a debug and test interface. It allows the SW development with a 100% compatible emulation system.

All functions, except RDS, are implemented in SW. Thus, the device may be adapted to customers´ requirements. This implies the variable implementation of SW modules developed by the customer, ST and third parties. This flexibility also allows the usage for applications others than car radios, e.g.: Boosters.

# 2 Block diagram

Figure 1. Block diagram



# 3 Pin description

Table 2. Pin description

<table>
<tr><th>N°</th><th>Name</th><th>Type</th><th colspan="6">Function</th></tr>
<tr><td>1</td><td>DAC4</td><td>A</td><td colspan="6">Signal output D/A converter (single ended)</td></tr>
<tr><td>2</td><td>DAC5</td><td>A</td><td colspan="6">Signal output D/A converter (single ended)</td></tr>
<tr><th>N°</th><th>Name</th><th>Type</th><th colspan="4">Voltage</th><th colspan="2">Function</th></tr>
<tr><td>3</td><td>VDD1V8_1</td><td>S</td><td colspan="4">1.8V</td><td colspan="2">Digital Supply dedicated to internal logic</td></tr>
<tr><td>4</td><td>GND1V8_1</td><td>S</td><td colspan="4">0V</td><td colspan="2">Digital Ground dedicated to internal logic</td></tr>
<tr><th rowspan="2">N°</th><th rowspan="2">Name</th><th rowspan="2">Type</th><th rowspan="2">Reset state</th><th colspan="3">After boot with</th><th rowspan="2">I/O</th><th rowspan="2">Function</th></tr>
<tr><th>SPI</th><th>$I^2C$ *</th><th>EMI</th></tr>
<tr><td>5</td><td>NRESET</td><td>I</td><td>E0</td><td>E1</td><td>E1</td><td>E1</td><td>Input 5VT</td><td>System Reset. A low level applied to NRESET input initializes the IC.</td></tr>
<tr><td>6</td><td>SRCCD<br>MISOD output<br>MISOD input</td><td>I/O</td><td>Z</td><td>Z</td><td>Z</td><td>Z</td><td>Input 5VT<br>Output 2mA PP/OD<br>Input 5VT</td><td>SPDIF input source 1 (e.g.: CD)<br>Display SPI SO (slave mode)<br>Display SPI MI (master mode)</td></tr>
<tr><td>7</td><td>SRCMD<br>MOSID input<br>MOSID output<br>DSP0 GPIO0<br>DSP0 GPIO0</td><td>I/O</td><td>Z</td><td>Z</td><td>Z</td><td>Z</td><td>Input 5VT<br>Input 5VT<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP</td><td>SPDIF input source 2 (e.g.: MD)<br>Display SPI SI (slave mode)<br>Display SPI MO (master mode)<br>GPIO input<br>GPIO output</td></tr>
<tr><td>8</td><td>SSD input<br>INT<br>DSP0 GPIO1<br>DSP0 GPIO1</td><td>I/O</td><td>Z</td><td>Z</td><td>Z</td><td>Z</td><td>Input 5VT<br>Input 5VT<br>Input 5VT<br>Output 2mA PP</td><td>Display SPI SS slave select<br>DSP0 external interrupt (IRQA)<br>GPIO input<br>GPIO output</td></tr>
<tr><td>9</td><td>CLKIN<br>SCKD input<br>SCKD output</td><td>I/O</td><td>Z</td><td>Z</td><td>Z</td><td>Z</td><td>Input 5VT<br>Input 5VT<br>Output 2mA PP</td><td>External clock input for PLL<br>Display SPI clock (slave mode)<br>Display SPI clock (master mode)</td></tr>
<tr><th>N°</th><th>Name</th><th>Type</th><th colspan="4">Voltage</th><th colspan="2">Function</th></tr>
<tr><td>10</td><td>AVDD</td><td>S</td><td colspan="4">3.3V</td><td colspan="2">Supply dedicated to the PLL</td></tr>
<tr><td>11</td><td>XTI</td><td>A</td><td colspan="4">AC</td><td colspan="2">Crystal oscillator input</td></tr>
<tr><td>12</td><td>XTO</td><td>A</td><td colspan="4">AC</td><td colspan="2">Crystal oscillator output</td></tr>
<tr><td>13</td><td>AGND</td><td>S</td><td colspan="4">0V</td><td colspan="2">Ground dedicated to the PLL</td></tr>
</table>

**Table 2. Pin description (continued)**

| N° | Name | Type | Reset State | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 14 | RDSCS<br>-<br>DSP0 GPIO2<br>DSP0 GPIO2 | I/O | Z | Z | Z | Z | Input 5VT<br>Output 2mA OD<br>Input 5VT<br>Output 2mA PP | RDS SPI CS chip select in<br>RDS bit data<br>GPIO input<br>GPIO output |
| 15 | INT<br>-<br>RDSINT<br>DSP0 GPIO3<br>DSP0 GPIO3 | I/O | Z | Z | Z | Z | Input 5VT<br>Output 2mA OD<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | DSP0 external interrupt (IRQA)<br>RDS bit clock<br>RDS Interrupt Output<br>GPIO input<br>GPIO output |
| **N°** | **Name** | **Type** | **Voltage** | | | | **Function** | |
| 16 | VDD3V3_1 | S | 3.3V | | | | Digital supply dedicated to I/O structures | |
| 17 | GND3V3_1 | S | 0V | | | | Digital ground dedicated to I/O structures | |
| 18 | SCKM input<br>SCKM output<br>SCL bi-direct<br>DSP0 GPIO4<br>DSP0 GPIO4 | I/O | Z | 0/1 | Z | Z | Input 5VT<br>Output 2mA PP<br>In 5VT/Out 2mA OD<br>Input 5VT<br>Output 2mA PP | Master/RDS SPI clock (slave m.)<br>Master SPI clock (master mode)<br>$I^2C$ clock<br>GPIO input<br>GPIO output |
| **N°** | **Name** | **Type** | **Reset state** | **After boot with** | | | **I/O** | **Function** |
| | | | | **SPI** | **$I^2C$ *** | **EMI** | | |
| 19 | MISOM output<br>MISOM input<br>ADDR select<br>DSP0 GPIO5<br>DSP0 GPIO5 | I/O | Z | 0/1 | Z | Z | Output 2mA PP/OD<br>Input 5VT<br>Input 5VT<br>Input 5VT<br>Output 2mA PP | Master/RDS SPI SO (slave m.)<br>Master SPI MI (master mode)<br>$I^2C$ Address select line<br>GPIO input<br>GPIO output |
| 20 | MOSIM input<br>MOSIM output<br>SDA bi-direct<br>DSP0 GPIO6<br>DSP0 GPIO6 | I/O | Z | 0/1 | Z | Z | Input 5VT<br>Output 2mA PP<br>In 5VT/Out 2mA OD<br>Input 5VT<br>Output 2mA PP | Master/RDS SPI SI (slave m.)<br>Master SPI MO (master mode)<br>$I^2C$ data<br>GPIO input<br>GPIO output |
| 21 | SSM input<br>DSP0 GPIO7<br>DSP0 GPIO7 | I/O | Z | Z | Z | Z | Input 5VT<br>Input 5VT<br>Output 2mA PP | Master SPI SS slave select<br>GPIO input<br>GPIO output |
| 22 | DSRA<0><br>DSRA<0> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP<br>In/Out 2mA PP | EMI SRAM Data 0<br>EMI DRAM Data 0 |
| 23 | DSRA<1><br>DSRA<1> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP<br>In/Out 2mA PP | EMI SRAM Data 1<br>EMI DRAM Data 1 |
| 24 | DSRA<2><br>DSRA<2> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP<br>In/Out 2mA PP | EMI SRAM Data 2<br>EMI DRAM Data 2 |

**Table 2. Pin description (continued)**

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 25 | DSRA<3><br>DSRA<3> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP<br>In/Out 2mA PP | EMI SRAM Data 3<br>EMI DRAM Data 3 |
| 26 | DSRA<4> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP | EMI SRAM Data 4 |
| 27 | DSRA<5> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP | EMI SRAM Data 5 |
| 28 | DSRA<6> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP | EMI SRAM Data 6 |
| 29 | DSRA<7> | I/O | 0 | 1 | 1 | Z | In/Out 2mA PP | EMI SRAM Data 7 |
| 30 | SRA<0><br>SRA<0> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 0<br>EMI DRAM Address 0 |
| 31 | SRA<1><br>SRA<1> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 1<br>EMI DRAM Address 1 |

| N° | Name | Type | Voltage | Function |
|---|---|---|---|---|
| 32 | VDD3V3_2 | S | 3.3V | Digital Supply dedicated to I/O structures |
| 33 | GND3V3_2 | S | 0V | Digital Ground dedicated to I/O structures |

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 34 | SRA<2><br>SRA<2> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 2<br>EMI DRAM Address 2 |
| 35 | SRA<3><br>SRA<3> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 3<br>EMI DRAM Address 3 |
| 36 | SRA<4><br>SRA<4> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 4<br>EMI DRAM Address 4 |
| 37 | SRA<5><br>SRA<5> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 5<br>EMI DRAM Address 5 |
| 38 | SRA<6><br>SRA<6> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 6<br>EMI DRAM Address 6 |
| 39 | SRA<7><br>SRA<7> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 7<br>EMI DRAM Address 7 |
| 40 | SRA<8><br>SRA<8> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 8<br>EMI DRAM Address 8 |
| 41 | SRA<9><br>SRA<9> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 9<br>EMI DRAM Address 9 |
| 42 | SRA<10><br>SRA<10> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 10<br>EMI DRAM Address 10 |

**Table 2. Pin description (continued)**

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | I$^2$C * | EMI | | |
| 43 | SRA<11><br>SRA<11> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 11<br>EMI DRAM Address 11 |
| 44 | SRA<12><br>SRA<12> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI SRAM Address 12<br>EMI DRAM Address 12 |
| **N°** | **Name** | **Type** | **Voltage** | | | | **Function** | |
| 45 | VDD1V8_2 | S | 1.8V | | | | Digital Supply dedicated to internal logic | |
| 46 | GND1V8_2 &<br>GND3V3_3 | S | 0V | | | | Digital Ground dedicated to internal logic and I/O structures | |
| 47 | VDD3V3_3 | S | 3.3V | | | | Digital Supply dedicated to I/O structures | |
| **N°** | **Name** | **Type** | **Reset state** | **After boot with** | | | **I/O** | **Function** |
| | | | | **SPI** | **I$^2$C *** | **EMI** | | |
| 48 | DRD | O | 1 | 1 | 1 | 1 | Output 2mA PP | EMI data read strobe |
| 49 | DWR | O | 1 | 1 | 1 | 1 | Output 2mA PP | EMI data write strobe |
| 50 | CAS<br>SRA<13> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP<br>Output 2mA PP | EMI DRAM CAS<br>EMI SRAM Address 13 |
| 51 | SRA<14> | O | 0 | 1 | 1 | 0/1 | Output 2mA PP | EMI SRAM Address 14 |
| 52 | SRA<15><br>DSP0 GPIO8<br>DSP0 GPIO8 | I/O | Z | Z | Z | 0/1 | Output 2mA PP<br>Input 5VT<br>Output 2mA PP | EMI SRAM Address 15<br>GPIO input<br>GPIO output |
| 53 | INOUTA<br>SRA<16><br>DSP1 GPIO0<br>DSP1 GPIO0 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 16<br>GPIO input<br>GPIO output |
| 54 | INOUTB<br>SRA<17><br>DSP1 GPIO1<br>DSP1 GPIO1 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 17<br>GPIO input<br>GPIO output |
| 55 | INOUTC<br>SRA<18><br>DSP1 GPIO2<br>DSP1 GPIO2 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 18<br>GPIO input<br>GPIO output |
| **N°** | **Name** | **Type** | **Reset state** | **After boot with** | | | **I/O** | **Function** |
| | | | | **SPI** | **I$^2$C *** | **EMI** | | |
| 56 | INOUTD<br>SRA<19><br>DSP1 GPIO3<br>DSP1 GPIO3 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 19<br>GPIO input<br>GPIO output |

**Table 2. Pin description (continued)**

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 57 | INOUTE<br>SRA<20><br>DSP1 GPIO4<br>DSP1 GPIO4 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 20<br>GPIO input<br>GPIO output |
| 58 | INOUTF<br>SRA<21><br>RAS<br>DSP1 GPIO5<br>DSP1 GPIO5 | I/O | Z | Z | Z | 0/1 | In 5VT/Out 2mA PP<br>Output 2mA PP<br>Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>EMI SRAM Address 21<br>EMI DRAM RAS<br>GPIO input<br>GPIO output |
| 59 | INOUTG<br>DSP1 GPIO6<br>DSP1 GPIO6 | I/O | Z | Z | Z | Z | In 5VT/Out 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>GPIO input<br>GPIO output |
| 60 | INOUTH<br>DSP1 GPIO7<br>DSP1 GPIO7 | I/O | Z | Z | Z | Z | In 5VT/Out 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>GPIO input<br>GPIO output |

| N° | Name | Type | Voltage | Function |
|---|---|---|---|---|
| 61 | VDD3V3_4 | S | 3.3V | Digital Supply dedicated to I/O structures |
| 62 | GND3V3_4 | S | 0V | Digital Ground dedicated to I/O structures |

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 63 | INOUTI<br>DSP1 GPIO8<br>DSP1 GPIO8 | I/O | Z | Z | Z | Z | In 5VT/Out 2mA PP<br>Input 5VT<br>Output 2mA PP | Multi function I/O<br>GPIO input<br>GPIO output |
| 64 | INOUTJ | I/O | Z | Z | Z | Z | In 5VT/Out 2mA PP | Multi function I/O |
| 65 | DBCK<br>OS1<br>DSP0/1 GPIO9<br>DSP0/1 GPIO9 | I/O | Z | 0 | 0 | 0 | Input 5VT<br>Out 2mA PP<br>Input 5VT<br>Output 2mA PP | Debug clock<br>Chip status 1<br>GPIO input<br>GPIO output |
| 66 | DBOUT<br>DSP0/1 GPIO10<br>DSP0/1 GPIO10 | I/O | Z | 1 | 1 | 1 | Output 2mA PP<br>Input 5VT<br>Output 2mA PP | Debug output<br>GPIO input<br>GPIO output |

| N° | Name | Type | Reset state | After boot with | | | I/O | Function |
|---|---|---|---|---|---|---|---|---|
| | | | | SPI | $I^2C$ * | EMI | | |
| 67 | DBIN<br>OS0<br>DSP0/1 GPIO11<br>DSP0/1 GPIO11 | I/O | Z | 0 | 0 | 0 | Input 5VT<br>Out 2mA PP<br>Input 5VT<br>Output 2mA PP | Debug input<br>Chip status 0<br>GPIO input<br>GPIO output |

**Table 2. Pin description (continued)**

| **N°** | **Name** | **Type** | **Reset state** | **After boot with** | | | **I/O** | **Function** |
|---|---|---|---|---|---|---|---|---|
| | | | | **SPI** | **$I^2C$ *** | **EMI** | | |
| 68 | Debug/Test_Sel0 | I | E1 | E1 | E1 | E1 | Input | Mode select (Debug0/1, Test) |
| 69 | Debug/Test_Sel1 | I | E1 | E1 | E1 | E1 | Input | Mode select (Debug0/1, Test) |
| 70 | INOUTK | I/O | 0 | 0 | 0 | 0 | In 5VT/Out 2mA PP | Multi function I/O |
| **N°** | **Name** | **Type** | **Voltage** | | | | **Function** | |
| 71 | VDD1V8_3 | S | 1.8V | | | | Digital Supply dedicated to internal logic | |
| 72 | GNDSUB_D | S | 0V | | | | Digital substrate Ground | |
| **N°** | **Name** | **Type** | **Function** | | | | | |
| 73 | LEVEL_AM/FM | A | Signal input to level ADC (single ended) | | | | | |
| 74 | MPX_AM+ | A | Signal input tuner AM (quasi differential) | | | | | |
| 75 | MPX_AM/FM- | A | Signal input tuner common ground (quasi differential) | | | | | |
| 76 | MPX_FM+ | A | Signal input tuner FM (quasi differential) | | | | | |
| 77 | MPX_RDS | A | Signal input background tuner (for RDS) single ended | | | | | |
| 78 | Navi- | A | Signal input from navigation system (differential) | | | | | |
| 79 | Navi+ | A | Signal input from navigation system (differential) | | | | | |
| 80 | Phone- | A | Signal input from Telephone (differential) | | | | | |
| 81 | Phone+ | A | Signal input from Telephone (differential) | | | | | |
| **N°** | **Name** | **Type** | **Voltage** | | | | **Function** | |
| 82 | ADCGND | S | 0V | | | | Analog Ground dedicated to the A/D converter | |
| 83 | ADCVDD | S | 3.3V | | | | Analog Supply dedicated to the A/D converter | |
| **N°** | **Name** | **Type** | **Function** | | | | | |
| 84 | ADCREF3 | A | ADC reference voltage decoupling | | | | | |
| 85 | CD_R+ | A | Signal right input from CD-changer (differential) | | | | | |
| 86 | CD_R- | A | Signal right input from CD-changer (differential) | | | | | |
| 87 | ADCREF2 | A | ADC reference voltage decoupling | | | | | |
| 88 | CD_L- | A | Signal left input from CD-changer (differential) | | | | | |
| 89 | CD_L+ | A | Signal left input from CD-changer (differential) | | | | | |
| 90 | ADCREF1 | A | ADC reference voltage decoupling | | | | | |
| 91 | CC_R | A | Signal right input from cassette (single ended) | | | | | |
| 92 | CC_L | A | Signal left input from cassette (single ended) | | | | | |
| **N°** | **Name** | **Type** | **Voltage** | | | | **Function** | |
| 93 | GNDSUB_A | S | 0V | | | | Analog substrate Ground | |
| 94 | DACVDD | S | 3.3V | | | | Analog Supply dedicated to the D/A converter. | |

**Table 2. Pin description (continued)**

<table>
<tr><th>N°</th><th>Name</th><th>Type</th><th colspan="2">Function</th></tr>
<tr><td>95</td><td>DACREF</td><td>A</td><td colspan="2">DAC reference voltage decoupling</td></tr>
<tr><th>N°</th><th>Name</th><th>Type</th><th>Voltage</th><th>Function</th></tr>
<tr><td>96</td><td>DACGND</td><td>S</td><td>0V</td><td>Analog Ground dedicated to the D/A converter.</td></tr>
<tr><th>N°</th><th>Name</th><th>Type</th><th colspan="2">Function</th></tr>
<tr><td>97</td><td>DAC0</td><td>A</td><td colspan="2">Signal output D/A converter (single ended)</td></tr>
<tr><td>98</td><td>DAC1</td><td>A</td><td colspan="2">Signal output D/A converter (single ended)</td></tr>
<tr><td>99</td><td>DAC2</td><td>A</td><td colspan="2">Signal output D/A converter (single ended)</td></tr>
<tr><td>100</td><td>DAC3</td><td>A</td><td colspan="2">Signal output D/A converter (single ended)</td></tr>
</table>

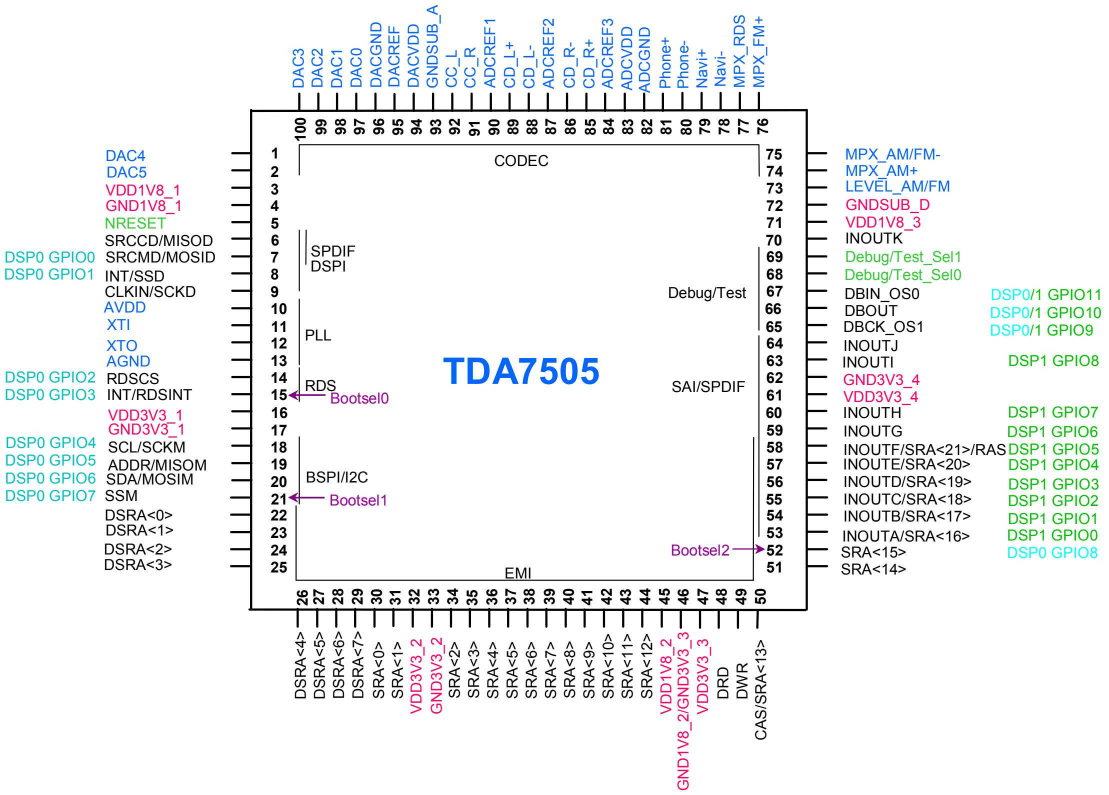
Type:
S: Supply pin
I: Digital Input pin
O: Digital Output pin
A: Analog pin

0: logic low output
1: logic high output
E0: logic low input
E1: logic high input
Z: high impedance (Input mode of bi-directional pin)

PP: push-pull
OD: open drain
5VT: 5 volt tolerant
Schmitt-trigger on all inputs

*) $I^2C$ Master boot mode, using multiplexed debug interface (pin15: INT/RDSINT = 1, pin21: SSM = 0, pin52: SRA15 = 0)

**Figure 2. LQFP100 pins connection (top view)**



# 4 Electrical specifications

## 4.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| VDD1V8 | Power supplies digital | | -0.5 to +1.95 | V |
| VDD3V3 | I/O | | -0.5 to +3.6 | V |
| AVDD | Analog | | -0.5 to +3.6(1) | V |
| DACVDD | DAC | | -0.5 to +3.6(1) | V |
| ADCVDD | ADC | | -0.5 to +3.6(1) | V |
| | Analog input or output voltage | | -0.5 to (AVDD+0.5) (1) | V |
| | Digital input or output voltage, 5V tolerant | Normal(2) | -0.5 to 6.3 | V |
| | | Fail-safe(3) | -0.5 to 3.8 | V |
| $T_{op}$ | Operating temperature range | | -40 to 85 | °C |
| $T_{stg}$ | Storage temperature | | -55 to 150 | °C |

1. The maximum difference in the voltage of AVDD, DACVDD, ADCVDD, analog inputs and analog outputs must not exceed 0.5V. Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. During Normal Mode operation VDD3 is always available as specified.
3. During Fail-save Mode operation VDD3 may be not available.

## 4.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction to ambient (1) | 55 | °C/W |
| $T_j$ | Operating junction temperature | 125 | °C |
| $R_{th\ j\text{-}case}$ | Thermal junction to case (2) | 10 | °C/W |

1. In still air
2. Measured on top side of the package

## 4.3 Electrical characteristics

### 4.3.1 Recommended DC operating conditions

**Table 5. Recommended DC operating conditions**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD1V8 | Digital supply voltage | | 1.7 | 1.8 | 1.9 | V |
| VDD3V3 | I/O supply voltage | | 3.15 | 3.3 | 3.49 | V |
| AVDD | Analog supply voltage | | 3.15 | 3.3 | 3.49 | V |
| DACVDD | D/A supply voltage | | 3.15 | 3.3 | 3.49 | V |
| ADCVDD | A/D supply voltage | | 3.15 | 3.3 | 3.49 | V |

### 4.3.2 Power consumption

**Table 6. Power consumption**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{dd}$ | Maximum current | Digital power supply @ 1.8V | | 195 | | mA |
| $I_{dio}$ | Maximum current | Digital IO power supply @ 3.3V | | 6 | | mA |
| $I_{DAC}$ | Maximum current | DAC analog power supply @ 3.3V | | 22 | | mA |
| $I_{ADC}$ | Maximum current | ADC analog power supply @ 3.3V | | 43 | | mA |

Note: 75MHz internal DSP clock, all CODEC channels enabled at $T_{amb}$ = 25 °C

### 4.3.3 Oscillator characteristics

**Table 7. Oscillator characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC}$ | Crystal oscillator frequency(1) | | | 8.55 | | MHz |
| $F_{EXT}$ | External oscillator frequency | connected through pin XTI(1) | | | 75 | MHz |
| $F_{CLKIN}$ | External oscillator frequency | connected through pin CLKIN(2) | | | 80 | MHz |

1. RDS works only with 8.55Mhz quartz or alternative with 74.1MHz applied externally on XTI pin.
2. An alternative clock input (pin CLKIN) can be used for PLL to adjust the audio sampling rate. RDS can work in parallel with the 8.55MHz quartz.

### 4.3.4 General interface electrical characteristics

Table 8. General interface electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{il}$ | Low level input current without pull-up device | $V_i = 0V$(1) | | | 1 | µA |
| $I_{ih}$ | High level input current without pull-up device | $V_i = V_{DD3V3}$ (1) | | | 1 | µA |
| $I_{oz}$ | Tri-state output leakage without pull up/down device | $V_o = 0V$ or $V_{DD3V3}$(1) | | | 1 | µA |
| $I_{ozFT}$ | 5V tolerant tri-state output leakage without pull up/down device | $V_o = 0V$ or $V_{DD3V3}$(1) | | | 1 | µA |
| | | $V_o = 5.5V$ | | 1 | 7 | µA |
| $I_{latchup}$ | I/O latch-up current | $V_i < 0V$, $V_i > V_{DD3V3}$ | 200 | | | mA |
| $V_{esd}$ | Electrostatic protection | Leakage, 1µA (2) | 2000 | | | V |

1. The leakage currents are generally very small, <1nA. The value given here, 1 A, is a maximum that can occur after an electrostatic stress on the pin.
2. Human Body Model.

### 4.3.5 High voltage CMOS interface DC electrical characteristics

Table 9. High voltage CMOS interface DC electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{il}$ | Low Level Input Voltage | $3.0V<V_{DD3V3}<3.6V$ | | | $0.3*V_{DD3V3}$ | V |
| $V_{ih}$ | High Level Input Voltage | $3.0V<V_{DD3V3}<3.6V$ | $0.5*V_{DD3V3}$ | | | V |
| $V_{hyst}$ | Schmitt trigger hysteresis | $3.0V<V_{DD3V3}<3.6V$ | 0.8 | | | V |
| $V_{ol}$ | Low level output Voltage | $I_{ol}$ = XmA (1),(2) | | | $0.1*V_{DD3V3}$ | V |
| $V_{oh}$ | High level output Voltage | | $0.89*V_{DD3V3}$ | | | V |

1. Takes into account 200mV voltage drop in both supply lines.
2. X is the source/sink current under worst-case conditions and is depicted for every I/O or output pin in the pin description.

### 4.3.6 DSP core

Table 10. DSP core

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{dsp}$ | DSP clock frequency | | | 75 | | MHz |
| $T_{res}$ | Reset signal low state duration | | | 1 | | µs |

## 4.4 SAI interface timing - receiver

Figure 3. SAI interface timing - receiver

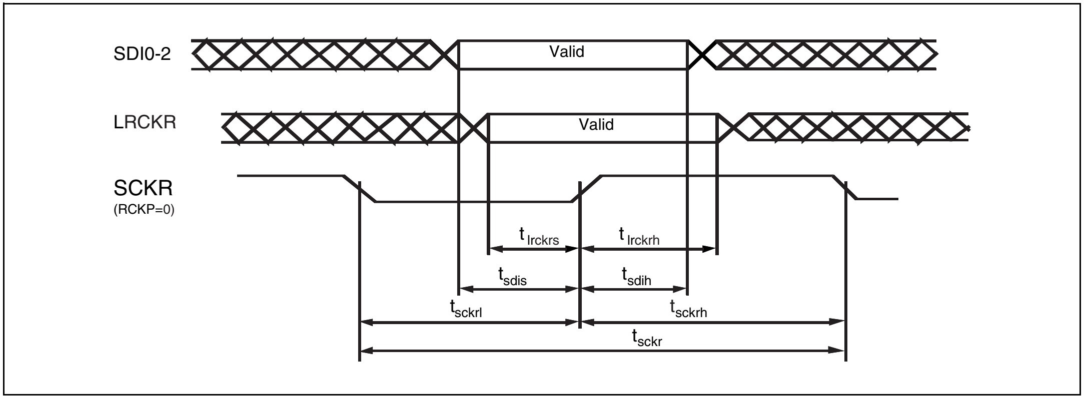


Table 11. SAI interface timing - receiver

| Timing | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{DSP}$(1) | Internal DSP clock period (typical 1/75MHz) | | 13.33 | | ns |
| $t_{sckr}$ | Minimum clock cycle | 6 $T_{DSP}$ | | | ns |
| $t_{lrckrs}$ | LRCKR setup time | $T_{DSP}$ | | | ns |
| $t_{lrckrh}$ | LRCKR hold time | $T_{DSP}$ | | | ns |
| $t_{sdid}$ | SDI setup time | $T_{DSP}$ | | | ns |
| $t_{sdih}$ | SDI hold time | $T_{DSP}$ | | | ns |
| $t_{sckrh}$ | Minimum SCKR high time | 0.35 $t_{sckr}$ | | | ns |
| $t_{sckrl}$ | Minimum SCKR low time | 0.35 $t_{sckr}$ | | | ns |

1. $T_{DSP}$ = DSP master clock cycle time = $1/F_{dsp}$

## 4.5 SAI interface timing - transmitter

Figure 4. SAI interface timing - transmitter

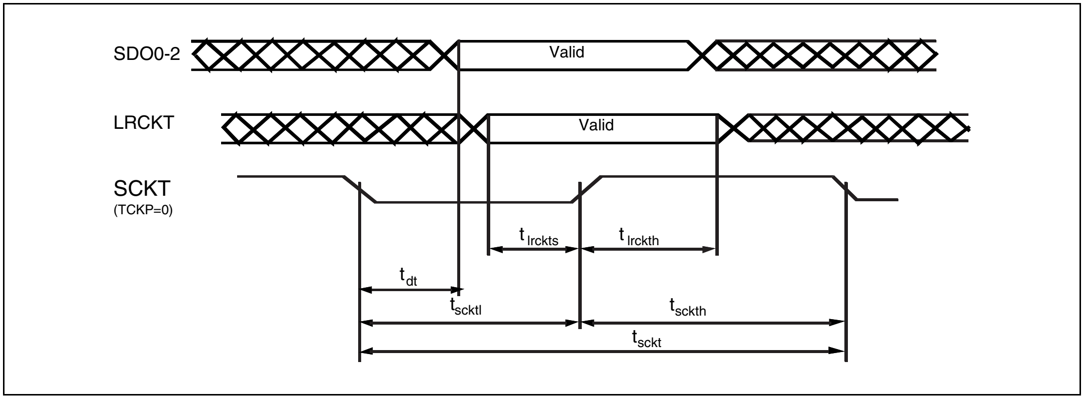


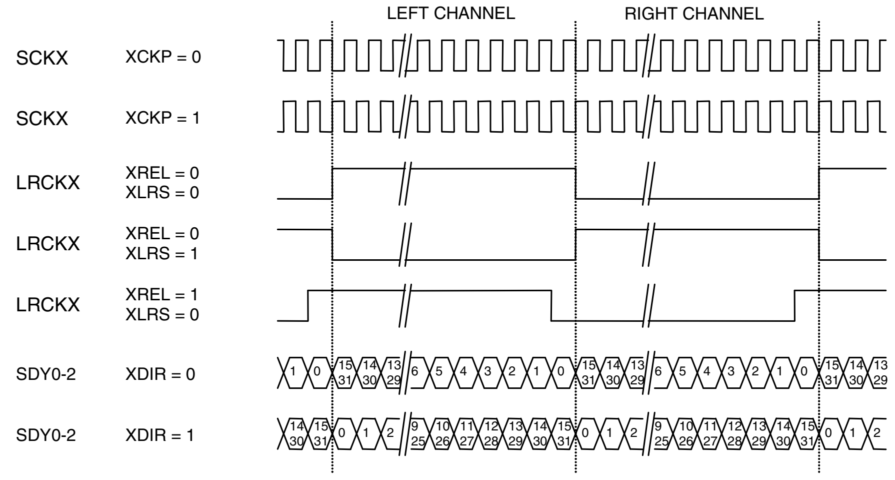
Table 12. SAI interface timing - transmitter

| Timing | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{DSP}$(1) | Internal DSP clock period (typical 1/75MHz) | | 13.33 | | ns |
| $t_{sckt}$ | Minimum clock cycle | 6 $T_{DSP}$ | | | ns |
| $t_{lrckts}$ | LRCKT setup time | $T_{DSP}$ | | | ns |
| $t_{lrckth}$ | LRCKT hold time | $T_{DSP}$ | | | ns |
| $t_{dt}$ | SCKT active edge to data out valid | $T_{DSP}$ | | | ns |
| $t_{sckth}$ | Minimum SCKT high time | 0.35 $t_{sckr}$ | | | ns |
| $t_{scktl}$ | Minimum SCKT low time | 0.35 $t_{sckr}$ | | | ns |

1. $T_{DSP}$ = DSP master clock cycle time = $1/F_{dsp}$

## 4.6 SAI protocol

Figure 5. SAI protocol



Notes: 1) X = R for receiver X = T for transmitter

2) Y = I for receiver Y = O for transmitter

## 4.7 SPDIF receiver

Table 13. SPDIF receiver

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{spdif}$ | Input sampling rate | $F_{dsp}$ = 75 MHz | 32 | | 96 | kHz |
| | Input precision with direct interface to DSP | | | | 24 | bit |
| | Input precision with interface to ASRC | | | | 20 | bit |

## 4.8 SPI interfaces (Buffered SPI, Display SPI, RDS SPI)

Figure 6. SPI interfaces

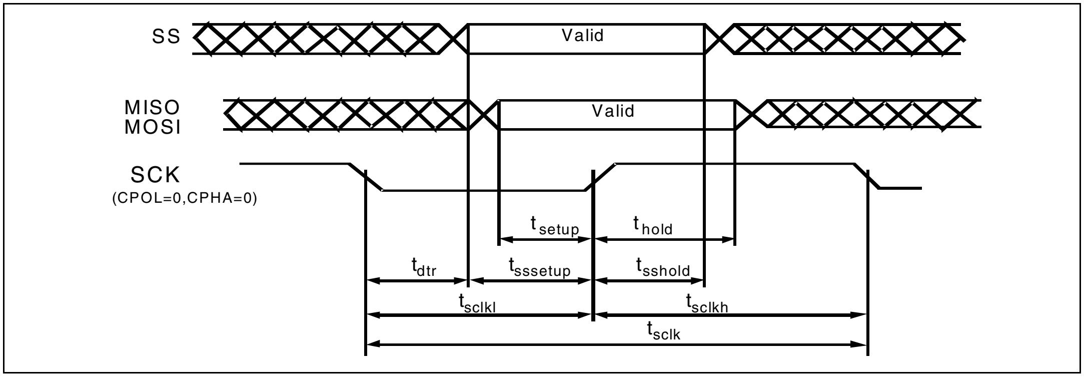
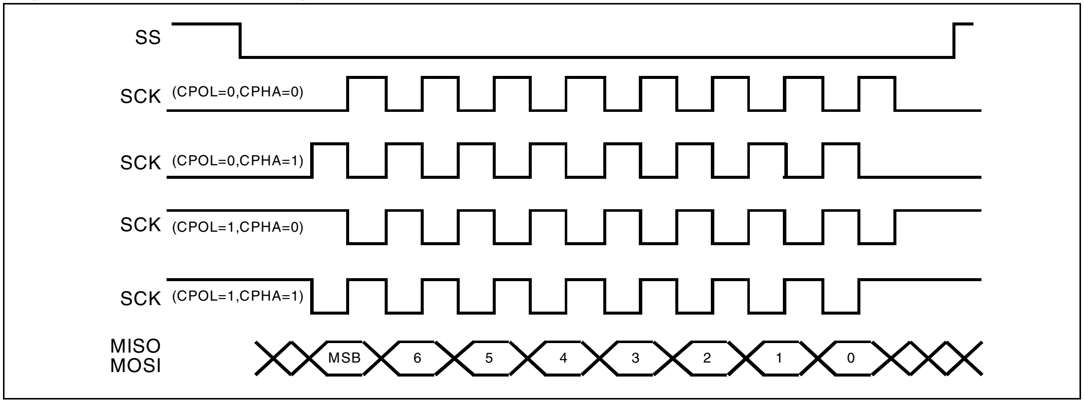


Table 14. SPI interfaces

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{DSP}$ | Internal DSP clock period (typical 1/75MHz) | | 13.33 | | ns |
| **Master mode** | | | | | |
| $t_{sclk}$ | Clock cycle | 12 $T_{DSP}$ | | | ns |
| $t_{dtr}$ | SCK edge to MOSI valid | 40 | | | ns |
| $t_{setup}$ | MISO setup time | 16 | | | ns |
| $t_{hold}$ | MISO hold time | 9 | | | ns |
| $t_{sclkh}$ | SCK high time | 0.5 $t_{sclk}$ | | | ns |
| $t_{sclkl}$ | SCK low time | 0.5 $t_{sclk}$ | | | ns |
| $t_{sssetup}$ | SS setup time | 40 | | | ns |
| $t_{sshold}$ | SS hold time | 25 | | | ns |
| **Slave mode** | | | | | |
| $t_{sclk}$ | Clock cycle | 12 $T_{DSP}$ | | | ns |
| $t_{dtr}$ | SCK edge to MOSI valid | 40 | | | ns |
| $t_{setup}$ | MOSI setup time | 16 | | | ns |
| $t_{hold}$ | MOSI hold time | 9 | | | ns |
| $t_{sclkh}$ | SCK high time | 0.5 $t_{sclk}$ | | | ns |
| $t_{sclkl}$ | SCK high low | 0.5 $t_{sclk}$ | | | ns |
| $t_{sssetup}$ | SS setup time | 40 | | | ns |
| $t_{sshold}$ | SS hold time | 20 | | | ns |

**Figure 7. SPI clocking scheme**



## 4.9 $I^2C$ Timing

**Figure 8. $I^2C$ Timing**

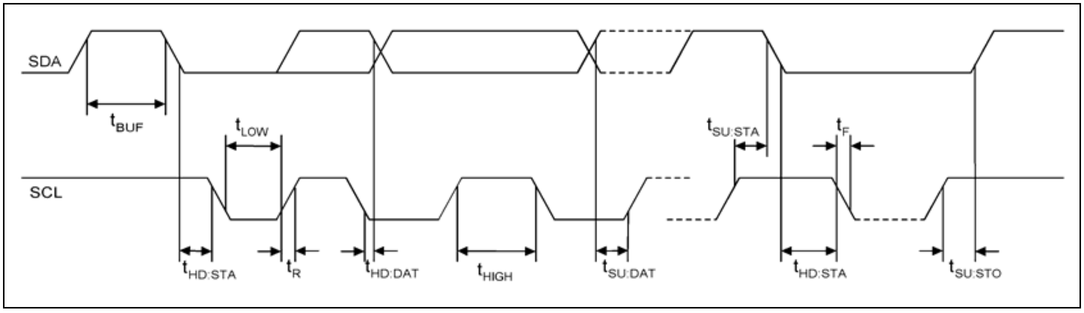


**Table 15. $I^2C$ Timing**

| Symbol | Parameter | Test condition | Standard mode $I^2C$ bus | | Fast mode $I^2C$ bus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $F_{SCL}$ | SCLI clock frequency | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | Bus free between a STOP and Start Condition | | 4.7 | – | 1.3 | – | ms |
| $t_{HD:STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | 4.0 | – | 0.6 | – | ms |
| $t_{LOW}$ | LOW period of the SCL clock | | 4.7 | – | 1.3 | – | ms |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 4.0 | – | 0.6 | – | ms |
| $t_{SU:STA}$ | Set-up time for a repeated start condition | | 4.7 | – | 0.6 | – | ms |
| $t_{HD:DAT}$ | DATA hold time | | 0 | – | 0 | 0.9 | ms |
| $t_R$ | Rise time of both SDA and SCL signals | Cb in pF | – | 1000 | 20+0.1Cb | 300 | ns |

### Table 15. I$^2$C Timing (continued)

| Symbol | Parameter | Test condition | Standard mode I$^2$C bus | | Fast mode I$^2$C bus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_F$ | Fall time of both SDA and SCL signals | Cb in pF | – | 300 | 20+0.1Cb | 300 | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | | 4 | – | 0.6 | – | ms |
| $t_{SU:DAT}$ | Data set-up time | | 250 | – | 100 | – | ns |
| $C_b$ | Capacitive load for each bus line | | – | 400 | – | 400 | pF |

## 4.10 DRAM/SRAM interface (EMI)

### Table 16. DRAM timing

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{acc0}$ | Fast DRAM access time | EDTM=0, 16 bit word | | 17 | | $T_{dsp}$ |
| $T_{acc0}$ | Fast DRAM access time | EDTM=0, 24 bit word | | 23 | | $T_{dsp}$ |
| $T_{acc1}$ | Slow DRAM access time | EDTM=1, 16 bit word | | 24 | | $T_{dsp}$ |
| $T_{acc1}$ | Slow DRAM access time | EDTM=1, 24 bit word | | 32 | | $T_{dsp}$ |

### Table 17. DRAM refresh period

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{ref}$ | DRAM refresh period | | 469 | | 782 | $T_{dsp}$ |

### Table 18. SRAM Timing

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{acc}$ | SRAM access time | | 2 | | 9 | $T_{dsp}$ |

## 4.11 Debug port interface

### Table 19. Debug port interface

| No. | Characteristics (Fdsp = 75MHz) | Min. | Max. | Unit |
|---|---|---|---|---|
| 1 | DBCK rise time | | 2 | ns |
| 2 | DBCK fall time | | 2 | ns |
| 3 | DBCK low | 40 | | ns |
| 4 | DBCK high | 40 | | ns |
| 5 | DBCK cycle time | 200 | | ns |
| 6 | DBRQN asserted to DBOUT (ACK) asserted | $5^*T_{DSP}$ | | ns |
| 7 | DBCK high to DBOUT valid | | 40 | ns |

**Table 19. Debug port interface (continued)**

| No. | Characteristics (Fdsp = 75MHz) | Min. | Max. | Unit |
|---|---|---|---|---|
| 8 | DBCK high to DBOUT invalid | 3 | | ns |
| 9 | DBIN valid to DBCK low (set-up) | 15 | | ns |
| 10 | DBCK low to DBIN invalid (hold) | 3 | | ns |
| | DBOUT (ACK) asserted to first DBCK high | $2^*T_{DSP}$ | | ns |
| | DBOUT (ACK) assertion width | $5^*T_{DSP} - 3$ | $5^*T_{DSP} + 7$ | ns |
| 11 | Last DBCK low of read register to first DBCK high of next command | $7^*T_{DSP} + 10$ | | ns |
| 12 | Last DBCK low to DBOUT invalid (hold) | 3 | | ns |
| | DBSEL setup to DBCK | $T_{DSP}$ | | ns |

**Figure 9. Debug port serial clock timing**

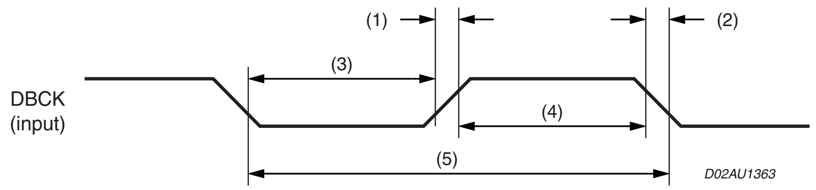


**Figure 10. Debug port acknowledge timing**

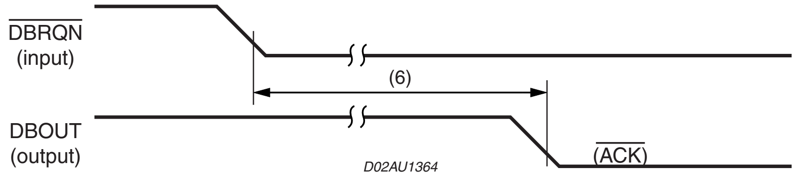
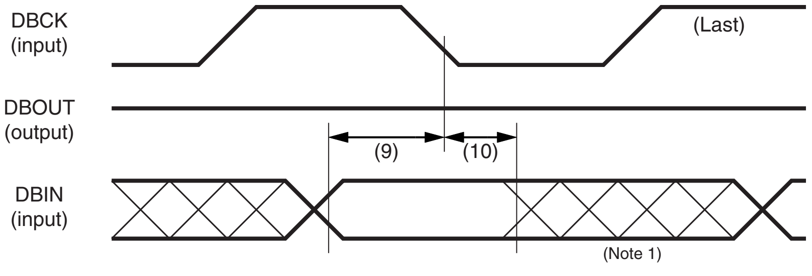
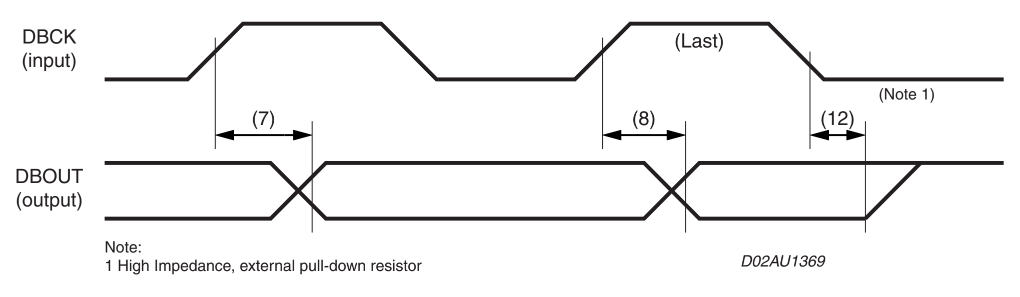


**Figure 11. Debug port data I/O to status timing**

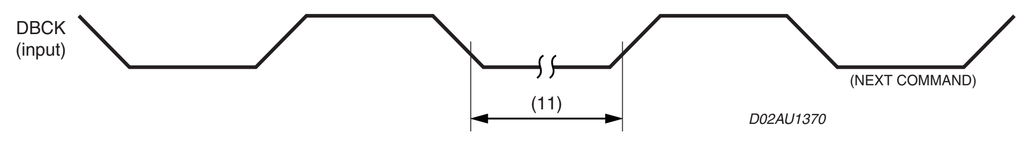


Note:
1 High Impedance, external pull-down resistor

### Figure 12. Debug port read timing



### Figure 13. Debug port DBCK next command after read register timing



### Table 20. ASRC

| Symbol | Parameters | Test conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| THD+N | Total harmonic distortion + noise, unweighted, Fsin / Fsout = 0.82 (36 kHz → 44.1 kHz) | 20 Hz–20 kHz, full scale, 16 bit inp. | | -95 | | dB |
| | | 20 Hz–20 kHz, Full scale, 20 bit inp. | | -98 | | dB |
| | | 1 kHz, full scale, 16 bit inp. | | -95 | | dB |
| | | 15 kHz, full scale, 16 bit inp. | | -95 | | dB |
| | | 1 kHz, full scale, 20 bit inp. | | -105 | | dB |
| | | 15 kHz, full scale, 20 bit inp. | | -98 | | dB |
| DR | Dynamic range, A-weighted, dithered input, Fsin / Fsout = 0.82 (36 kHz → 44.1 kHz) | 1 kHz, -60 dB, 16 bit inp. | | 98 | | dB |
| | | 1 kHz, -60 dB, 16 bit inp. | | 120 | | dB |
| IPD | Interchannel phase deviation | | | | 0 | deg |
| | Input sample rate range | No input signal decimation | 32 | | 48 | kHz |
| | Input sample rate | Input signal decimation by 2 | | 96 | | kHz |
| | Output sample rate range | | 32 | | 48 | kHz |
| **Digital filter** | | | | | | |
| $f_p$ | Passband Frequency | | | 0.4110 | | Fsin |
| $R_p$ | Passband Ripple | 0–0.4110 Fsin | -0.01 | | +0.01 | dB |
| $f_s$ | Stopband Corner Frequency | | | 0.5510 | | Fsin |
| $R_s$ | Stopband Attenuation | @ $f_s$ | | -120 | | dB |

### Table 21. Fractional-N PLL

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ | VCO output frequency | | 130 | | 310 | MHz |

### Table 22. ADC electrical characteristics - measurement bandwidth 10Hz to 20kHz
($T_{amb}$ = 25°C, ADCVDD = 3.3V, A-weighted filter.)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{in}$ | Input voltage dynamic range | Single ended mode<br>Differential mode | 0.5<br>1 | | | Vrms |
| $f_s$ | Sampling rate | Audio mode | | | 48 | kHz |
| DR(1) | Dynamic range | -60dB analog input | 84 | 88 | | dB |
| SNR | Signal to noise ratio | 1kHz; -3dB analog input | 84 | 88 | | dB |
| THD+N | Total harmonic distortion + noise | 1kHz; -3dB analog input | | -85 | -80 | dB |
| $R_i$ | Input impedance | @ fs = 44.1kHz | 45 | 80 | | kΩ |
| ICL(2) | Interchannel isolation | Full scale input @ 1kHz | | -95 | | dB |

1. The specified value is obtained by adding 60dB to THD+N measure @ full scale -60dB
2. ICL can be influenced by external anti alias filter

### Table 23. ADC electrical characteristics - measurement bandwidth 10Hz to 53kHz
($T_{amb}$ = 25°C, ADCVDD = 3.3V)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{in}$ | Input voltage dynamic range | | 0.5 | | | Vrms |
| $f_s$ | Sampling rate | FM-mode | | | 192 | kHz |
| DR (1) | Dynamic range | -60dB analog input | 80 | | | dB |
| SNR | Signal to noise ratio | 1kHz; -3dB analog input | 80 | | | dB |
| THD+N | Total harmonic distortion + noise | 1kHz; -3dB analog input | | | -80 | dB |

1. The specified value is obtained by adding 60dB to THD+N measure @ full scale -60dB

### Table 24. ADC electrical characteristics - measurement bandwidth 10Hz to 192kHz
($T_{amb}$ = 25°C, AVDD = 3.3V)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{in}$ | Input voltage dynamic range | | 0.5 | | | Vrms |
| $f_s$ | Sampling rate | FM-mode for spike and RDS | | | 384 | kHz |
| DR(1) | Dynamic range | -60dB analog input | 60 | | | dB |
| SNR | Signal to noise ratio | 1kHz; -3dB analog input | 60 | | | dB |

1. The specified value is obtained by adding 60dB to THD+N measure @ full scale -60dB

### Table 25. Level ADC electrical characteristics
($T_{amb}$ = 25°C, AVDD = 3.3V)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{in}$ | Input voltage range | | 0 | | 2.5 | V |
| THD | Total harmonic distortion | | | -57 | | dB |
| THD+N | Total harmonic distortion + noise | | | -46 | | dB |
| SNR | Signal to noise ratio | | | 46 | | dB |

### Table 26. DAC Performance

($T_{amb}$ = 25°C, DACVDD = 3.3V, measurement bandwidth 10Hz to 20kHz)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| THD+N | Total harmonic distortion + noise | 1kHz; -1dBFS, flat | | -90 | | dB |
| THD | Total harmonic distortion | 1kHz; -1dBFS, flat | | -90 | | dB |
| SNR | Signal to noise ratio | 1kHz;IEC61606 A-weighted RMS | | 100 | | dB |
| DR(1) | Dynamic range | 1kHz; -60dBFS;<br>IEC61606 A-weighted RMS | | 100 | | dB |
| NF(2) | Noise floor | IEC61606 A-weighted RMS | | -100 | | dBV |
| ICL | Interchannel isolation | 1kHz; 0dBFS | | -90 | | dB |
| Xtlk | Crosstalk | 1kHz; 0dBFS | | -90 | | dB |
| IGM | Interchannel gain mismatch | 1kHz; 0dBFS | | 0.1 | | dB |

1. The specified value is obtained by adding 60dB to THD+N measure @ full scale -60dB
2. With 00h input

### Table 27. FM stereo decoder (SW)

($T_{amb}$ = 25°C, ADCVDD = 3.3V, measurement bandwidth 10Hz to 20kHz, A-Weighted Filter.)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| a_ch | Channel separation | | | >40 | | dB |
| (THD+N) | Total harmonic distortion | -3dB analog input | | -80 | | dB |
| SNR | Signal to noise ratio | 1kHz; -3dB analog input; mono | | 86 | | dB |

# 5 Functional description

The TDA7505 is broken up into three distinct blocks. One block contains the two DSP Cores and their associated peripherals. The second contains the analog modules ADC with input multiplexer and level adjust and the DAC. The third module contains the RDS processing: filter, demodulator, decoder with error correction and the $I^2C$/SPI interface with data buffer and interrupts output.

## 5.1 24-bit DSP core

The two DSP cores are used to process the audio and FM/AM data, coming from the ADC, or any kind of digital data coming via SPDIF or SAI. After the digital signal processing these data are sent to the DAC for analog conversion. Functions such as volume, tone, balance, and fader control, as well as spatial enhancement and general purpose signal processing may be performed by the DSP0. When FM/AM mode is selected, DSP1 is fully devoted to AM/FM processing. Nevertheless it can be used for any kind of different application, when a different input source is selected. Some capabilities of the DSPs are listed below:

- Single cycle multiply and accumulate with convergent rounding and condition code generation
- 2 x 56-bit Accumulators
- Double precision multiply
- Scaling and saturation arithmetic
- 48-bit or 2 x 24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- Repeat instruction and zero overhead DO loops
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations, also Jump on bit test
- 4 pin serial debug interface
- Debug access to all internal registers, buses and memory locations
- 5 word deep program address history FIFO
- Hardware and software breakpoints for both program and data memory accesses
- Debug Single stepping, Instruction injection and Disassembly of program memory

## 5.2 DSP peripherals

There are a number of peripherals that are tightly coupled to the two DSP Cores. Some of the peripherals are connected to DSP 0 others are connected to DSP 1.

- 4k x 24-Bit Program RAM for DSP0
- 16k x 24-Bit mask programmable Program ROM for DSP0
- 4k x 24-Bit X-Data RAM for DSP0
- 4k x 24-Bit Y-Data RAM for DSP0
- 4k x 24-Bit Program RAM for DSP1
- 16k x 24-Bit mask programmable Program ROM for DSP1
- 4k x 24-Bit X-Data RAM for DSP1
- 4k x 24-Bit mask programmable X-Data ROM for DSP1
- 4k x 24-Bit Y-Data RAM for DSP1
- 6 channel Serial Audio Interface (SAI)
- 2 channel SPDIF receiver with sampling rate conversion
- I$^2$C and SPI interfaces
- XCHG Interface for DSP to DSP communication
- External Memory Interface (DRAM/SRAM) for time-delay and traffic information
- Debug Port for both DSP´s
- General-purpose Input/Output lines
- Asynchronous Sample Rate Converter
- SINCOS co-processor
- PLL Clock Oscillator
- ADC´s, ADC input multiplexer and DAC´s (see *Section 5.2.12: CODEC on page 32*)

### 5.2.1 Data and program memories

Both DSP0 and DSP1 have data and program memories attached to them. Each memory type is described below:

#### X-RAM

This is a 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be written to and read from the Data ALU of the DSP core.

#### X-ROM

This is a 24-Bit Single Port mask programmable ROM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be read from the Data ALU of the DSP core.

#### Y-RAM

This is a 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit address, YABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit Data, YDBx(23:0), is written to and read from the Data ALU of the DSP core.

### Program RAM

This is a 24-Bit Single Port SRAM used for storing and executing program code. The 16-Bit PRAM Address, PABx(15:0) is generated by the Program Address Generator of the DSP core for Instruction Fetching, and by the AGU in the case of the Move Program Memory (MOVEM) Instruction. The 24-Bit PRAM Data (Program Code), PDBx(23:0), can only be written to using the MOVEM instruction. During instruction fetching the PDBx Bus is routed to the Program Decode Controller of the DSP core for instruction decoding.

### Program ROM

This is a 24-Bit Single Port mask programmable ROM used for storing and executing program code. Additionally the boot loader SW is placed here. Essentially this consists of reading the data via I2C, SPI or EMI interface and store it in PRAM, XRAM and YRAM. The 16-Bit PROM Address, PABx(15:0) is generated by the Program Address Generator of the DSP core for Instruction Fetching, and by the AGU in the case of the Move Program Memory (MOVEM) Instruction. The 24-Bit PROM Data (Program Code), PDBx(23:0), can only be read but not written. During instruction fetching the PDBx Bus is routed to the Program Decode Controller of the DSP core for instruction decoding.

## 5.2.2 Serial audio interface (SAI)

The SAI is used to deliver digital audio to the device from an external source. Once processed by the device, either it can be returned through this interface or sent to the DAC for D/A conversion. The features of the SAI are listed below:

- 3 Synchronized Stereo Data Transmission Lines
- 3 Synchronized Stereo Data Reception Lines
- Master and Slave operating mode: clock lines can be both master and slave.
- Receive and Transmit Data Registers have two locations to hold left and right data.

## 5.2.3 Serial peripheral interface (SPI)

The DSP core requires a serial interface to receive commands and data over the LAN. During an SPI transfer, data are transmitted and received simultaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device.

When an SPI transfer occurs an 8-bit word is shifted out through one data pin while another 8-bit word is simultaneously shifted in through a second data pin. The central elements in the SPI system are the shift register and the read data buffer. The system is single buffered in the transfer direction and has a 10 word buffer in the receive direction (only master SPI; the display SPI is single word buffered only).

## 5.2.4 Sony/Phillips digital interface (S/PDIF)

The S/PDIF receiver is a serial digital audio interface. It receives and decodes serial audio data according to one of the following standards: AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 in a frequency range from 32kHz up to 96kHz. The transfer protocol provides two audio data channels.

There is a direct output connected to Asynchronous Sample Rate Converter. Left and right 20 bit audio-channels and sample clock are provided.

### 5.2.5 I$^2$C interface

The inter Integrated Circuit bus is a single bidirectional two-wire bus used for efficient inter IC control. The device is compliant with the I$^2$C specification including the highs peed (400 kHz) mode.

Every component hooked up to the I$^2$C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

The device may act as master or as slave.

#### XCHG interface (DSP to DSP exchange interface)

The Exchange Interface peripheral provides bidirectional communication between DSP0 and DSP1. Both 24 bit word data and four bit Flag data can be exchanged. A FIFO is utilized for received data. It minimizes the number of times an Exchange Interrupt Service Routine would have to be called if multi-word blocks of data were to be received. The Transmit FIFO is in effect the Receive FIFO of the other DSP and is written directly by the transmitting DSP. The features of the XCHG are listed below:

- 10 Word XCHG FIFO on DSP0 to transfer data to DSP1
- 24 Word XCHG FIFO on DSP1 to transfer data to DSP0
- Four Flags for each XCHG for DSP to DSP signaling
- Condition flags can optionally trigger interrupts on both DSP´s

### 5.2.6 DRAM/SRAM interface (DEMI)

The External DRAM/SRAM Interface is viewed as a memory mapped peripheral of both DSP cores. Data transfers are performed by moving data into/from data registers. The control is exercised by polling status flags in the control/status register or by servicing interrupts. This can be done by both DSP cores.

The features of the DEMI (Dual core Extended Memory Interface) are listed below:

- Data bus width fixed at 4 bits for DRAM and 8 bits for SRAM
- Data word length 16 or 24 bits for DRAM
- Data word length 8 or 16 or 24 bits for SRAM
- 13 DRAM address lines means $2^{26}$ = 256M bit addressable DRAM
- Refresh rate for DRAM can be chosen among eight divider factors
- SRAM relative addressing mode; $2^{22}$ = 32M bit addressable SRAM
- Four SRAM Timing choices
- Two Read Offset Registers

### 5.2.7 Debug interface

A multiplexed Debug Port is available for the DSP Cores. The debug logic is contained in the core design of the DSP. The features of the Debug Port are listed below:

- Breakpoint Logic
- Trace Logic
- Single stepping
- Instruction Injection
- Program Disassembly

### 5.2.8 General purpose input/output

The DSP requires a set of external general purpose input/output lines, and a reset line. These signals are used by external devices to signal events to the DSP. The GPIO lines are implemented as DSP 's peripherals. The GPIO lines are grouped in Port A, connected to DSP 0, and Port B, connected to DSP1.

### 5.2.9 Asynchronous sample rate converter

The ASRC, embedded in the device, offers a fully digital stereo asynchronous sample rate conversion of digital audio sources to the device's internal sample frequency. This solves the problem of mixing audio sources with different sample rates.

The ASRC is able to do both up- and down-sampling. There is no need to explicitly program the input and output sample rates, as the ASRC solves this problem with an automatic Digital Ratio Locked Loop.

In case of down sampling, an internal low pass filter limits the bandwidth. Thus any down folding products are avoided.

The ASRC is intended for applications up to 20 bit input word width. Digital Audio Sources can be applied in general Serial Audio Interface format (3 wires) as well as in AES/EBU, IEC 958, S/PDIF and EIAJ CP-340 format (1 wire).

An interface to the DSP core offers the possibility of interrupt controlled sample delivery. Furthermore, a programmable Control/Status Register inside the ASRC allows a great variety of adjustments and status information.

The ASRC is intended for applications

- up to 20 bit input and 24 bit output word width,
- 32kHz to 96kHz sample rate for input signal (SPDIF Receiver features)
- 32kHz to 48kHz sample rate for output signal.

### 5.2.10 SINCOS co-processor

The SINCOS is a cordic-based co-processor for calculation of sine and cosine without using DSP resources.

### 5.2.11 PLL clock oscillator

The PLL Clock Oscillator can accept an external clock at CLKIN or it can be configured to run with an internal oscillator when a crystal is connected across pins XTI & XTO. There is an input divide block IDF (1 -> 32) at the XTI clock input and a multiply block MF (9 -> 128) in the PLL loop. Hence the PLL can multiply the external input clock by a ratio MF/IDF to generate the internal clock. This allows the internal clock to be within 1 MHz of any desired frequency even when XTI is much greater than 1 MHz. It is recommended that the input clock is not divided down to less than 1 MHz as this reduces the Phase Detector's update rate.

The clocks to the DSP can be selected to be either the VCO output divided by 2 to 16, or be driven by the XTI pin directly.

The crystal oscillator and the PLL will be gated off when entering the power-down mode (by setting a register on DSP0).

### 5.2.12 CODEC

The CODEC is composed of four plus one A/D mono converters and three D/A stereo converters.

Two channels of the ADC can operate both in audio mode and in FM mode. When in audio mode, it converts the audio bandwidth from 20Hz to 20KHz. The A to D is a third order Sigma-Delta converter with 20-bit resolution. When in FM mode, the converted bandwidth is up to 192KHz.

Additionally a lower resolution A to D converter is implemented. It is used to convert the level signal of the tuner. Alternatively it may be used to convert voice signals.

The DAC is a second order multi bits Sigma-Delta converter accepting 24 bits input data. All the reference voltages are generated inside the chip but they have to be decoupled with external capacitors.

### 5.2.13 Radio data system (RDS)

The RDS block is a hardware cell able to deliver the RDS frames through a dedicated serial interface. An RDS quality signal is also available. This block needs to be initialized at reset by the DSP, after that it works in background and does not need any further DSP support. RDS is made of 57kHz filter, demodulator, decoder with error correction and an I$^2$C/SPI programmable interface with data buffer and interrupt output.

Due to its own interface, it may be considered as an independent function. Thus the module has a separate RDS I$^2$C device address as well as a separate chip select line for the RDS SPI. Only the pins are shared with the DSP interfaces.

### 5.2.14 Clock scheme

Due to the programmable PLL oscillator, the clock scheme is very flexible. The customer may choose the clock frequency according to the application needs. However one should take into account several constraints:

- The RDS module needs a crystal frequency of 8.55 MHz or alternative an external 74.1MHz Oscillator. However the PLL may be supplied by an external clock reference and the crystal in parallel may drive the RDS module.
- The CODEC (A/D and D/A) module needs a clock of 512 times the audio sample rate (Fs).
- The audio sample rate (Fs) should be close to 44.1 kHz. This allows CD quality. Higher sample rates will reduce the number of DSP clock cycles per Fs and hence will reduce the available MIPS.
- The DSP core clock frequency may not exceed 76 MHz
- In a car radio system the second and third system clock harmonics (DSP clock and CODEC clock) should be outside the radio frequency bands.

Two examples of convenient clock schemes are shown in the following table:

**Table 28. Examples of convenient clock schemes**

| | **Clock scheme** | **Alternative**(1) |
|---|---|---|
| Fxtal | 8.55 MHz | 74.1 MHz |
| Fcomp | Fxtal / 4<br>2.14 MHz | Fxtal/21<br>3.53 MHz |
| Fvco | Fcomp * 106<br>226.58 MHz | Fcomp * 64<br>225.8 MHz |
| Fdsp | Fvco / 3<br>75.53 MHz | Fvco / 3<br>75.28 MHz |
| Fcodec | Fvco / 10<br>22.66 MHz | Fvco / 10<br>22.58 MHz |
| Fs | 44.25 kHz | 44.11 kHz |

1. External clock oscillator used

# 6 Software features

A great flexibility is guaranteed by the two programmable DSP cores. A list of the main software functions, which can be implemented in the TDA7505, is enclosed hereafter:

## 6.1 AM/FM base band signal processing

- FM weak signal processing
- Integrated 19 kHz Pilot tone filter
- De-emphasis
- Stereo blend
- Variable high cut
- Flexible noise cancellation
- Flexible multipath detector
- Asynchronous demodulation allows the usage of any sample rate

## 6.2 Generic audio signal processing

- Loudness
- Bass, treble, fader control
- Volume control
- Distortion Limiting
- Premium Equalization
- Soft mute

## 6.3 TAPE signal processing

- Dolby B Noise Reduction
- Automatic Music Search

## 6.4 CD signal processing

- Dynamic Range Compression

## 6.5 Audiophile

- Parametric Equalization
- Crossover
- Channel Delays
- Center Channel Imaging Output
- Audio Noise Reduction

## 6.6 Audio decompression

- MP3 including C3 block decoder

## 6.7 Other

- Voice compression/decompression for traffic information storage
- Echo and noise canceling for mobile phone connection

## 6.8 Functional modes

The SW defines the whole functionality of the device, except RDS. Although ST is able to provide a complete set of SW, the customer may implement his own SW or may use third party SW. This allows a flexible adaptation to the application needs.

The concept allows the parallel processing of two independent audio sources. For example one source may go through the loudspeakers, whereas another source may feed a headphone. Additionally other sources like a phone or a navigation system may be mixed to the audio source. In case the 150 MIPS available are not sufficient, a co-dsp (e.g.: TDA7502) may be connected through the serial audio interface (SAI). Finally the device may be embedded into an audio bus system (e.g.: MOST).

Following table shows an example of possible modes:

**Table 29. Example of possible modes**

| Source | Comment | AM/FM mode | CD mode (digital) | CD Changer mode (analog) | Tape mode (digital) | Traffic info play mode |
|---|---|---|---|---|---|---|
| **AM/FM MPX (analog)** | DSP1 | Main source and RDS | Alternative Rear Source and RDS | Alternative Rear Source and RDS | Alternative Rear Source and RDS | Alternative Rear Source and RDS |
| **CD changer (analog)** | DSP1 | Alternative Rear Source | Alternative Rear Source | Main source | Alternative Rear Source | Alternative Rear Source |
| **Phone/Navi (analog)** | DSP0 | Summed to Main source | Summed to Main source | Summed to Main source | Summed to Main source | Summed to Main source |
| **CD/CD ROM audio/MP3 (digital SPDIF)** | DSP1 | Alternative Rear Source through SRC | Main source through SRC | Alternative Rear Source through SRC | Alternative Rear Source through SRC | Alternative Rear Source through SRC |
| **Tape via ADC (digital SAI)** | Dolby B on DSP1 | Alternative Rear Source | Alternative Rear Source | Alternative Rear Source | Main source | Alternative Rear Source |
| **DSP co-processor** | MDSP: master<br>CO-dsp: slave | Available (1) | Available(1) | Available(1) | Available(1) | Available(1) |
| **Traffic info storage** | DSP0 | Background recording | Background recording | Background recording | Background recording | Main source & Background recording |
| **MOST bus** | MDSP: slave<br>Co-dsp: slave<br>MOST: master | Available(1) | Available(1) | Available(1) | Available(1) | Available(1) |

1. The total number of SAI channels is six. They must be split between MOST, Co-DSP and the external ADC for tape. In case of MOST, the DSP clock must be synchronized to the MOST bus.

*Note: The main source (blue) may run in parallel with one of the alternative rear sources (yellow). Phone/Navi, DSP Co-processor, traffic info storage and MOST (green) are available in parallel to all modes.*

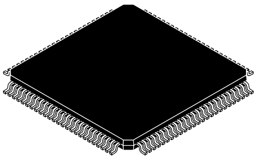
# 7 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

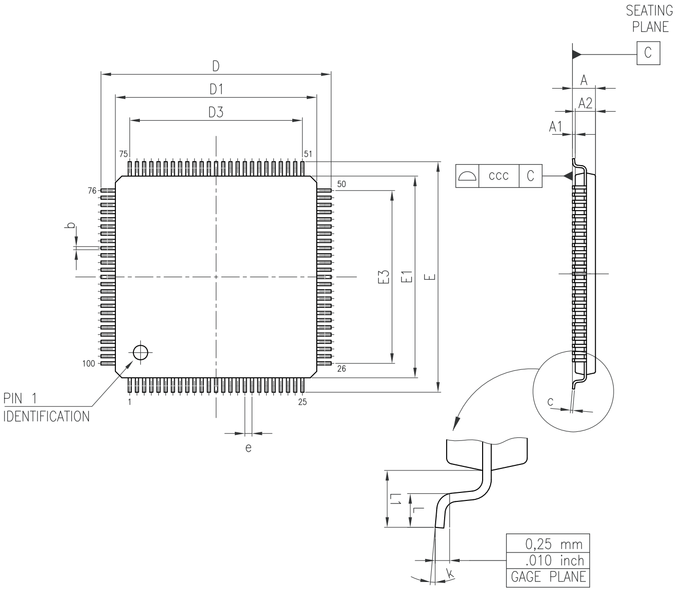
**Figure 14. LQFP100 (14x14x1.4mm) mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | **MIN.** | **TYP.** | **MAX.** | **MIN.** | **TYP.** | **MAX.** |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.000 | | | 0.4724 | |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | | 12.000 | | | 0.4724 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| K | 0° (min.), 3.5° (typ.), 7° (max.) | | | | | |
| ccc | | | 0.080 | | | 0.003 |

**OUTLINE AND MECHANICAL DATA**



**LQFP100 (14x14x1.40mm)**
**L**ow profile **Q**uad **F**lat **P**ackage



0086901 D

# 8 Revision history

Table 30. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 23-Oct-2007 | 1 | Initial release. |
| 24-Sep-2013 | 2 | Updated disclaimer. |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**