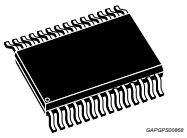
TDA7720B

3 band car audio processor

Datasheet - production data



TSSOP28

Features

- Input multiplexer
  - QD1: quasi-differential stereo input
  - QD2: quasi-differential stereo input
  - SE1: stereo single-ended input
  - SE2: stereo single-ended input
  - SE3: stereo single-ended input
- Loudness
  - 2nd order frequency response
  - Programmable center frequency (400 Hz / 800 Hz / 2400 Hz)
  - 15 dB with 1 dB steps
  - Selectable high frequency boost
  - Selectable flat-mode (constant attenuation)
- Volume
  - +23 dB to -63 dB with 1 dB step resolution
  - Soft-step control with programmable blend times
- Bass
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (60 Hz / 80 Hz / 100 Hz / 200 Hz)
  - Q programmable 1.0/1.25/1.5/2.0
  - DC gain programmable
  - -15 to 15 dB range with 1 dB resolution
- Middle
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (500 Hz / 1 kHz / 1.5 kHz / 2.5 kHz)
  - Q programmable 0.75/1.0/1.25
  - -15 to 15 dB range with 1 dB resolution
- Treble
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (10 kHz / 12.5 kHz / 15 kHz / 17.5 kHz)
  - -15 to 15 dB range with 1 dB resolution
- High-pass
  - 2nd order frequency response
  - Center frequency programmable in 3 steps (100 Hz / 120 Hz / 150 Hz)
- Subwoofer
  - 2nd order low pass filter
  - Programmable cut off frequency
  - (55 Hz / 85 Hz / 120 Hz / 160 Hz)
  - 2 independent soft-step level control, +15 dB to -79 dB with 1 dB steps
- Speaker
  - 6 independent soft-step speaker controls
  - +15 dB to -79 dB with 1 dB steps
  - Two selectable output DC level
  - Direct mute
- Mute functions
  - Direct mute
  - Digitally controlled soft-mute with 4 programmable mute-times
  - (0.48 ms / 0.96 ms / 8 ms / 16 ms)
- Offset detection
  - Offset voltage detection circuit for on-board power amplifier failure diagnosis

Description

The TDA7720B is a high performance signal processor specifically designed for car radio applications. The device includes a high performance audio processor with fully integrated audio filters and new soft-step architecture. The digital control allows programming in a wide range of filter characteristics.

Table 1. Device summary

Order code	Package	Packing
TDA7720B	TSSOP28	Tube
TDA7720BTR	TSSOP28	Tape and reel

Contents

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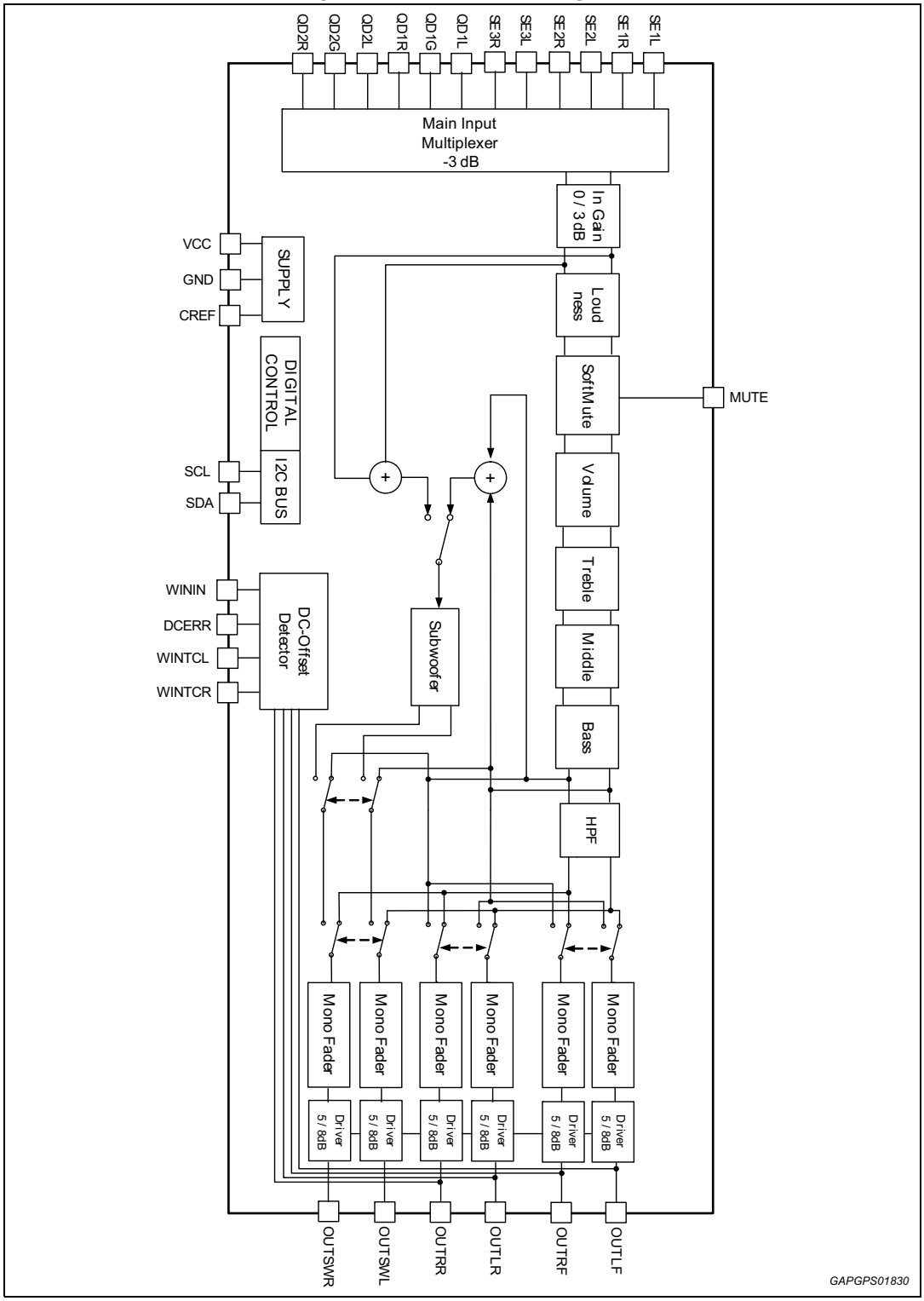
1 Block circuit diagram

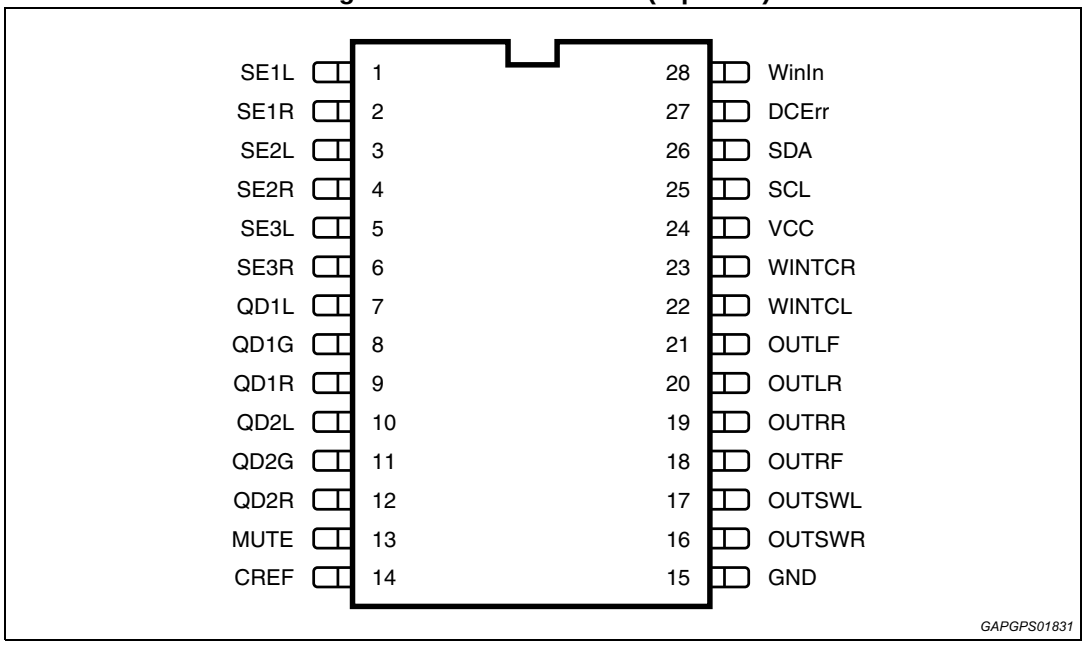
Figure 1. Block circuit diagram



2 Pins connection and description

2.1 Pins connection

Figure 2. Pins connection (top view)



2.2 Pins description

Table 2. Pins description

Pin #	Pin name	Description	I/O
1	SE1L	Single-end input left	I
2	SE1R	Single-end input right	I
3	SE2L	Single-end input left	I
4	SE2R	Single-end input right	I
5	SE3L	Single-end input left	I
6	SE3R	Single-end input right	I
7	QD1L	Quasi-differential stereo inputs left	I
8	QD1G	Quasi-differential stereo inputs common	I
9	QD1R	Quasi-differential stereo inputs right	I
10	QD2L	Quasi-differential stereo inputs left	I
11	QD2G	Quasi-differential stereo inputs common	I
12	QD2R	Quasi-differential stereo inputs right	I
13	MUTE	External mute pin	I

Table 2. Pins description (continued)

Pin #	Pin name	Description	I/O
14	CREF	Reference capacitor	O
15	GND	Ground	S
16	OUTSWR	Subwoofer right output	O
17	OUTSWL	Subwoofer left output	O
18	OUTRF	Front right output	O
19	OUTRR	Rear right output	O
20	OUTLR	Rear left output	O
21	OUTLF	Front left output	O
22	WINTCL	DC offset detector filter output left channel	O
23	WINTCR	DC offset detector filter output right channel	O
24	VCC	Supply	S
25	SCL	I^2C bus clock	I
26	SDA	I^2C bus data	I/O
27	DCERR	DC offset detector output	O
28	WinIn	DC offset detector input	I

Note: The L & R channels may be swapped as per the user's wishes making use of proper connections to the device pins, with no impact on electrical performance.
Software control has to take into account the external routing and be designed accordingly.

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\text{-}jamb}$	Thermal resistance junction-to-ambient	114	°C/W

3.1.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	13	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
V_{ESD}	ESD withstand voltage: Human body model Charged device model	 ≥ ±2000 ≥ ±250	 V V

3.2 Electrical characteristics

V_S =11.5 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; Output gain = 5 dB; Input = SE1; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
V_s	Supply voltage	-	7.5	11.5	12.5	V
I_s	Supply current	-	30	35	39	mA
Input selector						
R_{in}	Input resistance	All single ended inputs	70	100	130	kΩ
V_{CL}	Clipping level	Input gain = 0 dB, THD = 1 %	2	-	-	V_{RMS}
S_{IN}	Input separation	-	80	100	-	dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR	Common mode rejection Ratio for main source	V_{CM}=1 V_{RMS} @ 1 kHz	46	60	-	dB
		V_{CM}=1 V_{RMS} @ 10 kHz (1)	46	60	-	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Loudness control						
A_{MAX}	Max. attenuation (2)	-	14	15	16.5	dB
A_{STEP}	Step resolution (2)	-	0.5	1	1.5	dB
f_{Peak}	Peak frequency (3)	f_{P1}	-	400	-	Hz
		f_{P2}	-	800	-	Hz
		f_{P3}	-	2400	-	Hz
Volume control						
G_{MAX}	Max. gain (2)	-	21	23	25	dB
A_{MAX}	Max. attenuation (2)	-	-66	-63	-60	dB
A_{STEP}	Step resolution (2)	-	0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to +23 dB	-0.75	0	0.75	dB
		G = -20 to -63 dB	-4	0	3	dB
E_T	Tracking error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-5	0.1	5	mV
		From 0 dB to A_{MAX}	-8	0.5	8	mV
Soft-mute						
A_{MUTE}	Mute attenuation		80	100	-	dB
T_D	Delay time	T_1	0.36	0.48	0.6	ms
		T_2	0.84	0.96	1.08	ms
		T_3	7.3	7.6	8.5	ms
		T_4	14	15.3	16.8	ms
V_{TH_Low}	Low threshold for MUTE pin	(4)	-	-	0.8	V
V_{TH_High}	High threshold for MUTE pin	(4)	2.5	-	-	V
RPU	Internal pull-up resistor for MUTE pin	-	35	48	63	kΩ
VPU	Internal pull-up voltage for MUTE pin	-	3	3.3	3.6	V
Bass control						
Fc	Center frequency (3)	f_{C1}	-	60	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	200	-	Hz

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Q_{BASS}	Quality factor (3)	Q_1	-	1	-	-
		Q_2	-	1.25	-	-
		Q_3	-	1.5	-	-
		Q_4	-	2	-	-
C_{RANGE}	Control range (2)	-	14	15	16	dB
A_{STEP}	Step resolution (2)	-	0.5	1	1.5	dB
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	1	dB
		DC = on, Gain = ±14 dB	4	4.4	4.6	dB
Middle control						
C_{RANGE}	Control range (2)	-	14	15	16	dB
A_{STEP}	Step resolution (2)	-	0.5	1	1.5	dB
Fc	Center frequency (3)	f_{C1}	-	500	-	Hz
		f_{C2}	-	1	-	kHz
		f_{C3}	-	1.5	-	kHz
		f_{C4}	-	2.5	-	kHz
Q_{Middle}	Quality factor (3)	Q_1	-	0.75	-	-
		Q_2	-	1	-	-
		Q_3	-	1.25	-	-
Treble control						
C_{RANGE}	Clipping level	-	13	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
Fc	Center frequency (3)	f_{C1}	-	10	-	kHz
		f_{C2}	-	12.5	-	kHz
		f_{C3}	-	15	-	kHz
		f_{C4}	-	17.5	-	kHz
Speaker attenuators						
G_{MAX}	Max. gain (2)	-	14	15	16	dB
A_{MAX}	Max. attenuation (2)	-	-90	-79	-70	dB
A_{STEP}	Step resolution (2)	-	0.5	1	1.5	dB
A_{MUTE}	Mute attenuation	-	80	90	-	dB
E_A	Attenuation set error	G = -20 to +15 dB	-0.75	0	0.75	dB
		G = -20 to -79 dB	-10	0	10	dB
V_{DC}	DC steps	Adjacent attenuation steps	-5	0.1	5	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
HPF							
F_{HP}	High-pass corner frequency (3)	f_{HP1}		-	100	-	Hz
		f_{HP2}		-	120	-	Hz
		f_{HP3}		-	150	-	Hz
Audio outputs							
V_{CL}	Clipping level	PRE	THD = 0.5% VCC = 8.5V output level/gain = 4V/5 dB	2.5	-	-	V_{RMS}
		FRONT REAR	THD = 0.3% VCC = 8.5V output level/gain = 4V/5dB				
		PRE	THD = 0.5% VCC = 11.5V output level/gain = 5.75V/5dB	3.55	-	-	V_{RMS}
		FRONT REAR	THD = 0.3% VCC = 11.5V output level/gain = 5.75V/5dB				
R_{OUT}	Output impedance	-		-	30	50	Ω
R_L	Output load resistance	-		2	-	-	kΩ
C_L	Output load capacitor	-		-	-	10	nF
V_{DC}	Output DC level	Output level/gain = 4 V / 5 dB		3.8	4.0	4.2	V
		Output level/gain = 5.75 V / 8 dB		5.5	5.75	6	V
G_{OUT}	Output gain	Output level/gain = 4 V /5 dB		4	5	6	dB
		Output level/gain = 5.75 V / 8 dB		7	8	9	dB
Subwoofer low-pass							
f_{LP}	Low-pass corner frequency (3)	f_{LP1}		-	55	-	Hz
		f_{LP2}		-	85	-	Hz
		f_{LP3}		-	120	-	Hz
		f_{LP4}		-	160	-	Hz
DC offset detection circuit							
V_{th}	Zero comp. window size	V_1		±20	±30	±40	mV
		V_2		±30	±45	±55	mV
		V_3		±40	±60	±70	mV
		V_4		±70	±90	±100	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
τ_{sp}	Max. rejected spike length	T_1		7	11	25	µs
		T_2		14	22	45	µs
		T_3		22	33	65	µs
		T_4		28	44	80	µs
$I_{CHDCErr}$	DCErr charge current	-		3.5	5	6.5	µA
$I_{DISDCErr}$	DCErr discharge current	-		3.5	5	8	mA
V_{OutH}	DCErr high voltage	-		3.1	3.3	3.6	V
V_{OutH}	DCErr low voltage	-		0	100	300	mV
V_{TH_Low}	Low Threshold for WinIn pin	(4)		-	-	0.75	V
V_{TH_High}	High Threshold for WinIn pin	(4)		2.8	-	-	V
RPU	Internal pull-up resistor for WinIn pin	-		35	50	70	kΩ
VPU	Internal pull-up voltage for WinIn pin	-		3.1	3.3	3.5	V
General							
e_{NO}	Output noise	BW = 20 Hz to 20 kHz A-Weighted, all gain = 0dB, HPF=OFF, Input=SE/QD	Output level / gain = 4V / 5dB	-	15	30	µV
			Output level/gain=5.75V/8dB	-	21	35	µV
		BW = 20 Hz to 20 kHz A-Weighted, Output muted	Output level/gain=4V/5dB	-	9	21	µV
			Output level/gain=5.75V/8dB	-	12.5	21	µV
S/N	Signal to noise ratio	all gain = 0 dB, A-weighted; Output level/gain = 4 V / 5 dB; V_o = 2.5 V_{RMS}		98	104	-	dB
		all gain = 0dB, A-weighted; Output level/gain = 5.75 V / 8 dB; V_o = 3.55 V_{RMS}		98	104	-	dB
D	Distortion	VIN=1V_{RMS}; all gain = 0dB, HPF=OFF	Output level/gain = 4 V / 5 dB	-	0.01	0.05	%
			Output level/gain=5.75V/8dB	-	0.01	0.05	%
S_C	Channel separation left/right	-		75	90	-	dB

1. Guaranteed by design.
2. Measure performed in DC.
3. Value guaranteed by measuring correlated parameter.
4. Verified only in characterization.

4 Description of audioprocessor

4.1 Input stage

Two quasi-differential stereo input and three single-ended inputs are available.

4.1.1 Single-ended stereo input (SE1, SE2, SE3)

The input-impedance at each input is 100 kΩ and the attenuation is fixed to -3 dB for incoming signals.

4.1.2 Quasi-differential stereo Input (QD1,QD2)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 kΩ input-impedance at each input. There is -3 dB attenuation at QD input stage.

4.1.3 Fast charge

Each differential input pin features a "fast-charge" switch allowing to quickly charge any external large coupling capacitors upon power-on of the device. When the device is power-on, the “fast-charge” switches are automatically turn on, for normal operation these switches need to be released by any programming of byte_0. After that, the “fast-charge” switches can be turned on/off by setting “fast charge = on/off”.

4.2 Input gain

A 0/3 dB input gain is selectable to compensate the attenuation of input stage.

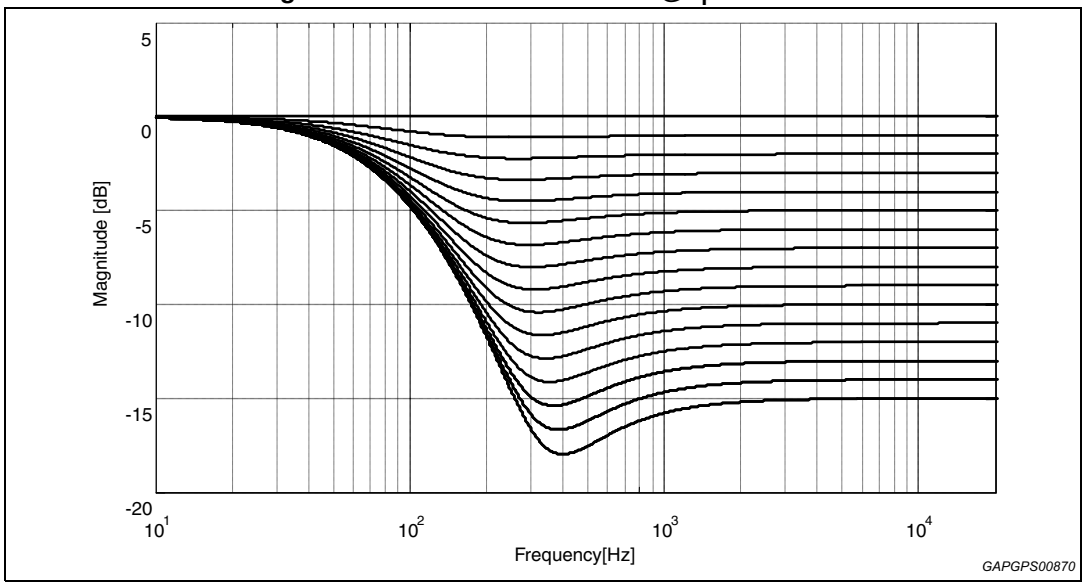
4.3 Loudness

There are four parameters programmable in the loudness stage.

4.3.1 Loudness attenuation

Figure 3 shows the attenuation as a function of frequency at f_P = 400 Hz

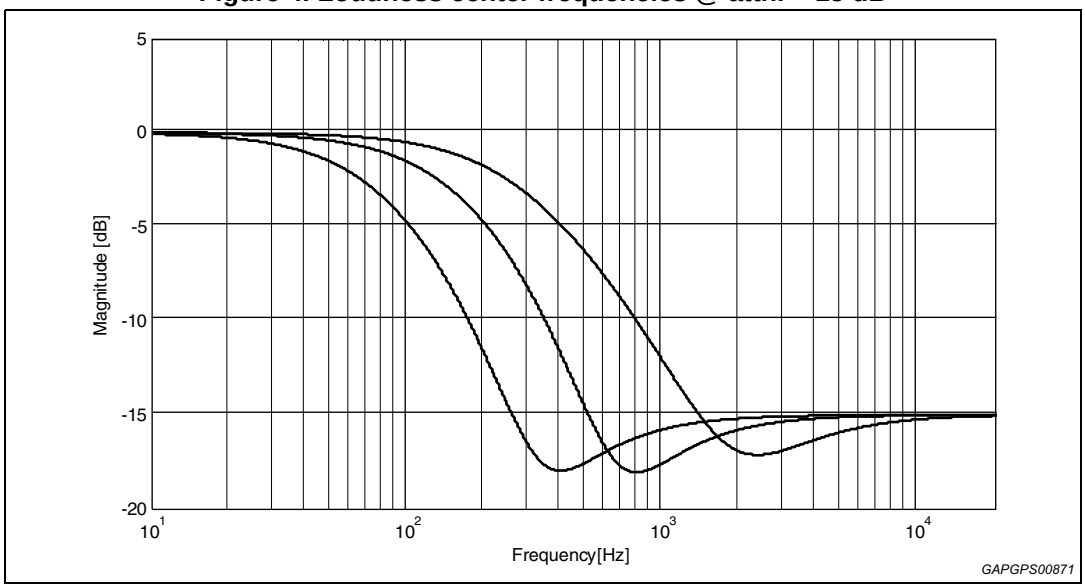
Figure 3. Loudness attenuation @ f_P = 400 Hz



4.3.2 Peak frequency

Figure 4 shows the four possible peak-frequencies at 400, 800 and 2400 Hz

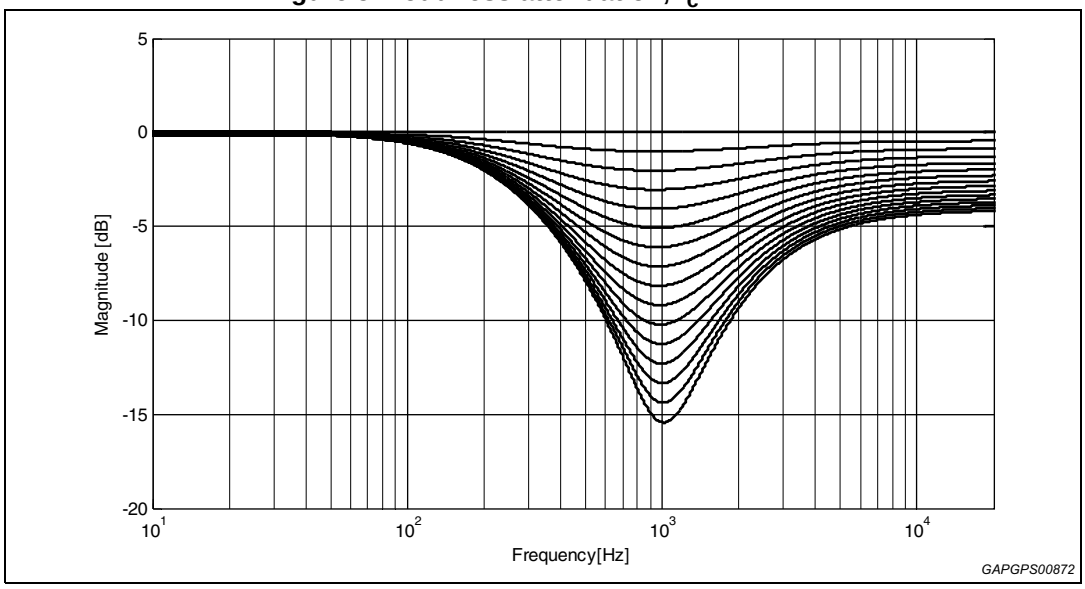
Figure 4. Loudness center frequencies @ attn. = 15 dB



4.3.3 High frequency boost

Figure 5 shows the different loudness shapes in low and high frequency boost.

Figure 5. Loudness attenuation, f_c = 2.4 kHz



4.3.4 Flat mode

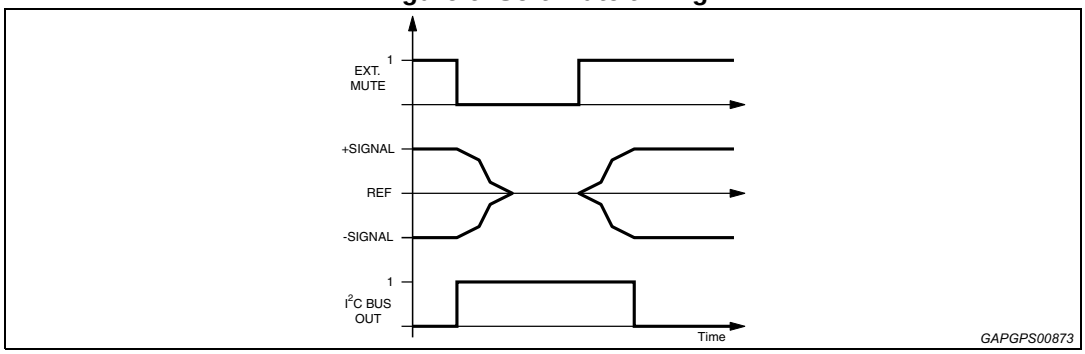
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.4 Soft-mute

The digitally controlled soft-mute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the soft-mute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 6*).

For timing purposes the bit0 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 6. Soft-mute timing



Note: Please notice that a started mute-action is always terminated and could not be interrupted by a change of the mute –signal.

4.5 Volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-offset before the volume-stage or the sudden change of the envelope of the audio signal. With the soft-step-feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5 ms or 10 ms. The soft-step control is described in detail in *Section 4.1.1*.

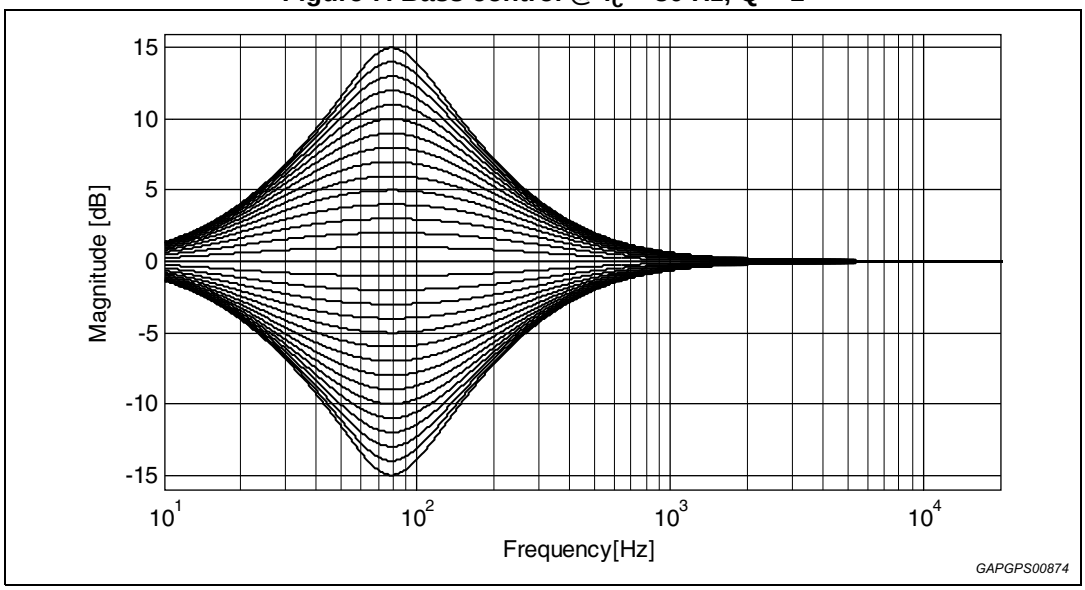
4.6 Bass

There are four parameters programmable in the bass stage.

4.6.1 Bass attenuation

Figure 7 shows the attenuation as a function of frequency at a center frequency of 80 Hz.

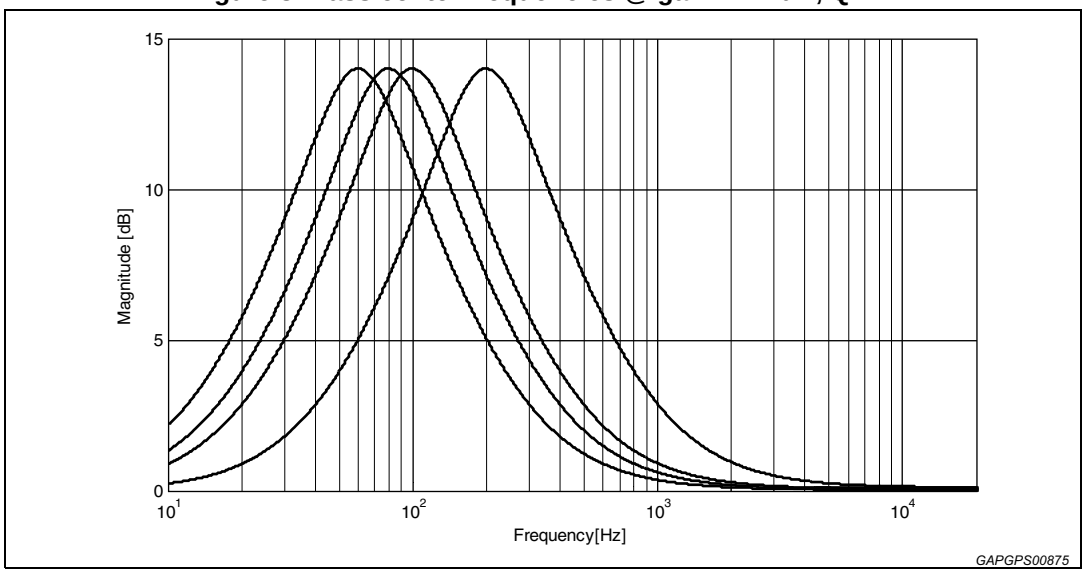
Figure 7. Bass control @ f_c = 80 Hz, Q = 1



4.6.2 Center frequency

Figure 8 shows the four possible center frequencies 60, 80, 100 and 200 Hz.

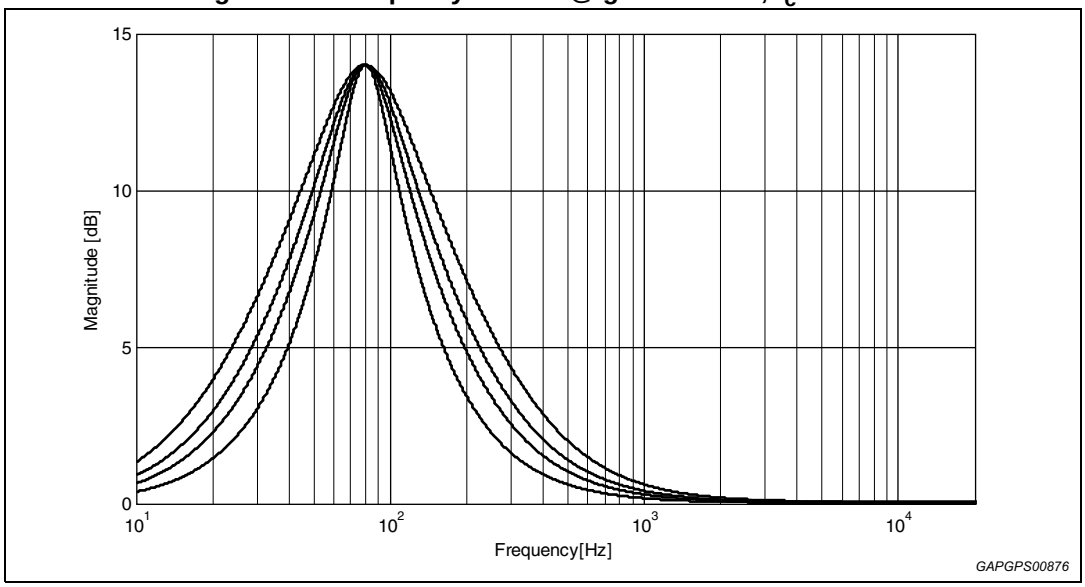
Figure 8. Bass center frequencies @ gain = 14 dB, Q = 1



4.6.3 Quality factors

Figure 9 shows the four possible quality factors 1, 1.25, 1.5 and 2.

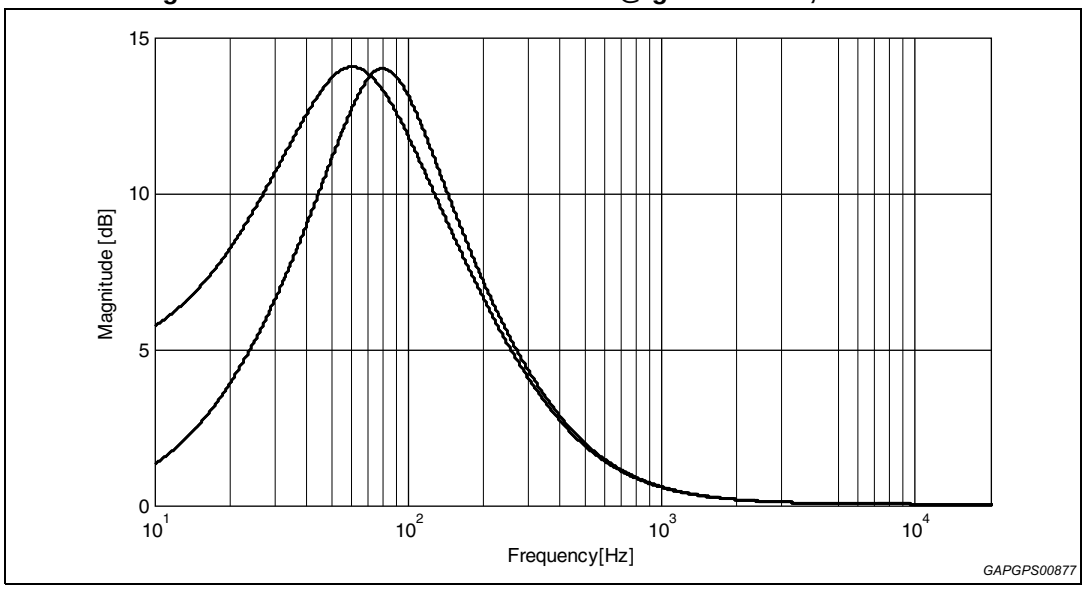
Figure 9. Bass quality factors @ gain = 14 dB, f_c = 80 Hz



4.6.4 DC mode

In this mode the DC-gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

Figure 10. Bass normal and DC mode @ gain = 14 dB, fc = 80 Hz



Note: The center frequency, Q and DC-mode can be set fully independently.

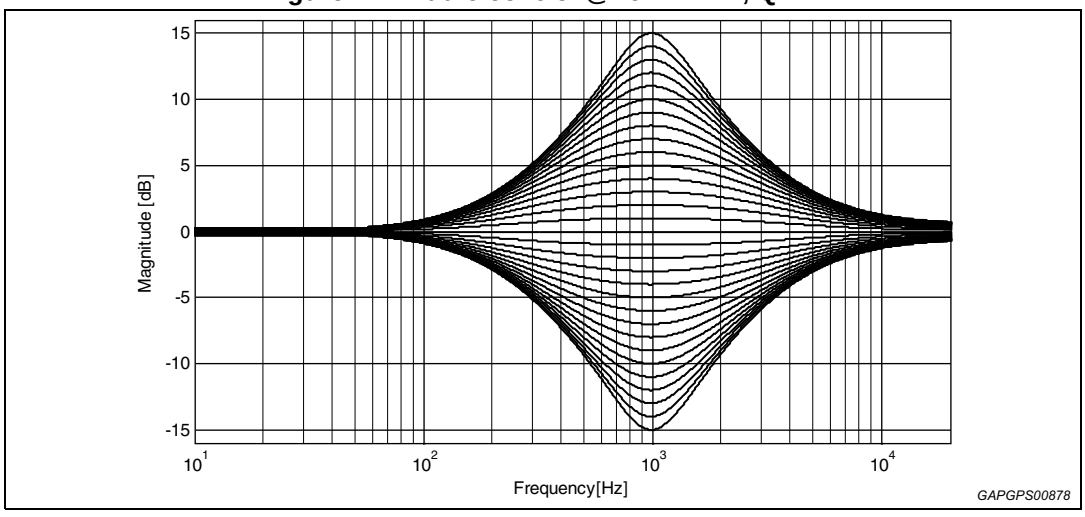
4.7 Middle

There are three parameters programmable in the middle stage.

4.7.1 Middle attenuation

Figure 11 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

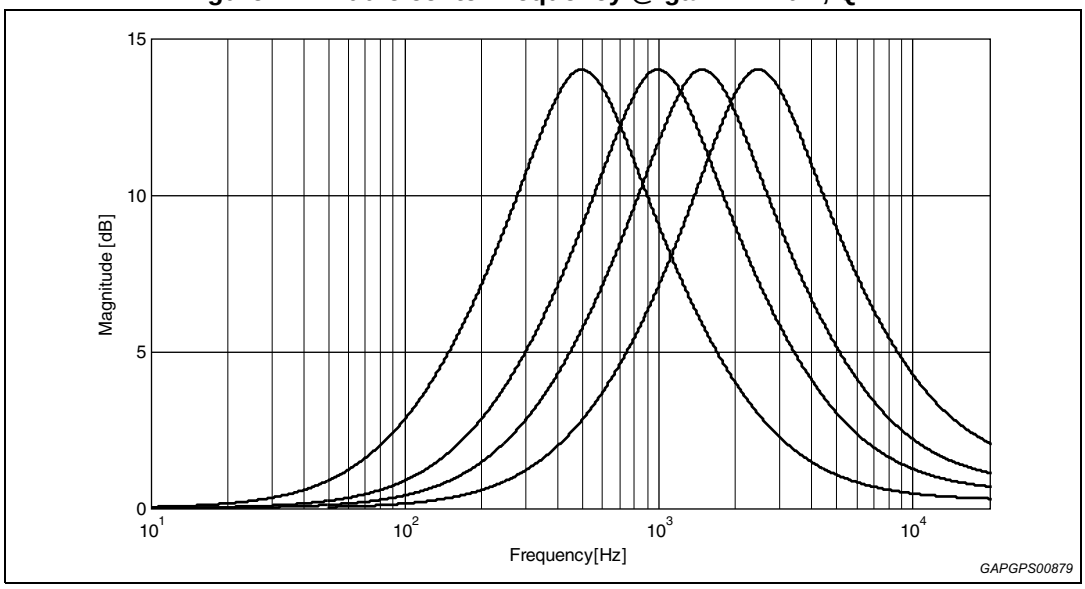
Figure 11. Middle control @ fc = 1 kHz, Q = 1



4.7.2 Middle center frequency

Figure 12 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

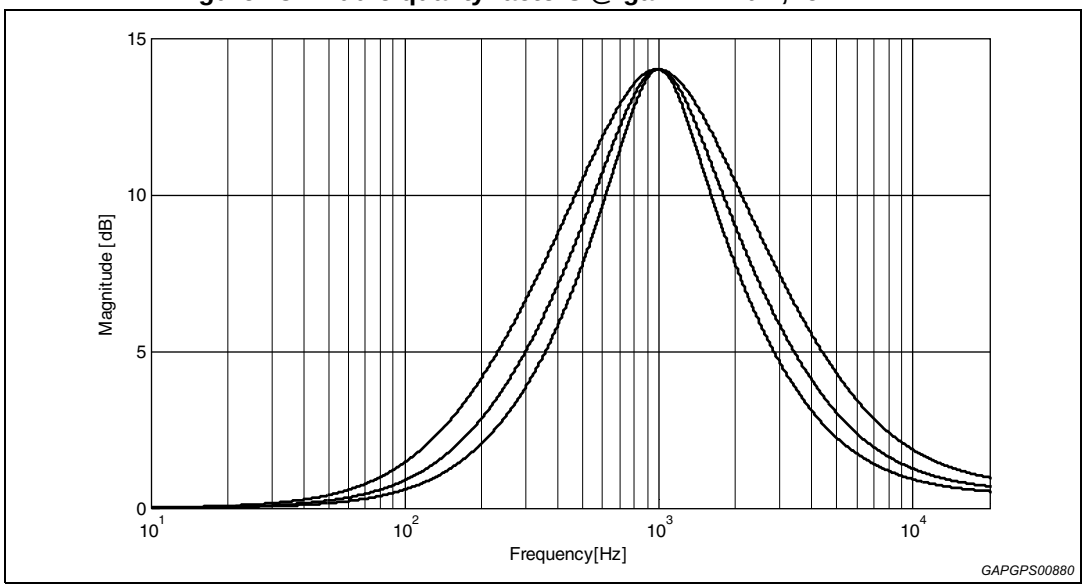
Figure 12. Middle center frequency @ gain = 14 dB, Q = 1



4.7.3 Quality factors

Figure 13 shows the three possible quality factors 0.75, 1 and 1.25.

Figure 13. Middle quality factors @ gain = 14 dB, fc =1 kHz



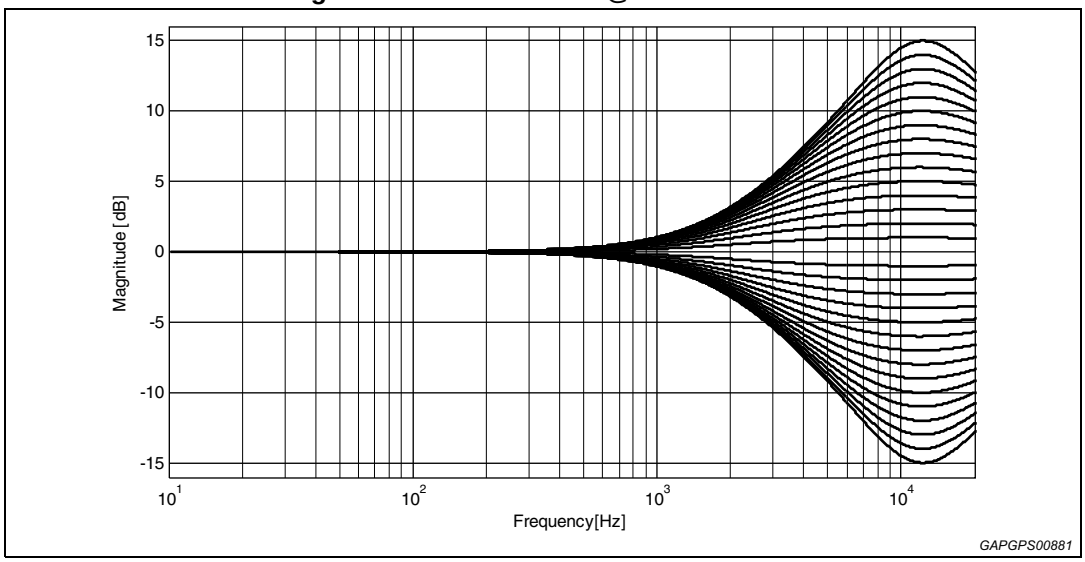
4.8 Treble

There are two parameters programmable in the treble stage.

4.8.1 Treble attenuation

Figure 14 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

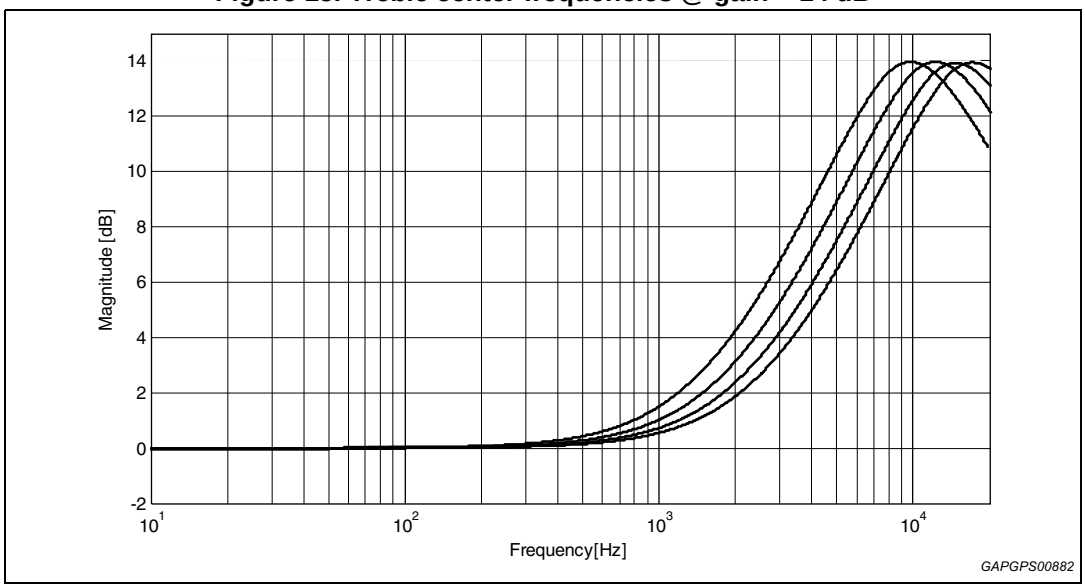
Figure 14. Treble control @ fc = 17.5 kHz



4.8.2 Center frequency

Figure 15 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5 kHz.

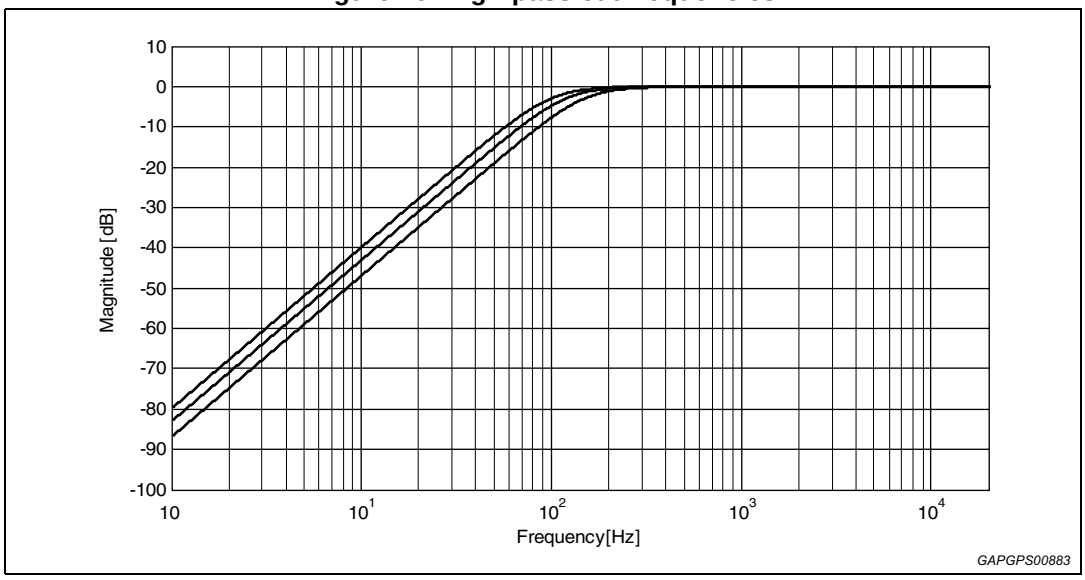
Figure 15. Treble center frequencies @ gain = 14 dB



4.9 High-pass filter

The high-pass filter has 2 order filter characteristics with programmable cut-off frequency (100 / 120 / 150 Hz

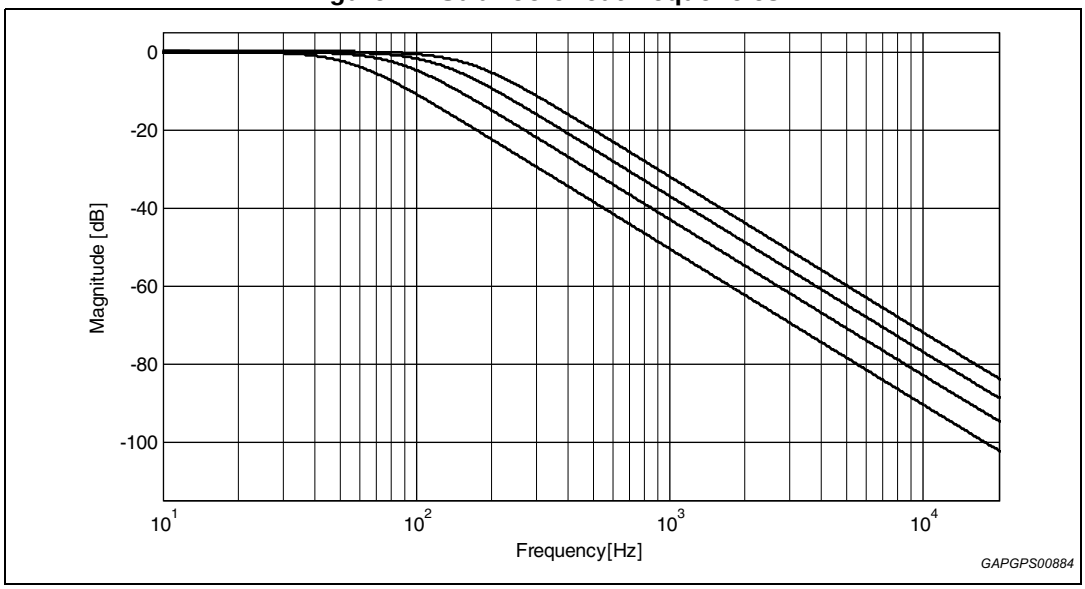
Figure 16. High-pass cut frequencies



4.10 Subwoofer filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (55 Hz / 85 Hz/ 120 Hz/ 160 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input mux.

Figure 17. Subwoofer cut frequencies



4.11 Soft-step control

In this device, the soft-step function is available for volume, speaker, loudness, treble, middle and bass block. With soft-step function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the soft-step function is controlled by soft-step on/off control bit in the control table. The soft-step transient time selection (5 ms or 10 ms) is common for all blocks and it is controlled by soft-step time control bit. The soft-step operation of all blocks has a common centralized control. In this case, a new soft-step operation will not be started before the completion of previous soft-step.

There are two different modes to activate the soft-step operation. The soft-step operation can be started right after I^2C data sending, or the soft-step can be activated in parallel after data sending of several different blocks. The two modes are controlled by the ‘act bit’ (it is normally bit7 of the byte.) of each byte. When act bit is ‘0’, which means action, the soft-step is activated right after the date byte is sent. When the act bit is ‘1’, which means wait, the block goes to wait for soft-step status. In this case, the block will wait for some other block to activate the operation. The soft-step operation of all blocks in wait status will be done together with the block which activate the soft-step. With this mode, all specific blocks can do the soft-step in parallel. This avoids waiting when the soft-step is operated one by one. Be noticed that if a block is set to ‘gain1’ with act bit =1, later this block is set to ‘gain2’ with act bit=0, in this case the block will do a soft-step from present gain to ‘gain2’ but not from present gain to ‘gain1’ then to ‘gain2’.

Chip Addr	Sub Addr	0xxxxxxx

|← Soft-step start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	.....	0xxxxxxx

|← Soft-step start here for all

4.12 DC offset detector

Using the DC offset detection circuit (*Figure 18*) an offset voltage difference between the audio power amplifier and the APR's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the APR. The WinIn-input has an 50 kΩ internal pull-up resistor connected to 3.3 V. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin are implemented, with external capacitors introducing the same delay $\tau = 22.5\ k\Omega * C_{ext}$ as the AC-coupling between the APR and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

See *Electrical characteristics on page 9*.

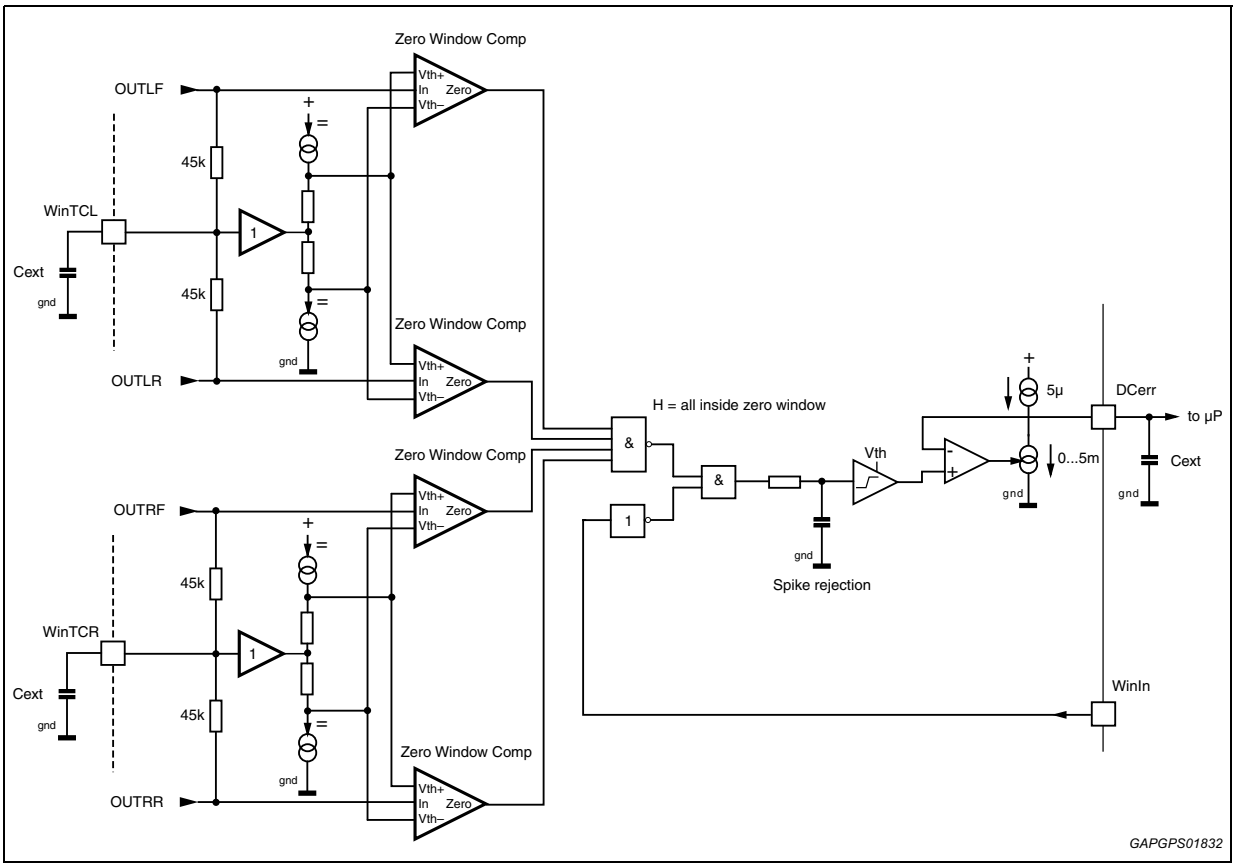
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) Front and rear outputs are inside zero crossing windows.

b) The input voltage V_{winin} is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

Figure 18. DC offset detection circuit (simplified)



4.13 Output stage

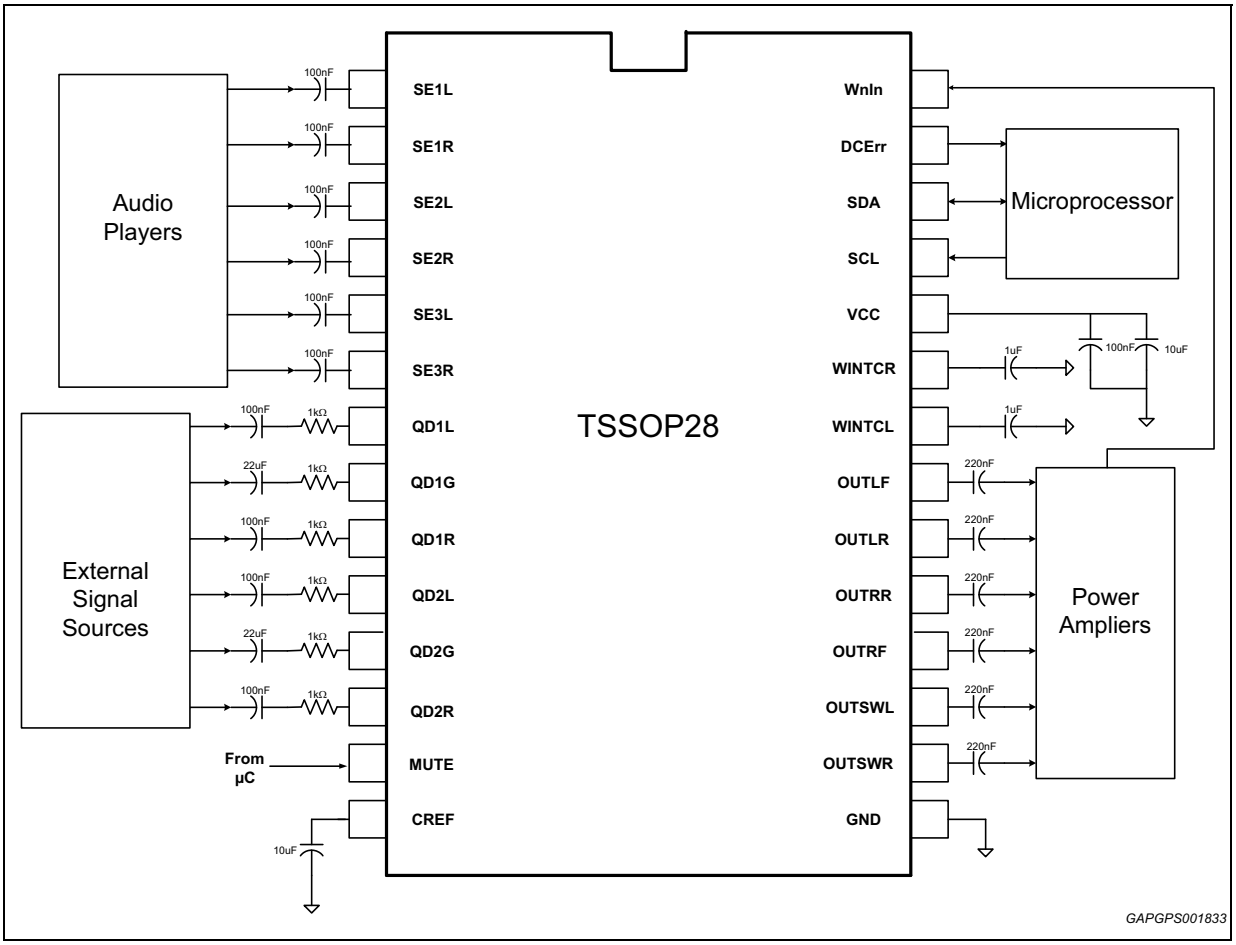
The output gain and output DC voltage is configurable by I^2C to fit different application. The configuration is as following:

- AC Gain = 5 dB, DC level = 4 V
- AC Gain = 8 dB, DC level = 5.75 V

4.14 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the QD2G pin. In this mode, the input resistance of 100 kOhm is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

Figure 19. Test circuit



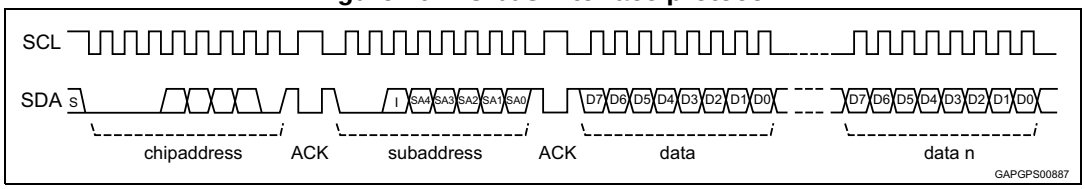
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400kbits/s
- 3.3 V logic compatible

Figure 20. I²C bus interface protocol



S = Start

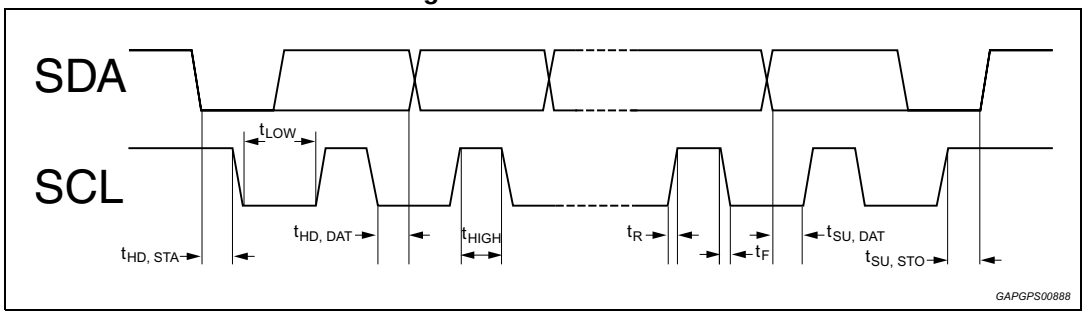
ACK = Acknowledge

5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	-	400	kHz
V_{IH}	High level input voltage	2.4	-	V
V_{IL}	Low level input voltage	-	0.8	V
$t_{HD,STA}$	Hold time for START	0.6	-	µs
$t_{SU,STO}$	Setup time for STOP	0.6	-	µs
t_{LOW}	Low period for SCL clock	1.3	-	µs
t_{HIGH}	High period for SCL clock	0.6	-	µs
t_F	Fall time for SCL/SDA	-	300	ns
t_R	Rise time for SCL/SDA	-	300	ns
$t_{HD,DAT}$	Data hold time	0	-	ns
$t_{SU,DAT}$	Data setup time	100	-	ns

Figure 21. I²C bus data



5.2.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive mode (Chip can be programmed by µP)

"1" -> Transmission mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.2.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	BZ	SM	ACK	P	

SM = Soft-mute activated for main channel

BZ = Soft-step busy (‘0’ = Busy)

X = Not used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in following tables.

Table 7. Subaddress (receive mode)

MSB							LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0	
0 1	-	-	-	-	-	-	-	**Testing mode** Off On
-	x	-	-	-	-	-	-	**Not used**
-	-	0 1	-	-	-	-	-	**Auto increment mode** Off On
-	-	-	0	0	0	0	0	Main selector
-	-	-	0	0	0	0	1	Output DC level / highpass
-	-	-	0	0	0	1	0	Not used
-	-	-	0	0	0	1	1	Not used
-	-	-	0	0	1	0	0	Soft-mute / others
-	-	-	0	0	1	0	1	Soft-step I
-	-	-	0	0	1	1	0	Soft-step II / DC-detector
-	-	-	0	0	1	1	1	Loudness
-	-	-	0	1	0	0	0	Volume / output gain
-	-	-	0	1	0	0	1	Treble
-	-	-	0	1	0	1	0	Middle
-	-	-	0	1	0	1	1	Bass
-	-	-	0	1	1	0	0	Subwoofer / middle / bass
-	-	-	0	1	1	0	1	Speaker attenuator left front
-	-	-	0	1	1	1	0	Speaker attenuator right front
-	-	-	0	1	1	1	1	Speaker attenuator left rear
-	-	-	1	0	0	0	0	Speaker attenuator right rear
-	-	-	1	0	0	0	1	Subwoofer attenuator left
-	-	-	1	0	0	1	0	Subwoofer attenuator right
-	-	-	1	0	0	1	1	Testing audio processor 1
-	-	-	1	0	1	0	0	Testing audio processor 2
-	-	-	1	0	1	0	1	Testing audio processor 3

5.3 Data byte specification

Table 8. Main selector (0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	**Main source selector** SE1 SE3 QD1 QD2 SE2 Mute Mute Mute
-	-	-	-	x	-	-	-	**Not used**
-	-	-	0 1	-	-	-	-	Main source input gain select 0 dB 3 dB
-	-	0 1	-	-	-	-	-	**Subwoofer flat** Off On
-	0 1	-	-	-	-	-	-	**Subwoofer input source** Input mux Bass output
x	-	-	-	-	-	-	-	**Not used**

Table 9. Output DC level / highpass (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	-	**Not used**
-	-	-	-	-	-	0 1	-	**Output DC level** 4 V (AC Gain = 5 dB) 5.75 V (AC Gain = 8 dB)
-	-	-	-	0 0 1	0 1 x	-	-	**High-pass frequency** 100 Hz 120 Hz 150 Hz
-	-	-	0 1	-	-	-	-	**High-pass enable** Off (bypass) On
x	x	x	-	-	-	-	-	**Not used**

Table 10. Soft-mute / others (4)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Soft-mute** On Off
-	-	-	-	-	-	0 1	-	**Pin influence for mute** Pin and IIC IIC
-	-	-	-	0 0 1 1	0 1 0 1	-	-	**Soft-mute time** 0.48 ms 0.96 ms 7.68 ms 15.36 ms
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Speaker-Ls/Rs input selection (OUTSWL & OUTSWR)** High Pass filter Subwoofer filter High Pass filter Bass filter
-	0 1	-	-	-	-	-	-	**Fast charge** On Off
0 1	-	-	-	-	-	-	-	**Anti-alias filter** On Off (bypass)

Table 11. Soft-step I (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Loudness soft-step** On Off
-	-	-	-	-	-	0 1	-	**Volume soft-step** On Off
-	-	-	-	-	0 1	-	-	**Treble soft-step** On Off
-	-	-	-	0 1	-	-	-	**Middle soft-step** On Off
-	-	-	0 1	-	-	-	-	**Bass soft-step** On Off
-	-	0 1	-	-	-	-	-	**Speaker LF soft-step** On Off
-	0 1	-	-	-	-	-	-	**Speaker RF soft-step** On Off
0 1	-	-	-	-	-	-	-	**Speaker LR soft-step** On Off

Table 12. Soft-step II / DC detector (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Speaker RR soft-step** On Off
-	-	-	-	-	-	0 1	-	**Subwoofer left soft-step** On Off
-	-	-	-	-	0 1	-	-	**Subwoofer right soft-step** On Off
-	-	-	-	0 1	-	-	-	**Soft-step time** 5 ms 10 ms
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Zero-comparator window size** ±90 mV ±60 mV ±45 mV ±30 mV
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Spike rejection time constant** 11 µs 22 µs 33 µs 44 µs

Table 13. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	**Attenuation** 0 dB -1 dB : <u>-14 dB</u> -15 dB
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Center frequency** Flat 400 Hz 800 Hz <u>2400 Hz</u>
-	0 1	-	-	-	-	-	-	**High boost** On <u>Off</u>
0 1	-	-	-	-	-	-	-	**Soft-step action** Act <u>Wait</u>

Table 14. Volume (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
	0	0	0	0	0	0	0	+0 dB
	0	0	0	0	0	0	1	+1 dB
	0	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15 dB
	0	0	1	0	0	0	0	+16 dB
	0	:	:	:	:	:	:	:
	0	0	1	0	1	1	1	+23 dB
	0	0	1	1	0	0	0	Not used
	0	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	Not used
-	0	1	0	0	0	0	0	-0 dB
	0	:	:	:	:	:	:	:
	0	1	0	1	1	1	1	-15 dB
	0	:	:	:	:	:	:	:
	0	1	1	1	1	1	0	-30 dB
	0	1	1	1	1	1	1	-31 dB
	1	0	0	0	0	0	0	-32 dB
	1	0	0	0	0	0	1	-33 dB
	1	:	:	:	:	:	:	:
	1	0	1	1	1	1	1	-63dB
	1	1	x	x	x	x	x	Not used
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 15. Treble filter (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Treble center frequency
	0	0						10.0 kHz
-	0	1	-	-	-	-	-	12.5 kHz
	1	0						15.0 kHz
	1	1						17.5 kHz
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 16. Middle filter (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Middle Q factor
	0	0						0.75
-	0	1	-	-	-	-	-	1
	1	0						1.25
	1	1						Reserved
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 17. Bass filter (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Bass Q factor
	0	0						1.0
-	0	1	-	-	-	-	-	1.25
	1	0						1.5
	1	1						2.0
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 18. Subwoofer / middle / bass (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Subwoofer cut-off frequency
						0	0	55 Hz
-	-	-	-	-	-	0	1	85 Hz
						1	0	120 Hz
						1	1	160 Hz
								Subwoofer output phase
-	-	-	-	-	0	-	-	180 deg
					1			0 deg
								Middle center frequency
			0	0				500 Hz
-	-	-	0	1	-	-	-	1000 Hz
			1	0				1500 Hz
			1	1				2500 Hz
								Bass center frequency
	0	0						60 Hz
-	0	1	-	-	-	-	-	80 Hz
	1	0						100 Hz
	1	1						200 Hz
								Bass DC mode
0	-	-	-	-	-	-	-	On
1								Off

Table 19. Speaker attenuation (FL/FR/RL/RR/SWL/SWR) (13-18)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
	0	0	0	0	0	0	0	+0 dB
	0	0	0	0	0	0	1	+1 dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15 dB
-	0	0	1	0	0	0	0	-0 dB
	0	0	1	0	0	0	1	-1 dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78 dB
	1	0	1	1	1	1	1	-79 dB
	1	1	x	x	x	x	x	mute
								Soft-step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 20. Testing audio processor 1 (19)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Audio processor testing mode
-	-	-	-	-	-	-	0	Off
							1	On
								Test multiplexer at DCSEL (1)
			0	0	0	0		SSCLK
			0	0	0	1		REQ
			0	0	1	0		SMCLK
			0	0	1	1		DCDet Vth High
			0	1	0	0		DCDet Vth Low
			0	1	0	1		IntZeroErr
-	-	-	0	1	1	0	-	Ref5V5
			0	1	1	1		VGB1.95
			1	0	0	0		Clock200k
			1	0	0	1		SDCLK
			1	0	1	0		VrefDCO
			1	0	1	1		REQ_TEST
			1	1	x	x		Reserved
								Clock fast mode (2)
-	-	0	-	-	-	-	-	On
		1						Off

Table 20. Testing audio processor 1 (19) (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	0 1	-	-	-	-	-	-	**Clock source** (2) External (MUTE Pin) Internal (200 kHz)
0 1	-	-	-	-	-	-	-	**Attenuator gain clock control** (2) On Off

1. The control bit needs both I²C test mode on & sub-address test mode on.
2. The control bit does not depend on test mode.

Table 21. Testing audio processor 2 (20)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Test architecture** (1) Normal Split
-	-	-	-	-	-	0 1	-	**Oscillator clock** (2) 400 kHz 800 kHz
-	-	-	-	-	0 1	-	-	**Soft-step curve** (2) S-Curve Linear curve
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Manual set busy signal** (1) Auto Auto 0 1
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Request for clk generator** (1) Allow Allow Stopped Stopped
-	-	0 1	-	-	-	-	-	**No DCO spike rejection**(1) On Off
x	x	-	-	-	-	-	-	**Not used**

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

Table 22. Testing audio processor 3 (21)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Enable clock for FL/FR/RL/RR/SWL/SWR** On Off
-	-	-	-	-	-	0 1	-	**Enable clock for volume** On Off
-	-	-	-	-	0 1	-	-	**Enable clock for treble and bass** On Off
-	-	-	-	0 1	-	-	-	**Enable clock for loudness and middle** On Off
x	x	x	x	-	-	-	-	**Not used**

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

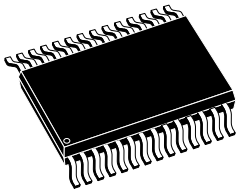
ECOPACK® is an ST trademark.

Figure 22. TSSOP28 mechanical data and package dimensions

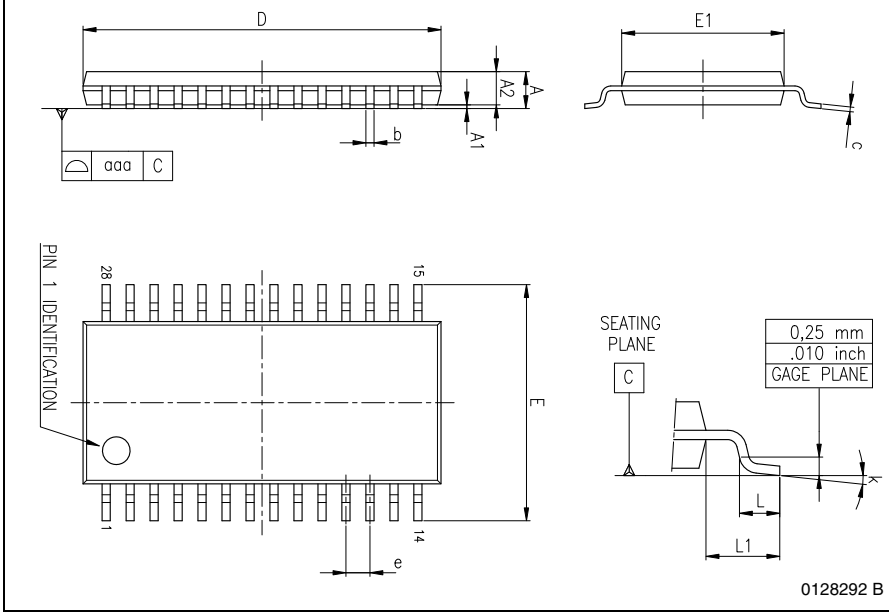
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	9.600	9.700	9.800	0.378	0.382	0.386
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.), 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or po trusions shall not exceed 0.1 5mm (.006inch) per side.

OUTLINE AND MECHANICAL DAT A



TSSOP28
Thin Shrink Small Outline Package
JEDEC MO-153-AC



GAPGPS00889

7 Revision history

Table 23. Document revision history

Date	Revision	Changes
01-Mar-2013	1	Initial release.
16-Sept-2013	2	Updated Disclaimer

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